Impact of Manufacturing Defects on Carbon Nanotube Logic Circuits

Daniel Gil, David de Andrés, Juan-Carlos Ruiz, Pedro Gil
Fault Tolerant Systems Research Group, Instituto de Aplicaciones de las TIC Avanzadas
Universidad Politécnica de Valencia, Campus de Vera s/n, 46022, Spain Phone: +34 96 3877007 Ext {75777, 75752, 85703, 79707}, Fax: +34 96 3877579
{dgil, ddandres, jcruizg, pgil}@disca.upv.es

As CMOS technology enters the nanoelectronics realm (tens of nanometres and below), where quantum mechanical effects start to prevail, conventional CMOS devices are meeting many technological challenges for further scaling. This situation has motivated the emergence of a variety of new nanoelectronic devices [1] [2]. However, as new generations of nanodevices are developed, we become less familiar with their fault mechanisms and the causes behind their failures [3]. On the one hand, the nature of the materials and the physical phenomena used in these technologies are very different from current CMOS. On the other, it is widely acknowledged that the small sizes of resulting devices will cause higher levels of manufacturing defects than those of current CMOS solutions. In addition, in-service (transient and permanent) faults will have to be dealt with [4]. This situation justifies why reliability has become (and will be) a big challenge in the design of current (and future) nanoelectronic devices and architectures.

The confident use of these emerging technologies relies on our capacity to better understand their fault mechanisms, and our ability to develop related fault models. Those fault models can be considered as a step forward towards the dependability assessment of emerging architectures for the definition of new and efficient fault mitigation techniques [5].

Among the wide set of new emerging nanoelectronic devices, 1D structures, as Carbon Nanotubes (CNTs) and Silicon Nanowires (SiNWs), are among the most promising for the development of logic circuits [6]. They present the best values for a number of factors that evaluate their potential use, like scalability, gain, operational reliability, performance, room temperature operation, energy efficiency, and CMOS technological and architectural compatibility. In addition, programmable logic array reconfigurable architectures are suggested for 1D structures. As we already analysed SiNWs [7], this study will focus on CNTs.

CNTs have mechanical and electrical properties that make them very attractive as nanoelectronic wires and devices. Due to their structure, CNTs have an extraordinary strength and can behave as metallic wires or semiconductors, depending on their chirality and diameter [8] [9]. Metallic wire CNTs can offer superior electrical properties to SiNWs or copper [10]. As semiconductors, CNTs allow the design of field effect transistors (CNTFET). They have a MOSFETs-like structure (which is depicted in Figure 1) but present some potential key advantages: smaller channel and ballistic transport of electrons. Despite the good CNTs properties, the main hurdles concern their fabrication: selectively controlling their electronic properties (e.g. metallic or semiconducting) and placement [8].

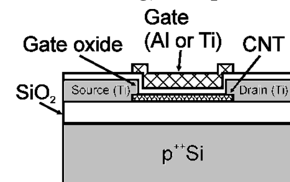

Figure 1. Carbon Nanotube Field Effect Transistor [1].

This work first reports the main manufacturing defect causes and mechanisms, extracted from the literature, of CNT-based logic circuits. Then, the resulting error propagation is analysed to deduce fault models at device and logic abstraction levels. These fault models, that constitute the main contribution of this paper, will enable the future development and precise parameterisation of defect and fault-tolerant architectures for nanoelectronic systems (see Figure 2).

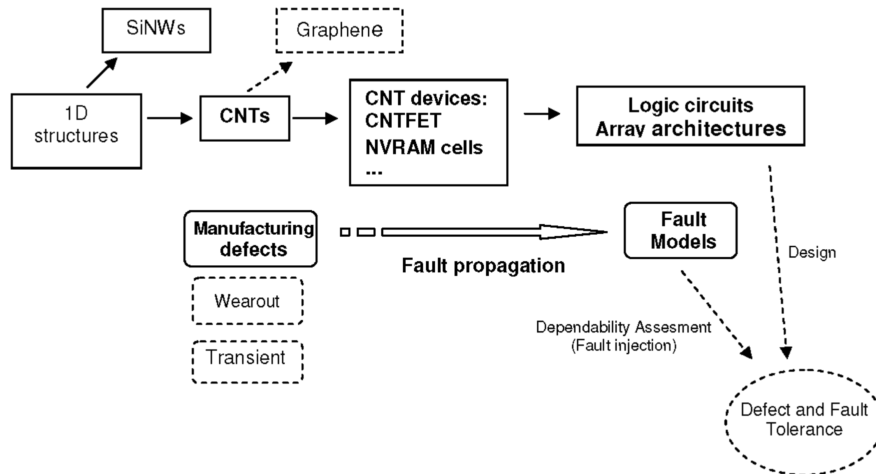

Figure 2. Applied methodology: fault manifestation at higher abstraction levels.

Table 1 lists relevant manufacturing defects reported in the bibliography, and their effects on CNT FETs and array-based devices (non-volatile RAM or PLAs). CNT defects include: metallic CNTs [11] [12] [13], misaligned/miss-positioned CNTs [12], open CNTs [14], poor contacts [1] [15], parametric variations [15] [16], and erroneous doping [15]. Related causes and mechanisms, along with their effect on CNTFET characteristics, are also summarised in Table 1. Defects in programmable crosspoints lead to non-programmable or shorted crosspoints.

Table 2 suggests fault models at device level. They have been deduced from the structure of CNTFETs and non-volatile RAM cells (see Figure 3).

Table 1. Manufacturing defects and their effect on devices.

Manufacturing defects		Causes and mechanisms	Effects on CNT FET
CNT defects	Metallic	Bad chirality control	Resistive D-S shorts Excessive leakage Degraded noise margins Delay variations
	Misaligned/Miss-positioned	CNT passes under incorrect gate CNT outside gate	D-S open, connection with other transistors D-S short
	Open	Mechanical stress, bending	D-S open
	Poor contacts	Defect CNT-metal contacts	Increase of the channel resistance
	Parametric variation	Diameter, length, gate oxide thickness	Threshold voltage (V_T) variation Channel resistance variation
	Erroneous doping	PMMA mask misalignment in complementary gates	Channel cannot be N-doped
Crosspoint defects*	Open crosspoint	Crossed CNTs make imperfect contact	Non-programmable crosspoint
	Short crosspoint	Crossed CNTs have imperfect separation	Shorted crosspoint

Table 2. Fault models at device and logic level.

Manufacturing defects		CNT FET	Logic circuits
CNT defects	Metallic	Stuck-on Delay	Stuck-at (0,1), indetermination Delay
	Misaligned/Miss-positioned	Stuck-off Stuck-on	Incorrect logic behaviour Stuck-at (0,1) Loss of memory behaviour
	Open	Stuck-off	Stuck-at (0,1) High-impedance Loss of memory behaviour
	Poor contacts	Delay	Delay
	Parametric variation	Delay	Delay
	Erroneous doping	N-type → P-type	Incorrect logic behaviour
Crosspoint defects*	Open crosspoint	Non-programmable	Stuck-at 0
	Short crosspoint	Shorted	Stuck-at 1

* In NVRAM or PLA cells.

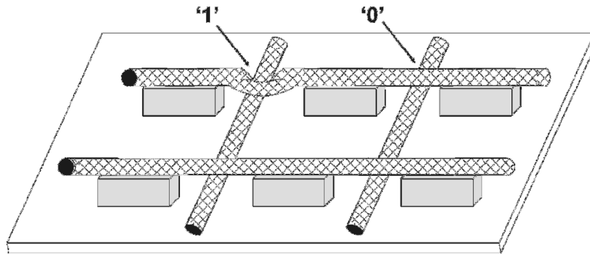

Figure 3. CNT non-volatile RAM [8].

Fault models at logic level have been deduced from the structure of real logic circuits made of transistors. Figures 4 to 7 show some representative examples of simple logic gates and SRAM cell that have been fabricated and tested. They were used to study faults propagation towards the logic abstraction level.

From the results condensed in Tables 1 and 2, we can extract the following conclusions:

(i) Manufacturing defects are mainly related to defects in the CNT (the channel) of transistors, or the crosspoints of array-based devices. Some of them are similar to those found in SiNWs devices [7]: open, poor contacts, erroneous doping, and open/short crosspoints. Others are more specific to CNT technology: conducting (metallic), misaligned/miss-positioned, and parametric variation of the CNTFET channel. These are the most frequent and troublesome. Stochastic assembly manufacturing process makes nearly impossible to guarantee the perfect alignment and accurate positioning of all CNTs at VLSI scale, or the growing of semiconducting CNTs exclusively.

(ii) Manufacturing defects manifest at transistor level mainly as well-known stuck-on, stuck-off and delay fault models. This is due to its structural similarity to MOSFET transistors, although its behaviour arises from Schottky barriers at the source-CNT interface and its interaction with electric fields.

(iii) Most fault models at logic level are well-known fault models in MOSFET technology: stuck-at (0/1), delay and, with less incidence, high-impedance and indetermination. The reason is double: CNT devices are electronic charge-based devices, and CNT-based logic circuits present NMOS- or CMOS-like structures.

(iv) Some fault models are unusual. For instance, the function of logic gates can change due to miss-positioned/misaligned CNTs. Erroneous doping of CNTs due to misalignment of the PMMA window can modify the transistor's type (p-type instead of n-type), leading to the incorrect logic behaviour of complementary gates. The memory behaviour of SRAM cells can be lost due to opens or miss-positioning/misalignment in CNTs.

It is to note that the proposed methodology can be applied to any logic circuit regardless its complexity, and can greatly benefit from using CAD tools to simulate CNT device models to obtain quantitative results.

Some challenges requiring a further research include (see Figure 2):

(i) The study of operational faults, particularly, wear out processes and environmental agents that provoke transient faults in CNT circuits.

(ii) A similar overall research for other promising devices (for instance graphene, spintronic and molecular devices) [6].

(iii) The development of defect and fault tolerance techniques for architectures based on CNT devices. The question is how to handle the very high defect rates of all individual devices and wires, in systems with over 10^{12} devices per cm^2. Traditional techniques must be adapted to these stringent conditions [8].

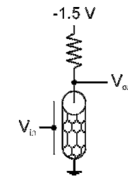

Figure 4. Inverter gate [1].

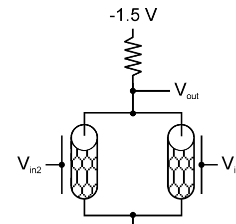

Figure 5. NOR gate [1].

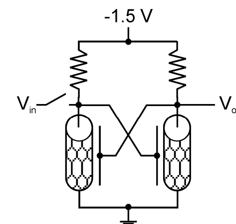

Figure 6. SRAM cell [1].

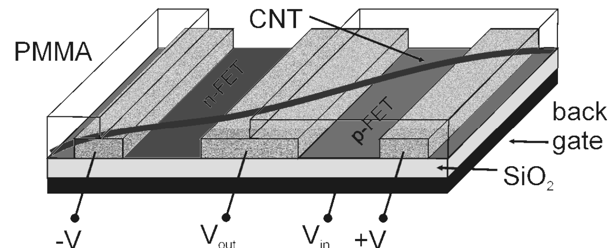

Figure 7. Intramolecular complementary inverter [17].

Acknowledgements

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