Third Workshop on Dependable and Secure Nanocomputing Preface

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The Workshop is aimed at focusing on the emerging challenges that are attached to the evolution of hardware designs and semiconductor technologies. Two main tracks are being considered to incorporate an increasingly large number of devices and processing elements into a chip:

1. Top-down "More Moore": pushing further the long standing Moore's Law-based trend that is progressively reaching nanometric scale elementary devices.
2. Bottom-up "Beyond Moore": featuring atomic assemblies of nanoscale technologies, e.g., carbon nanotubes, organic molecules, and extending to quantum computing and micro/nanofluidics.

This series of Workshop was established in 2007 in the frame of DSN-2007. Both editions already run were quite successful: each gathered about 50 participants and resulted in fruitful and lively discussions among the contributors and the attendees. Of course, not all issues at stake could be addressed with sufficient level of details then and also the field is moving really fast which raises novel challenges. Accordingly, we are pleased to welcome you to this third edition. Due to the back-to-back scheduling of IOLTS and DSN, this year, the Workshop is thus an authentic crossroad for the respective communities!

Let us summarize here the aim of the Workshop; it is twofold: i) better characterization the hardware-related threats; ii) identifying possible design paradigms and techniques for sustaining dependable and secure computing. More specifically, the intent is to:

1. *Review* the state-of-knowledge about main threats in nanoscale technologies: manufacturing defects, operational faults, and malicious attacks.
2. *Identify* existing solutions and *propose* new solutions attached to various design options for mitigating faults and implementing resilient computing devices and systems.
3. *Forecast* the risks associated to emerging technologies and *foster* new trends for cooperative work, possibly combining various alternatives to help increase the pace of advances and solutions.

The feedback received from the community was, once again, very good: 11 papers were submitted, involving nine different countries. Each of these submissions has been reviewed by at least four members of the Program Committee. We are extremely thankful to them for their support in the evaluation process and especially for their dedication in providing insightful feedback to the authors.

This evaluation has shown the richness and large scope of the submitted contributions, spanning many issues relevant for and influenced by nanoscale technologies: manufacturing defects, parameter variation and fault models, soft error characterization and mitigation, power efficient architectures, asynchronous design paradigm, fault tolerance techniques, integration into critical embedded systems, efficient simulation and testing, etc.

Eight of these contributions were selected to be part of the program of the Workshop. Based on first author citizenship, papers are distributed as follows: Japan (2), Austria, India, Spain, Sweden, UAE and USA (1 each). It is also worth noting that the program includes 2 tri-country papers: India-USA-Sweden, UAE-Ireland-Canada.

These contributions constitute the backbone of this year's Workshop program and are grouped into two sessions as follows: i) reliability issues and assessment, ii) resilience enhancement techniques. As a kick-off, the program is opened by a session featuring two distinguished invited speakers:

- Vikas Chandra (ARM R&D, San Jose, CA, USA): *Dependable Design in Nanoscale CMOS Technologies: Challenges and Solutions.*
- Cecilia Metra (University of Bologna, Italy): *Trading Off Dependability and Cost for Nanoscale High Performance Microprocessors: The Clock Distribution Problem.*

A panel session will end the Workshop day in order to identify and discuss issues and solutions relevant for technologies scaling towards nanometer size devices.

You will find hereafter the written material that accompanies each of the presentations given at the Workshop. For your convenience, the papers are listed according to the session schedules. We sincerely hope that you will enjoy the Workshop and actively participate! We welcome your comments and hints about this event.

Further information is available from the Workshop websites (www.laas.fr/WDSN0x, x ∈ {7, 8, 9}). In particular, the WDSN09 site will be updated after the Workshop to include the slides presented.