Multi-Level Resiliency Techniques for Nanoscale Technology

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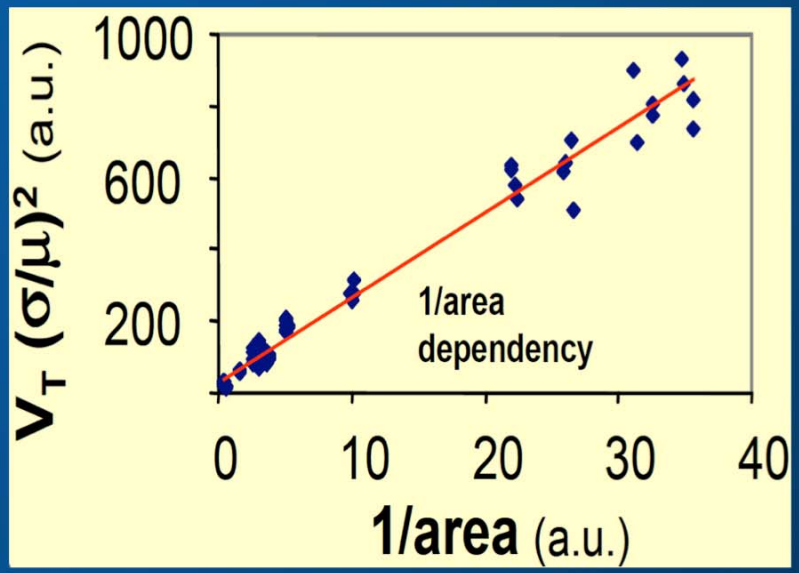
Intel Labs

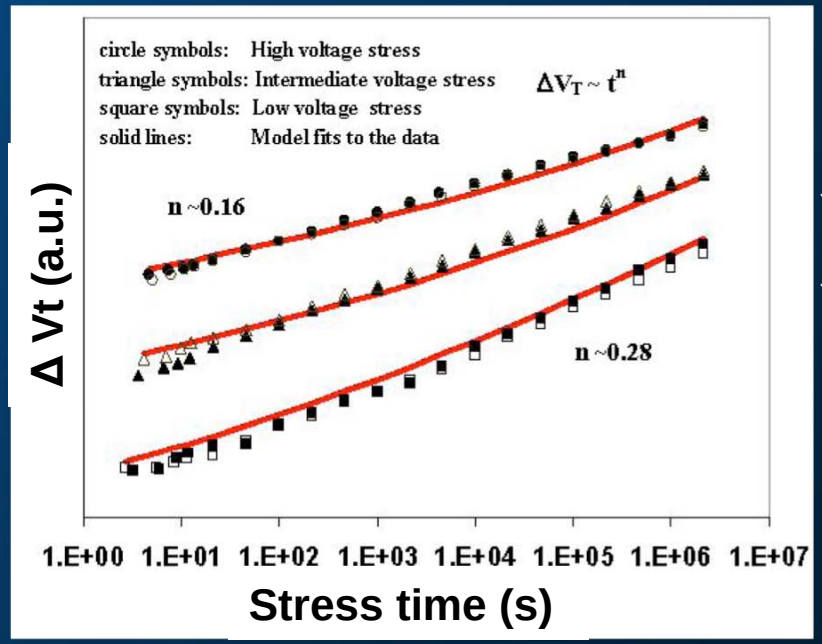
Sources of Unreliability

Variation on Vt



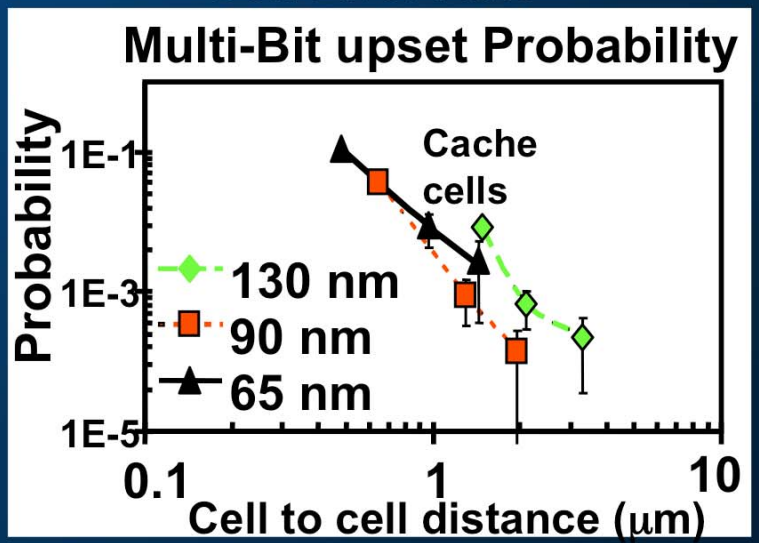
Tschanz, Intel

Aging Effect on Vt



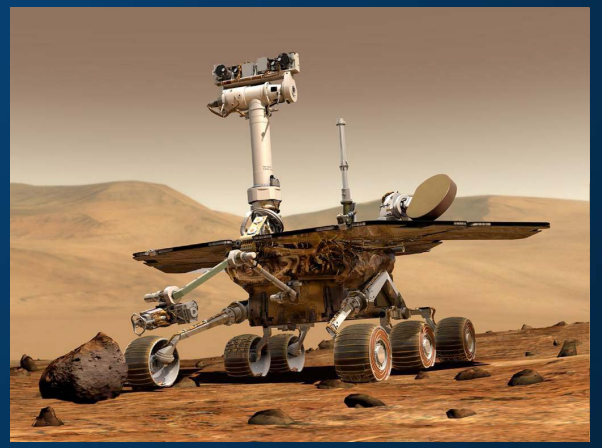
Ioannou, IBM, IRW'08

Soft Error Rate



Incremental Change or Big Change?

- High reliability requirement
  - Space program
  - Scientific Computation applications
  - Financial application
- Future Technology
  - Resiliency is essential
  - Cost is the limiting

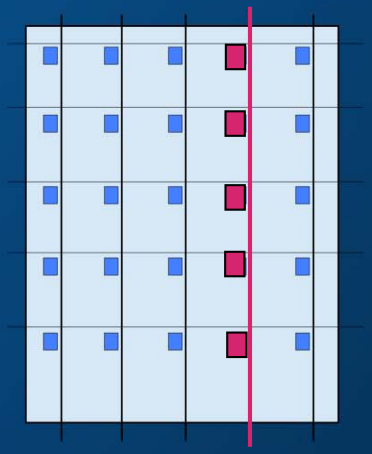


How to design inexpensive resiliency techniques for commercial systems?

An already proved approach!

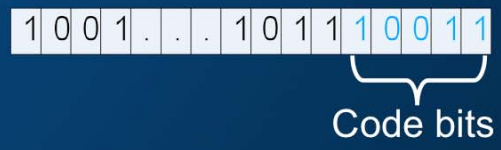
Multi-level Resiliency for Memory System

Cache Line Disable



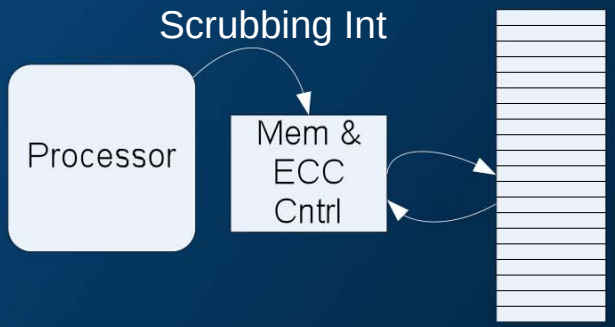
Device
Gate

Error Correcting Code



Cell
Architecture

Scrubbing Memory

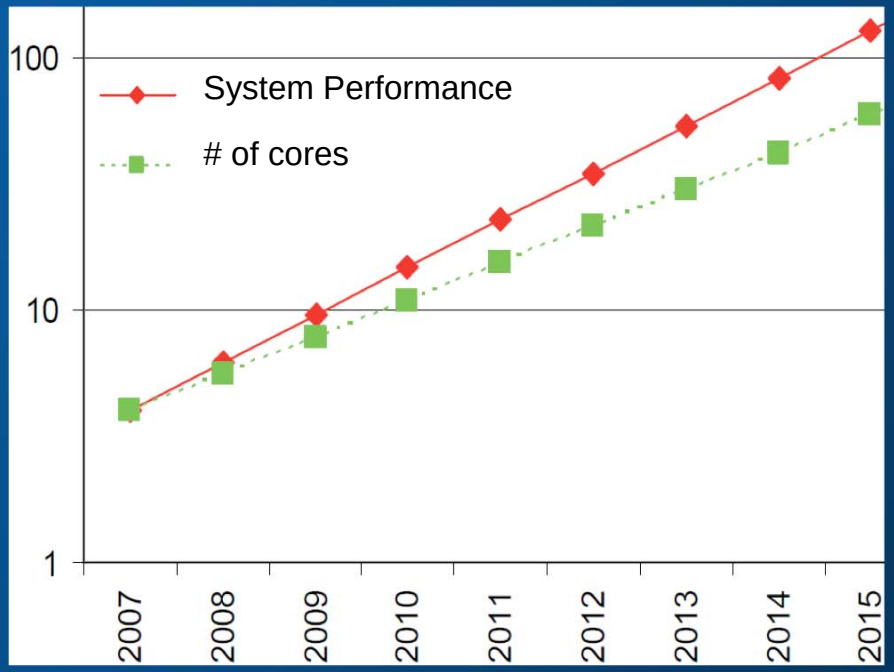


Architecture
OS

Remapping bad sectors

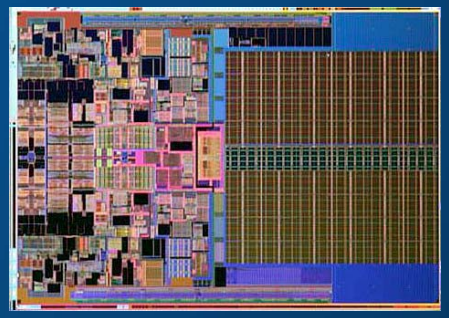
OS

System Design Trends

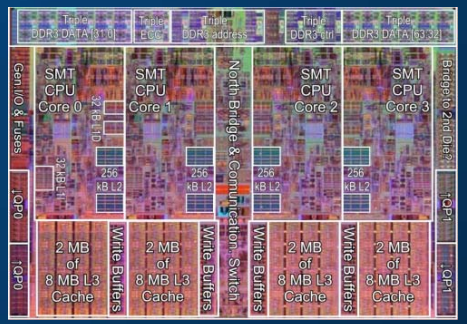


ITRS 2007-- SOC

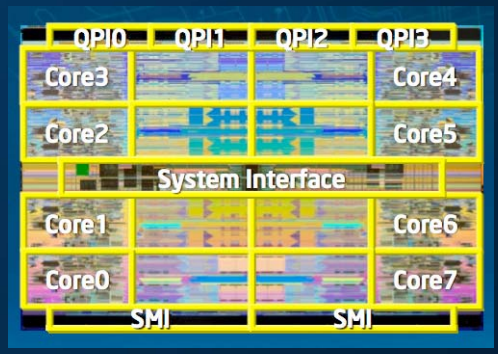
"Processors are new NAND gates."



2-core: 2007



4-core: 2008



8-core: 2009?

Multi-Level Resiliency Techniques

- How to design inexpensive resiliency techniques for commercial systems?
- Expanding resiliency techniques to the system level
  - Benefits
    - More efficient
    - Adaptive (resilient)
    - Flexible
  - Challenges
    - New Programming paradigm
    - This is not only a technical problem to solve
    - Cross-layer resiliency →cross-industry solution