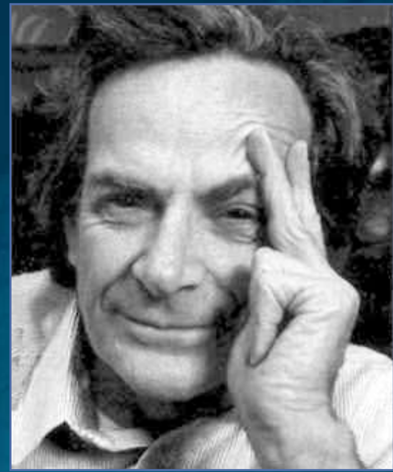
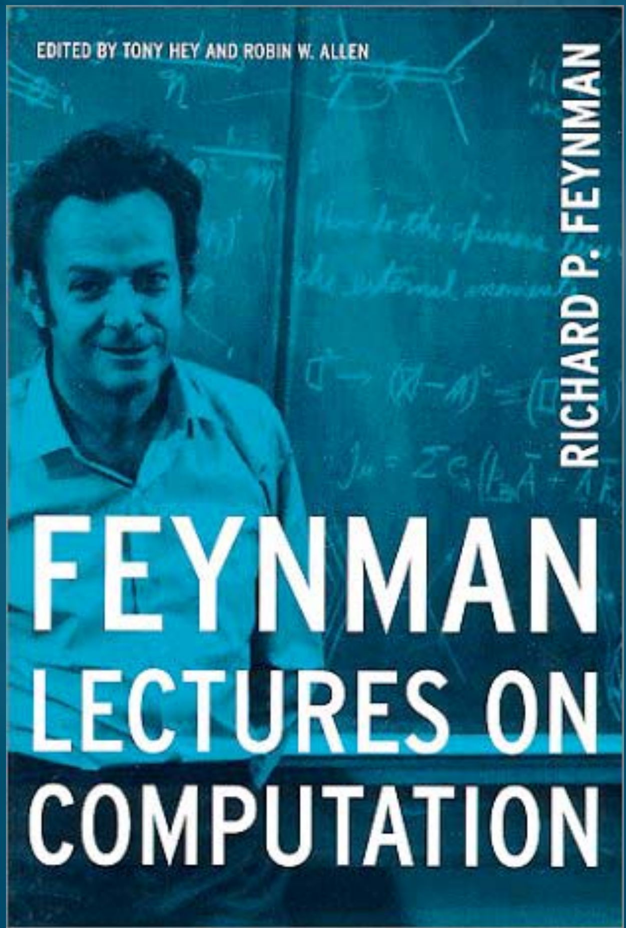
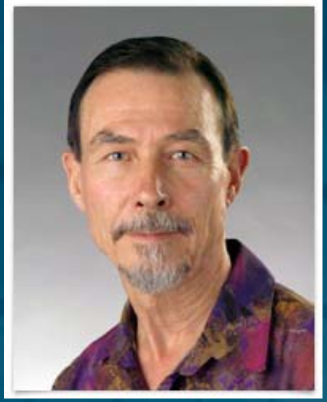
There are plenty of challenges at the top





"The principles of physics,
as far as I can see, do not
speak against the possibility
of maneuvering things atom by atom.

It is not an attempt to violate
any laws; it is something,
in principle, that can be done;
but, in practice it has not been done
because we are too big."



There are two reasons why wafer scale integration is very difficult

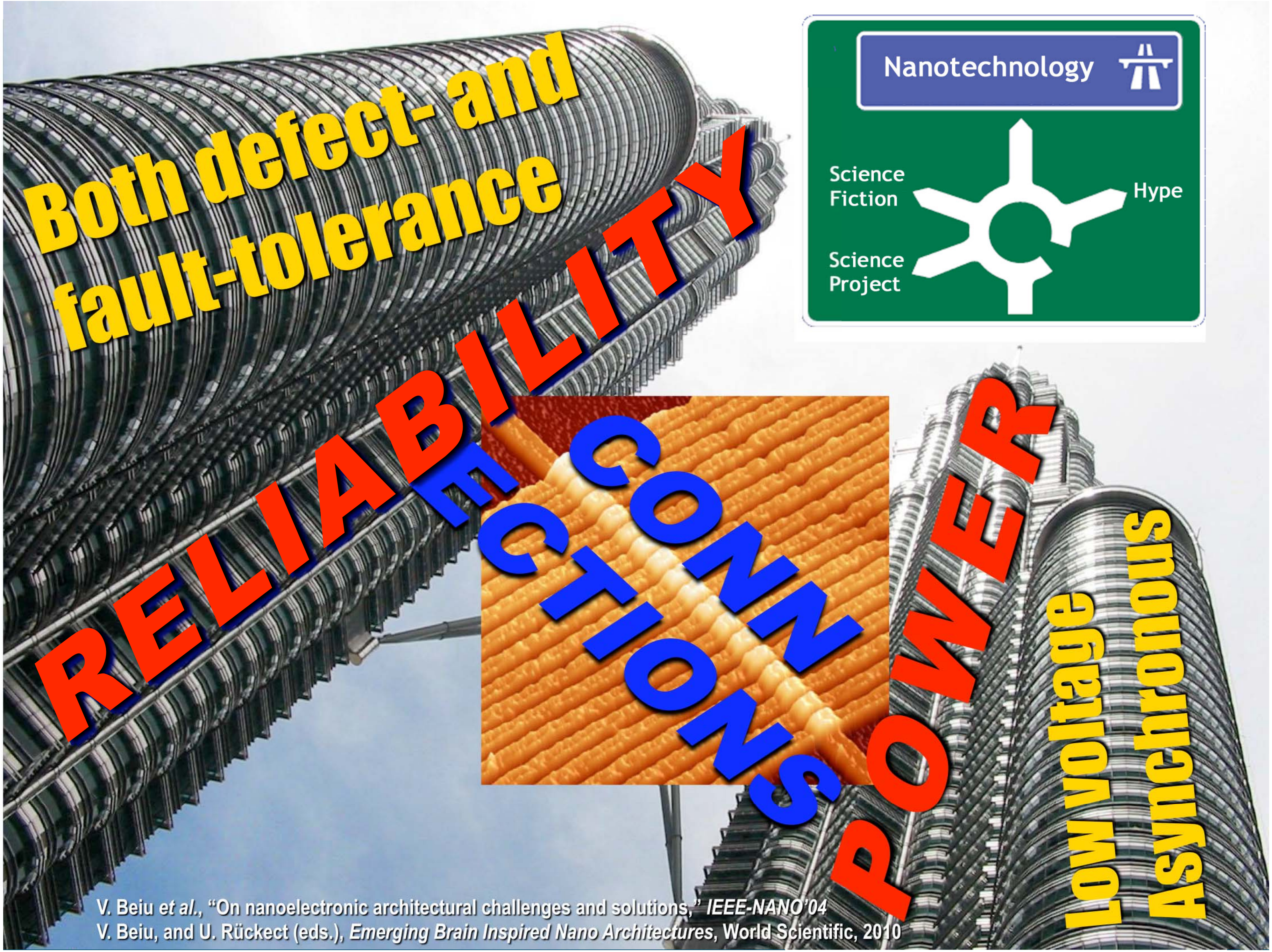
First, a typical digital chip will fail if even a single transistor or wire is defective

Second, the power dissipated by several hundred chips of circuitry is over 100W

and getting rid of all that heat is a major packaging problem

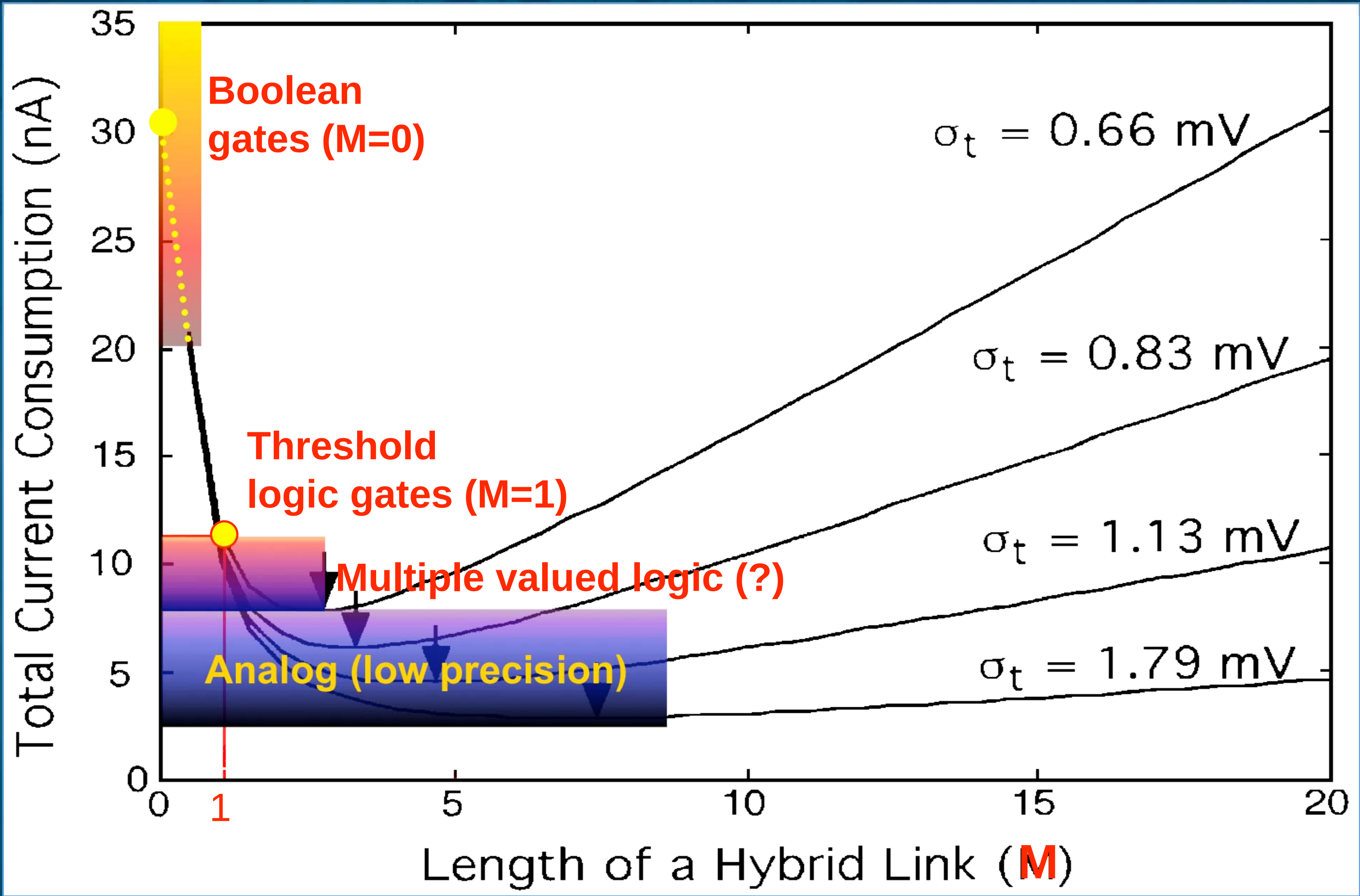
Together these two problems have prevented even the largest computer companies from deploying wafer scale systems successfully

Carver Mead



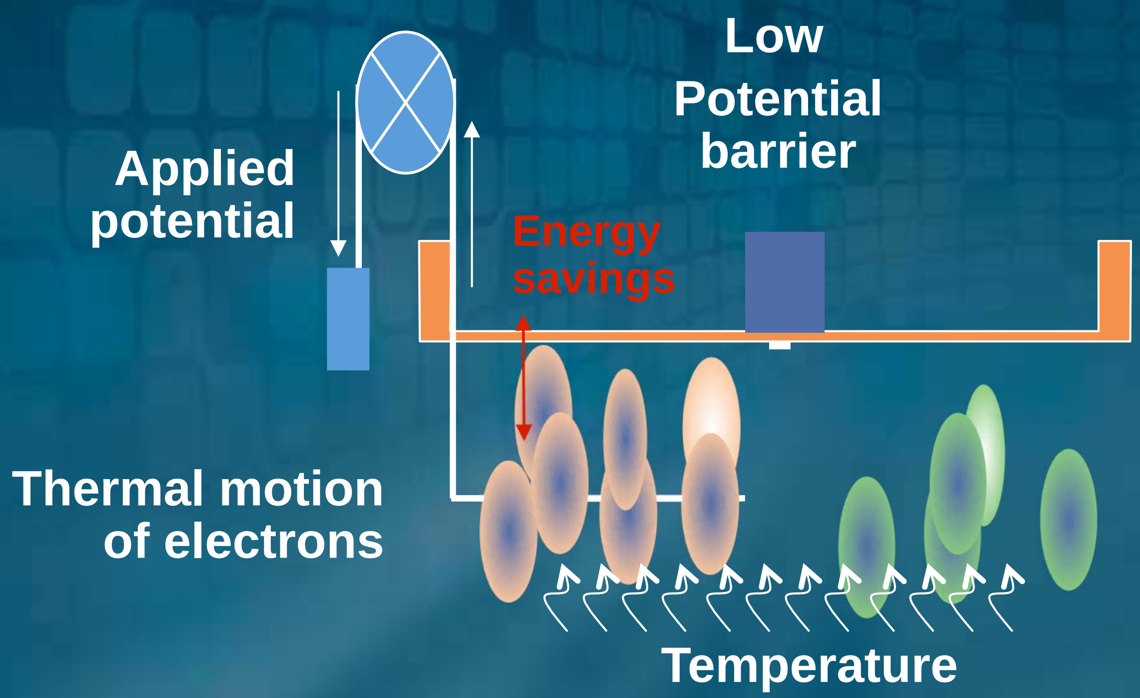
Nanotechnology
Science Fiction
Hype
Science Project
Both defect- and fault-tolerance
RELIABILITY
CONNECTIONS
POWER
Low voltage
Asynchronous
V. Beiu *et al.*, "On nanoelectronic architectural challenges and solutions," *IEEE-NANO'04*
V. Beiu, and U. Rückect (eds.), *Emerging Brain Inspired Nano Architectures*, World Scientific, 2010

Power and S-to-N (... no wires!)



R. Sarpeshkar, "Analog versus digital: Extrapolating from electronics to neurobiology," *Neural Computation*, 1998

Abstract model (of a switch)

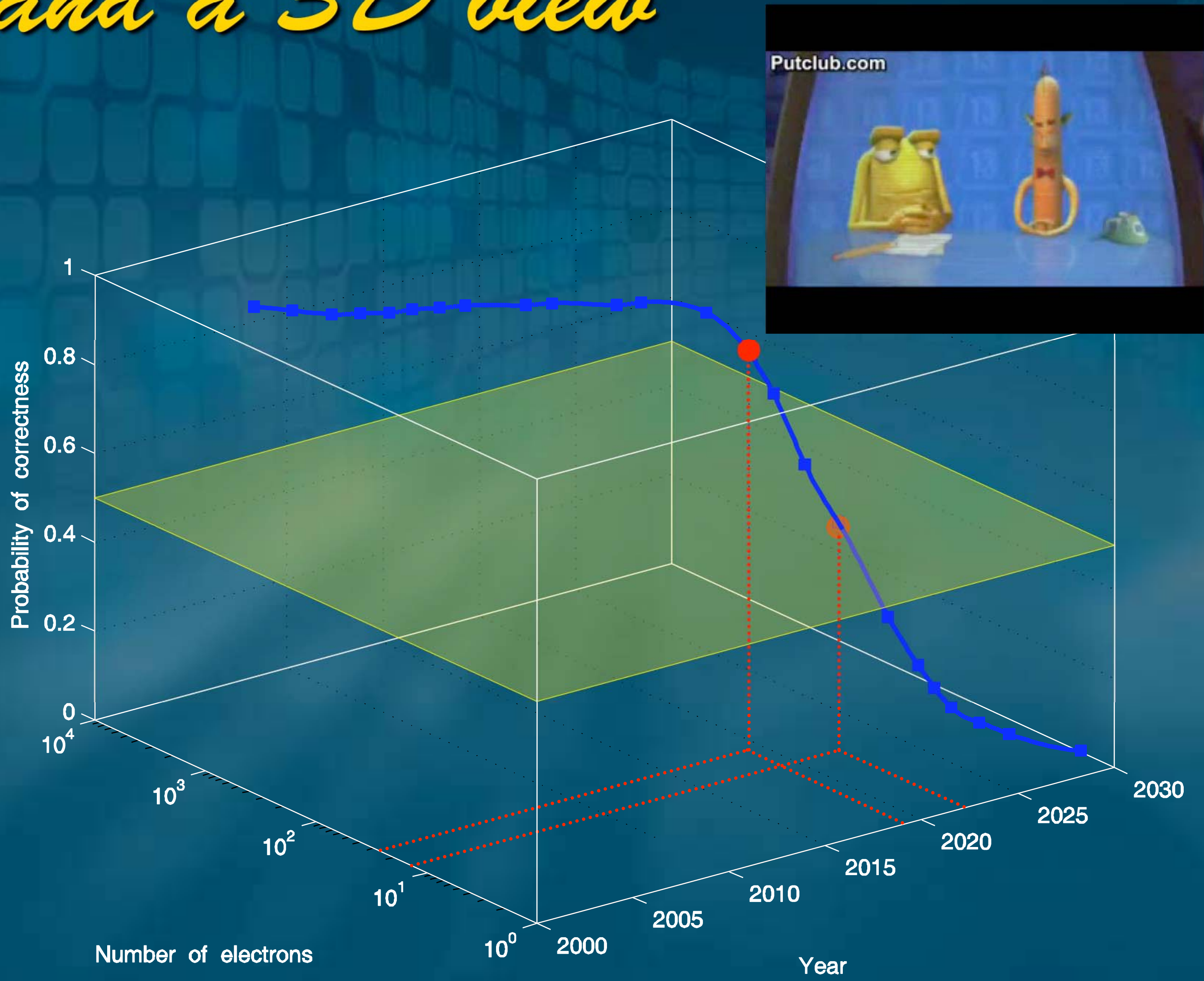


Applied potential needed to move electron across barrier

- Lower barrier implies lower energy
- Switching errors are possible since electrons can be in the wrong position due to thermal agitation

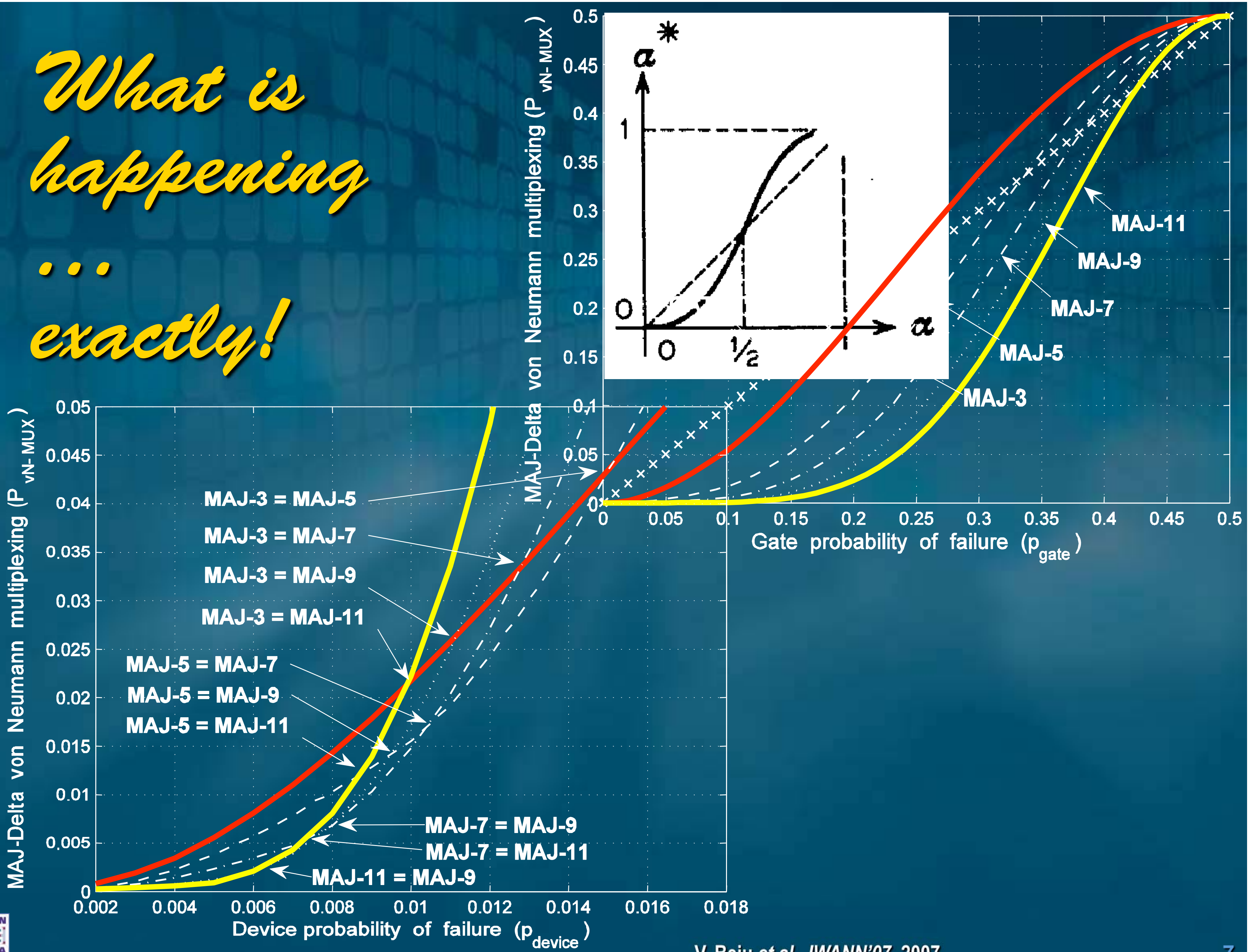
- **Energy gains related to unreliable switching**
  - **Errors in switching**
  - **Energy savings from a lower barrier at the expense of switching error**

… and a 3D view



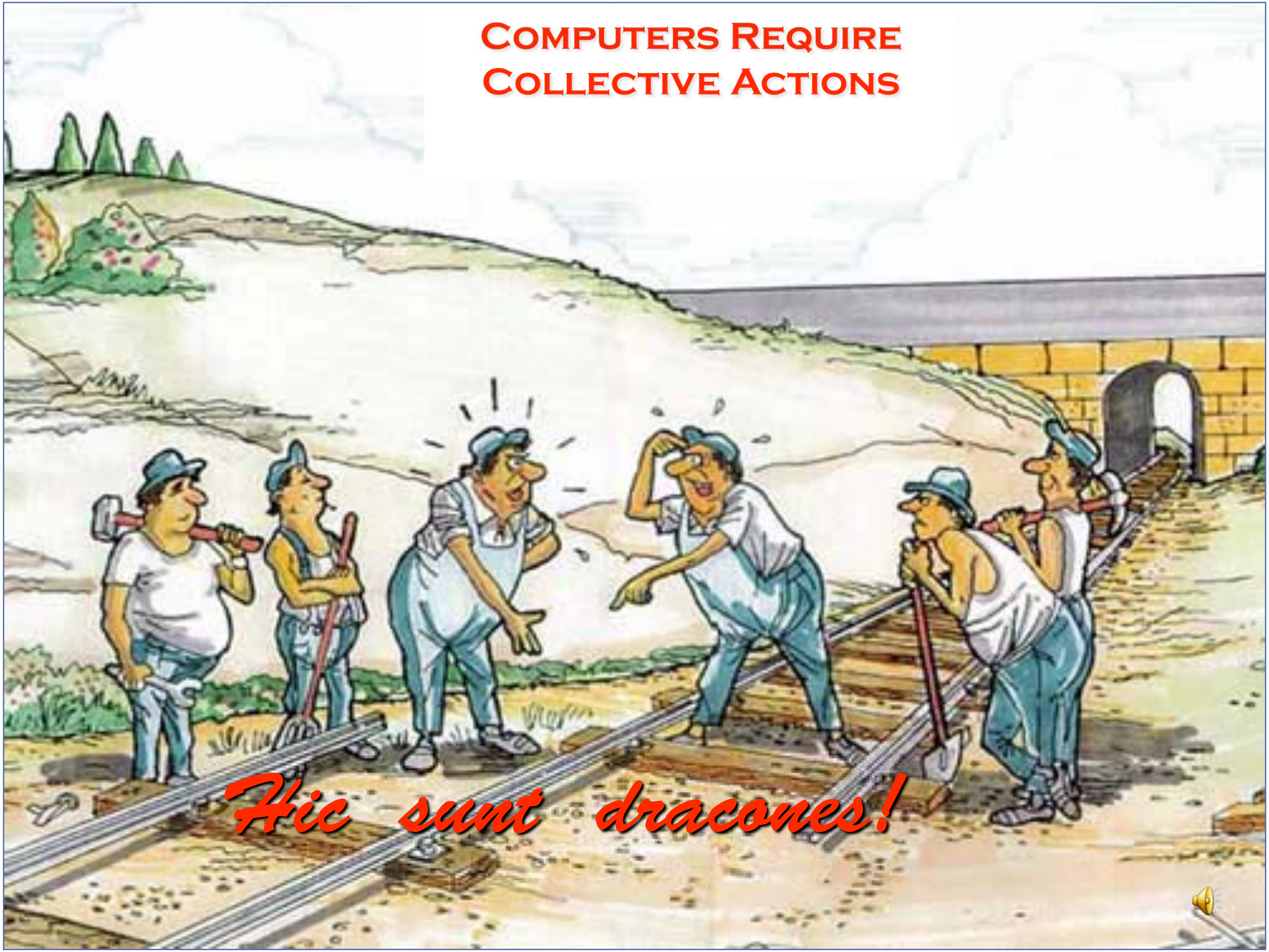
V. Beiu, 2007

What is happening … exactly!

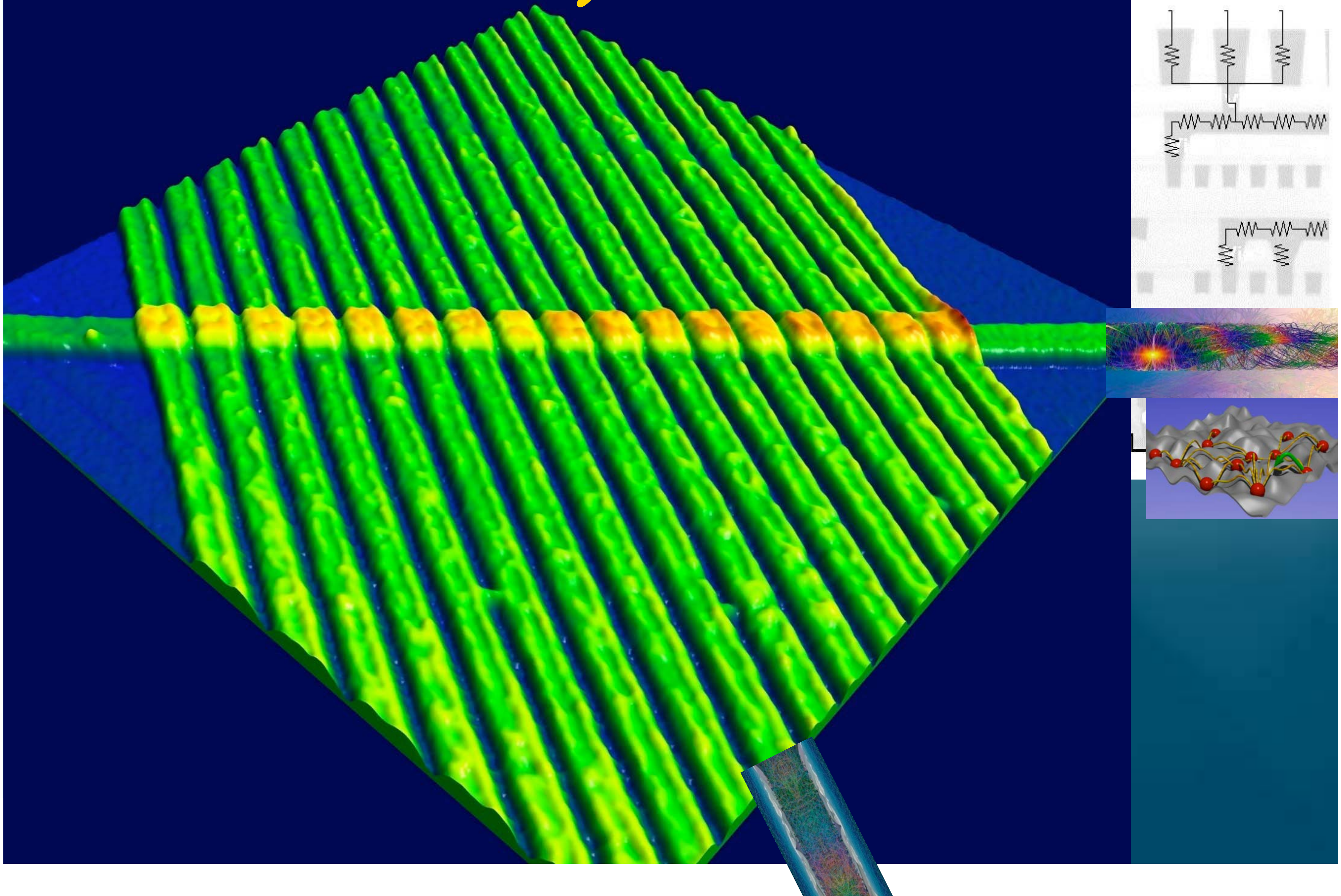


V. Beiu *et al.*, *IWANN'07*, 2007

Computers Require Collective Actions



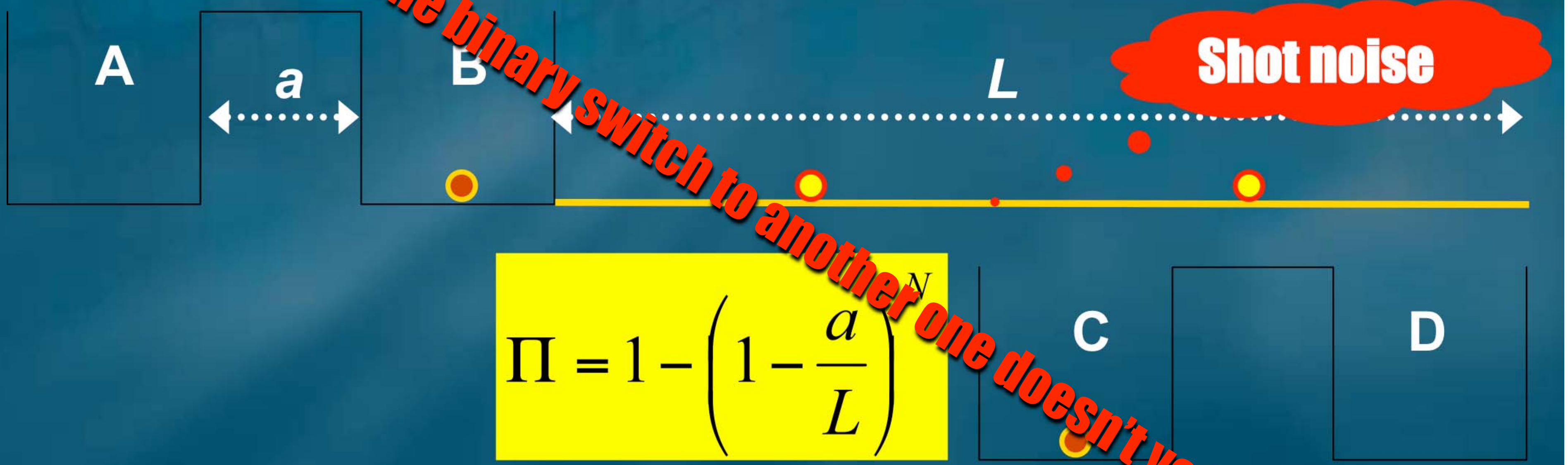
What's cooking … on the wires



Connecting two switches (via wires)

- The problem is to 'place' (at least) an electron on the downstream gate (... unfortunately, more than one electron is needed to 'charge' a wire ...)

NOTE: Connecting one binary switch to another one doesn't yet do computation!



$$\Pi = 1 - \left(1 - \frac{a}{L}\right)^N$$

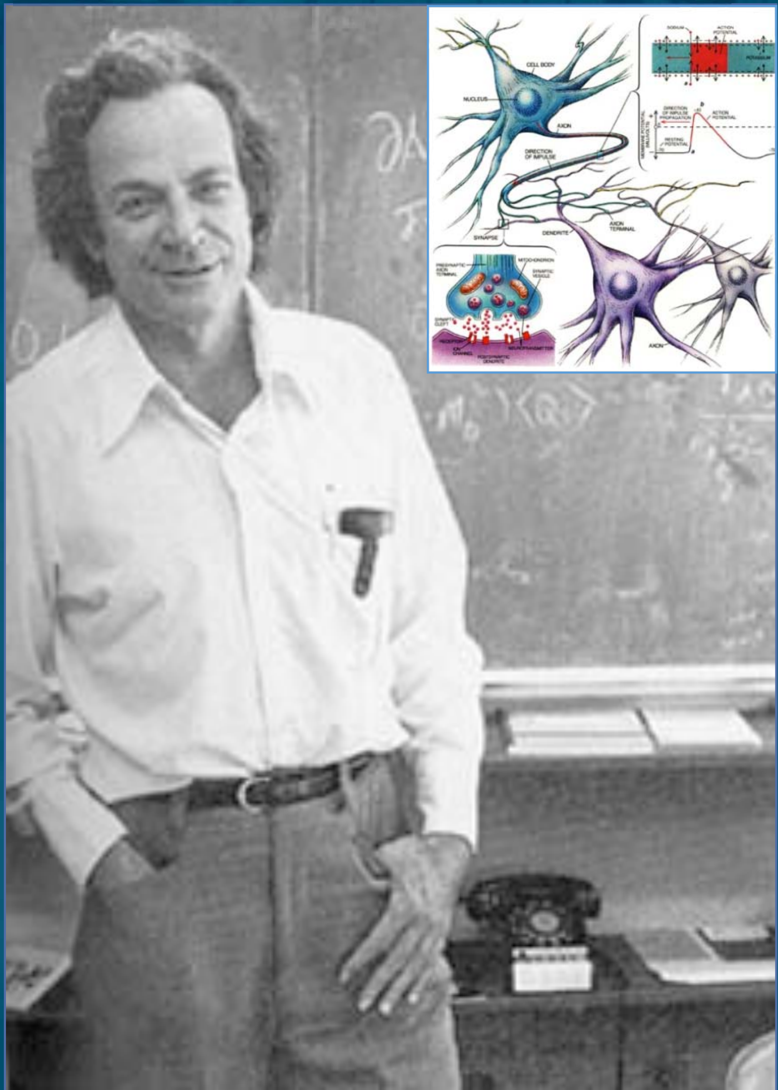
Example $L = 4a$

N = number of e

$N = 1 \quad \rightarrow \quad P < 0.25$

$$\Pi_{CD} = \frac{a}{L}$$

Biomorphic ?



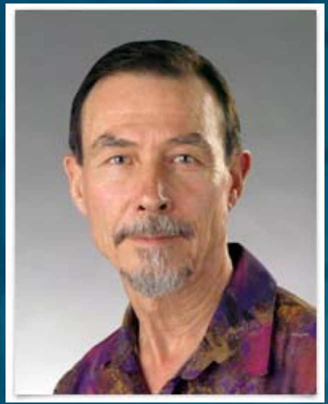
"In an actual cell, the pyrophosphate concentration is kept low by hydrolysis, ensuring that only the copying process occurs, not its inverse. The whole RNA polymerase system is not particularly efficient as far as energy use goes:

it dissipates about 100kT per bit.

Less could be wasted if the enzyme moved a little more slowly (and of course, the reaction rate does vary with concentration gradient), but there has to be a certain speed for the sake of life!

Still, 100kT per bit is considerably more efficient than the 10^8kT thrown away by a typical transistor!"

(~37,600kT in 90nm, ~15,300kT in 65nm)



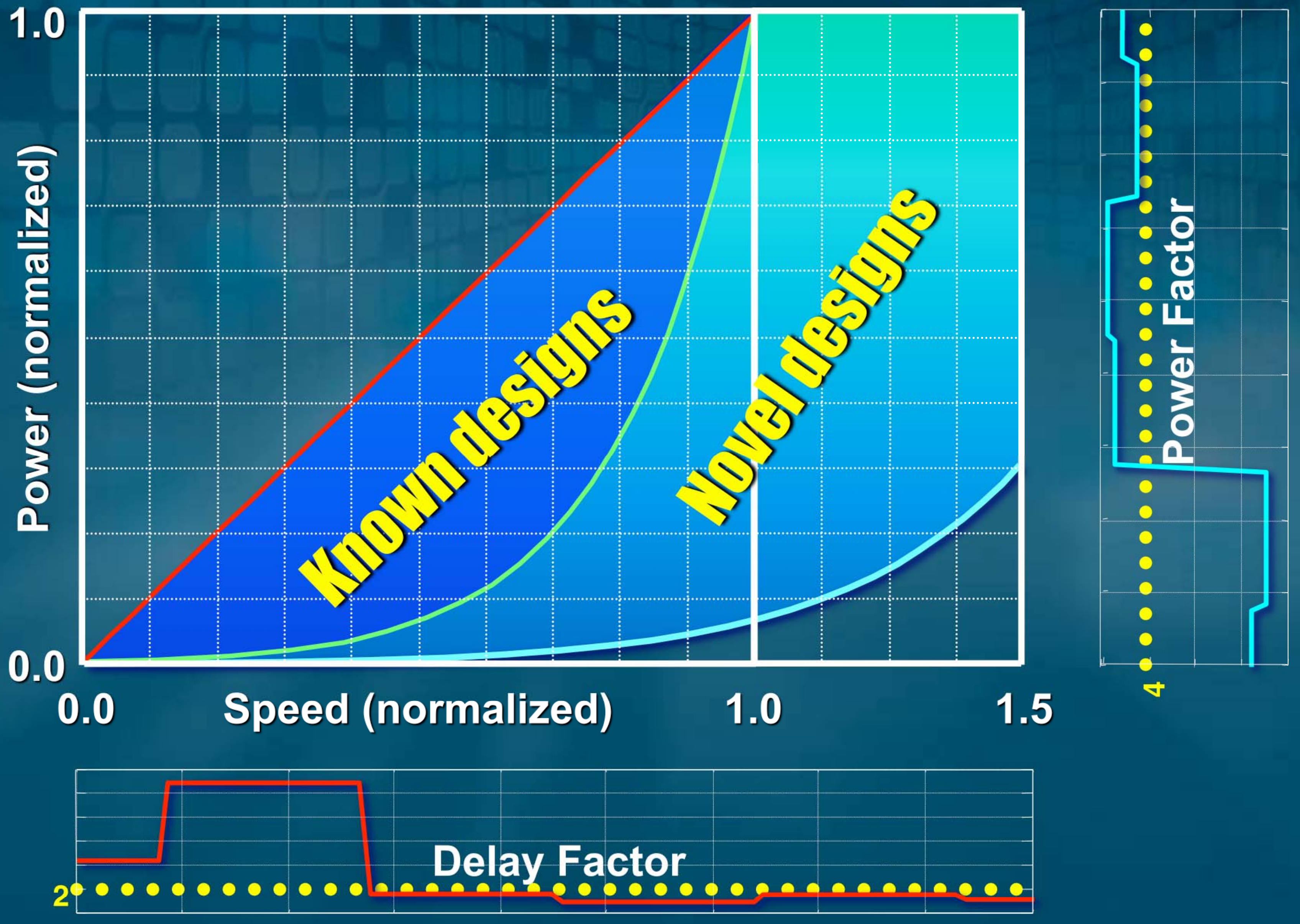
It is clear to me
that we will develop
silicon neural systems
and that learning
how to design them

is

one of the greatest
intellectual quests
of all times

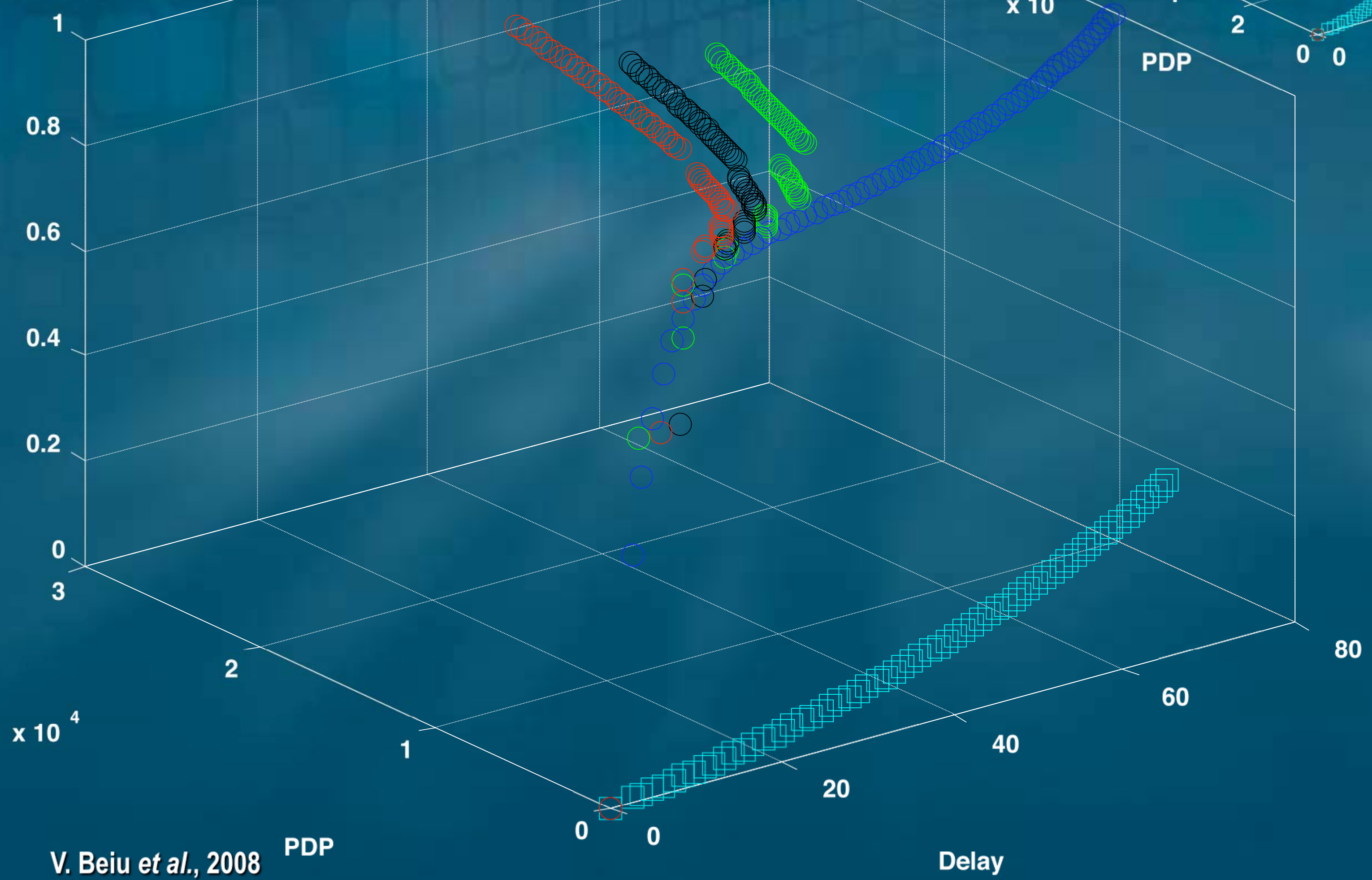
Carver Mead

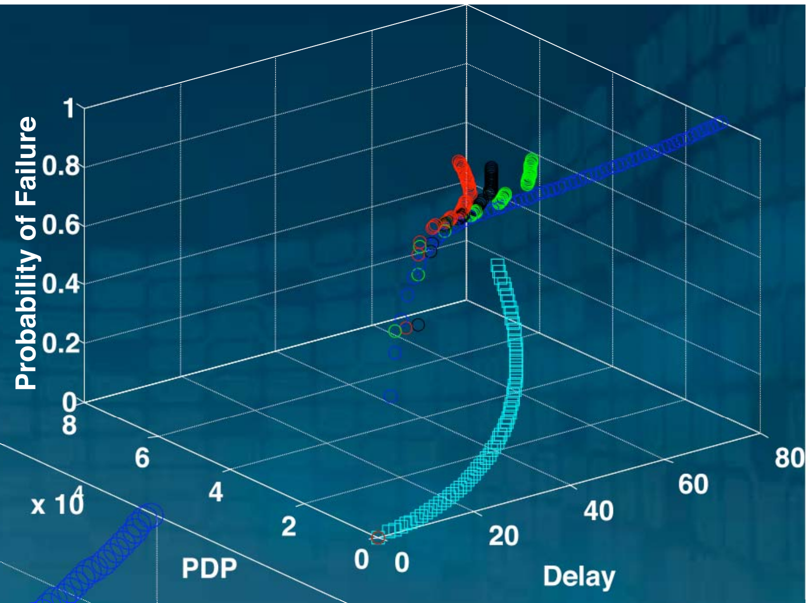
Adaptive ... the name of the game!



V. Beiu *et al.*, "Sub-pico Joule switching: High speed reliable CMOS circuits are feasible," *IIT'05*

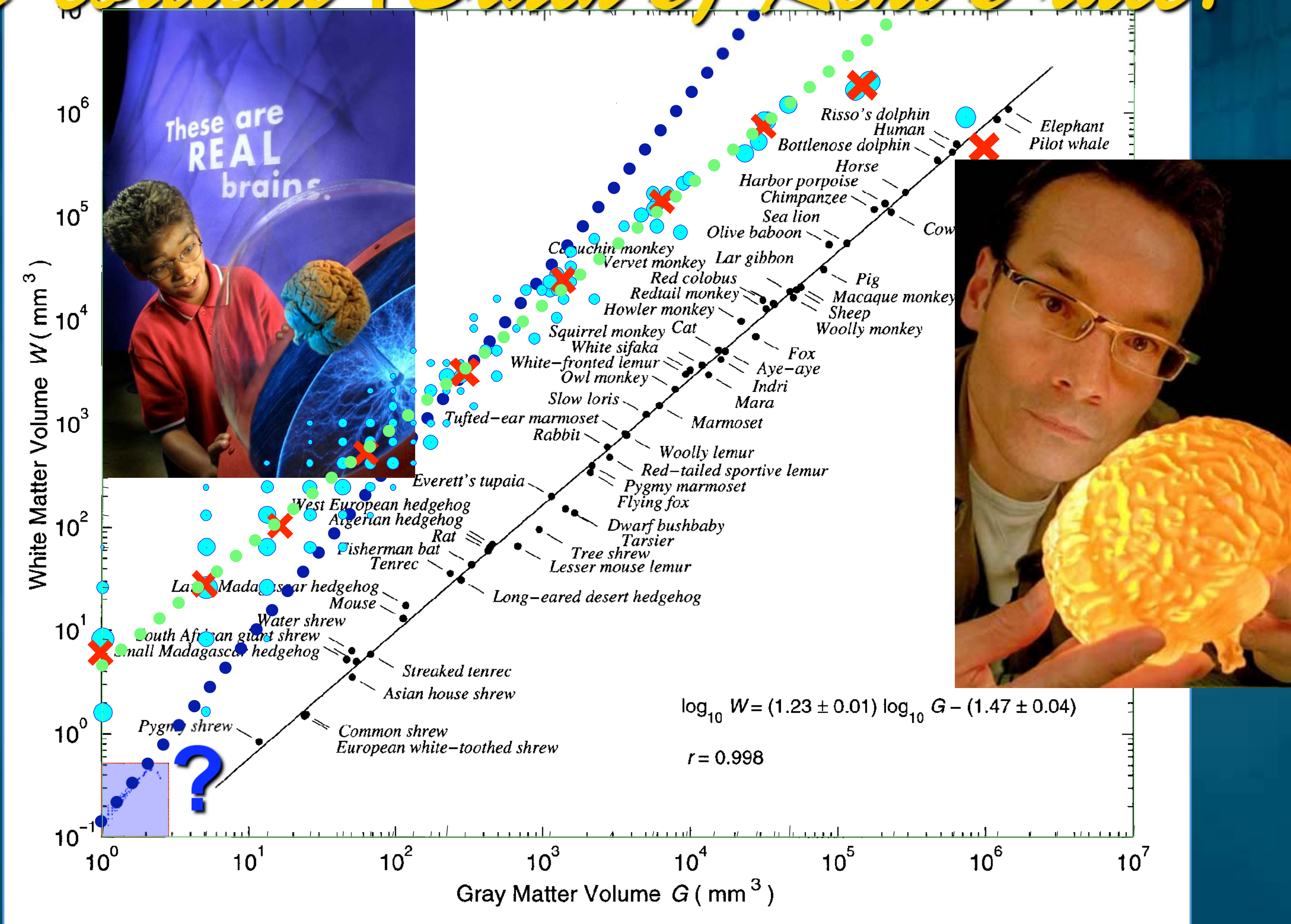
Adders (64 bit)
pf = 0.1, sub-V_{th}





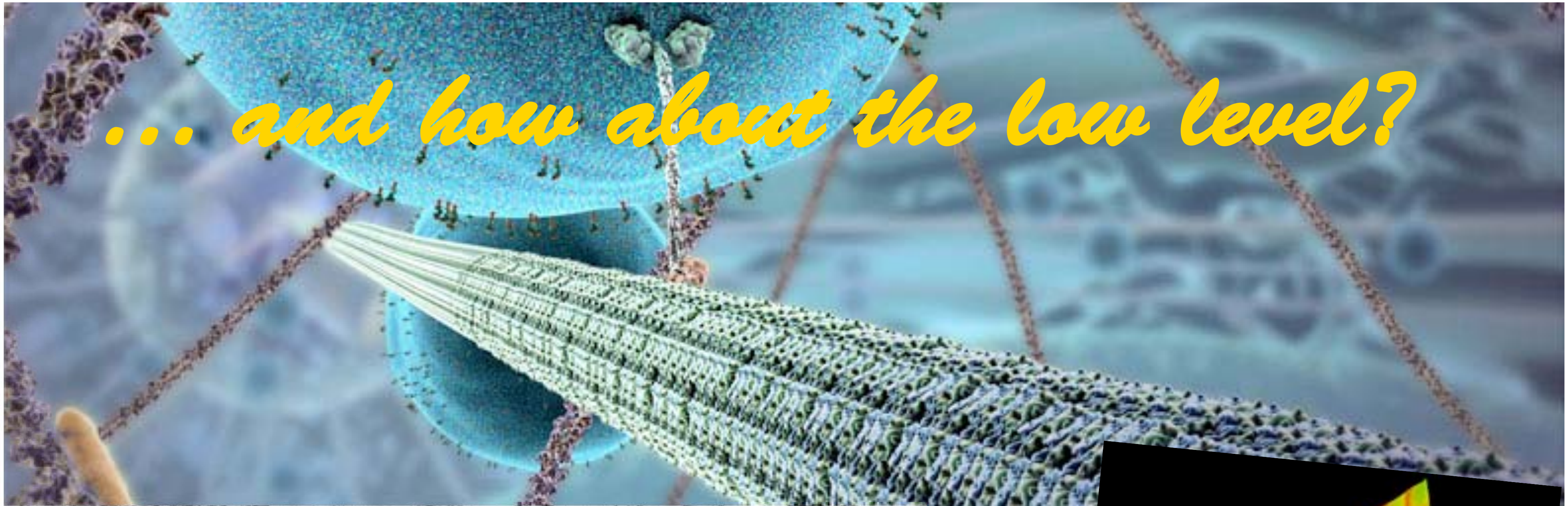
V. Beiu *et al.*, 2008

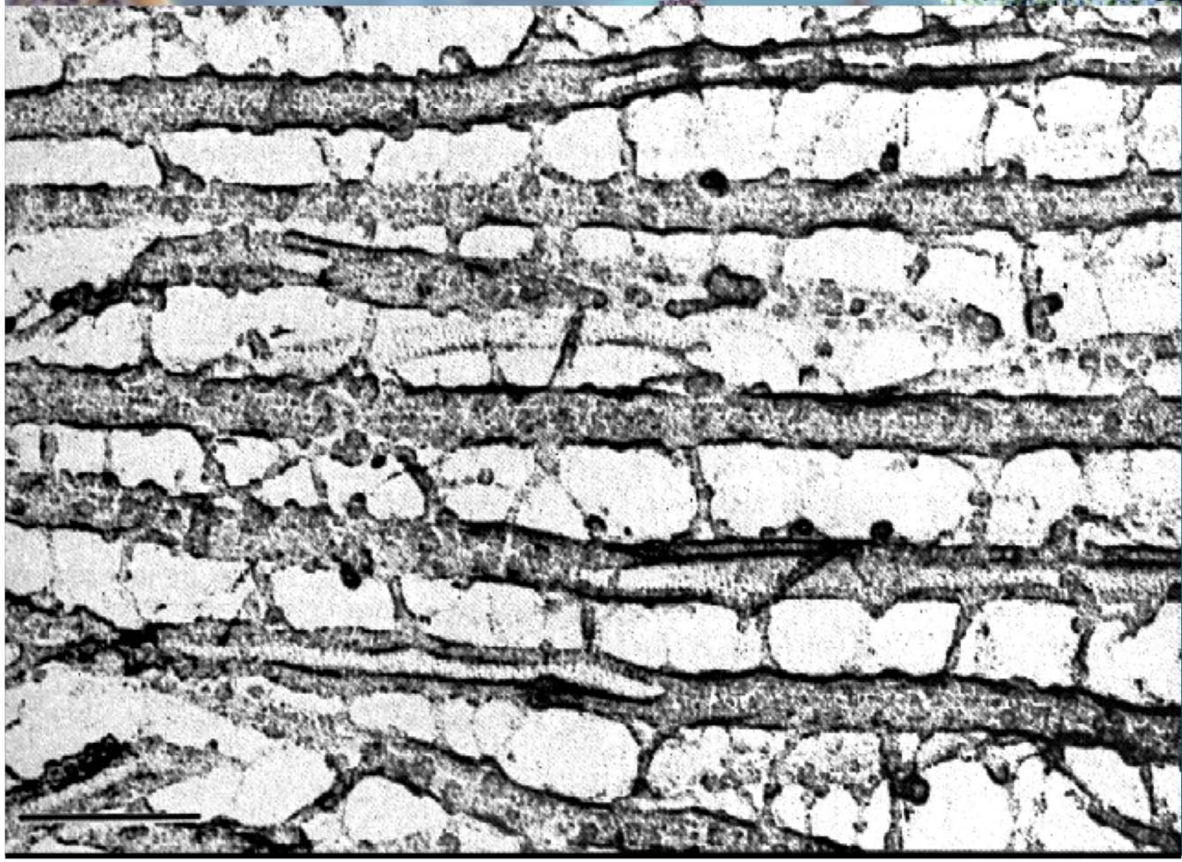
A cortical (Brain's) Rent's rule?

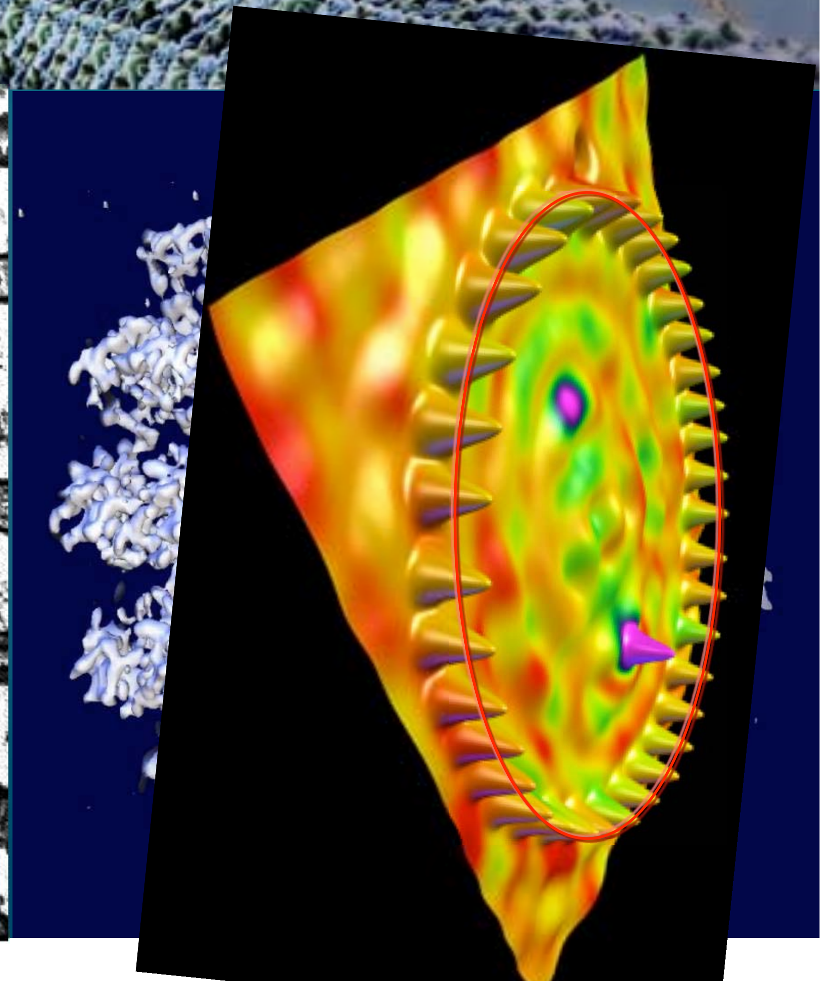


K. Zhang & T.J. Sejnowski, 2000

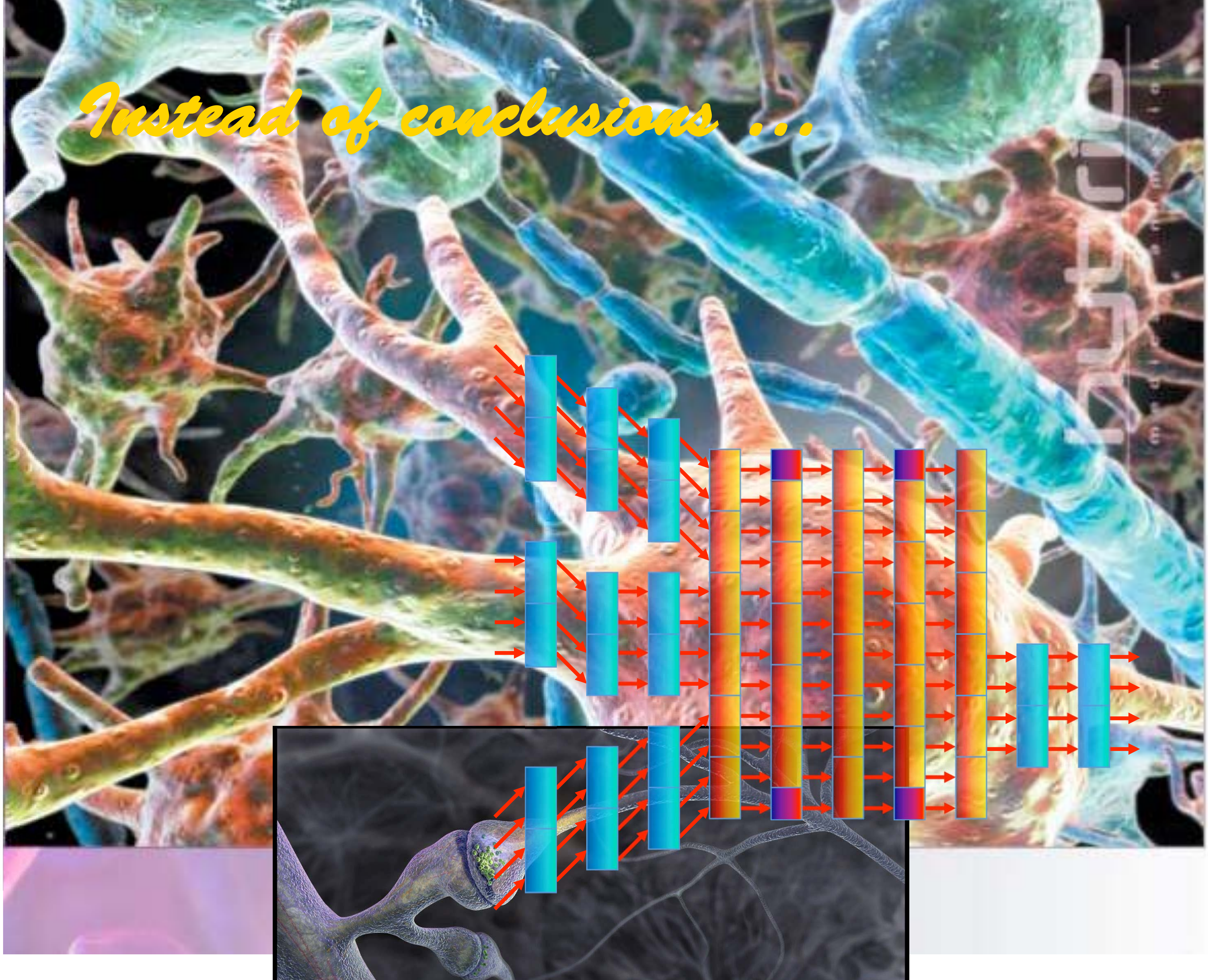
... and how about the low level?







Instead of conclusions ...

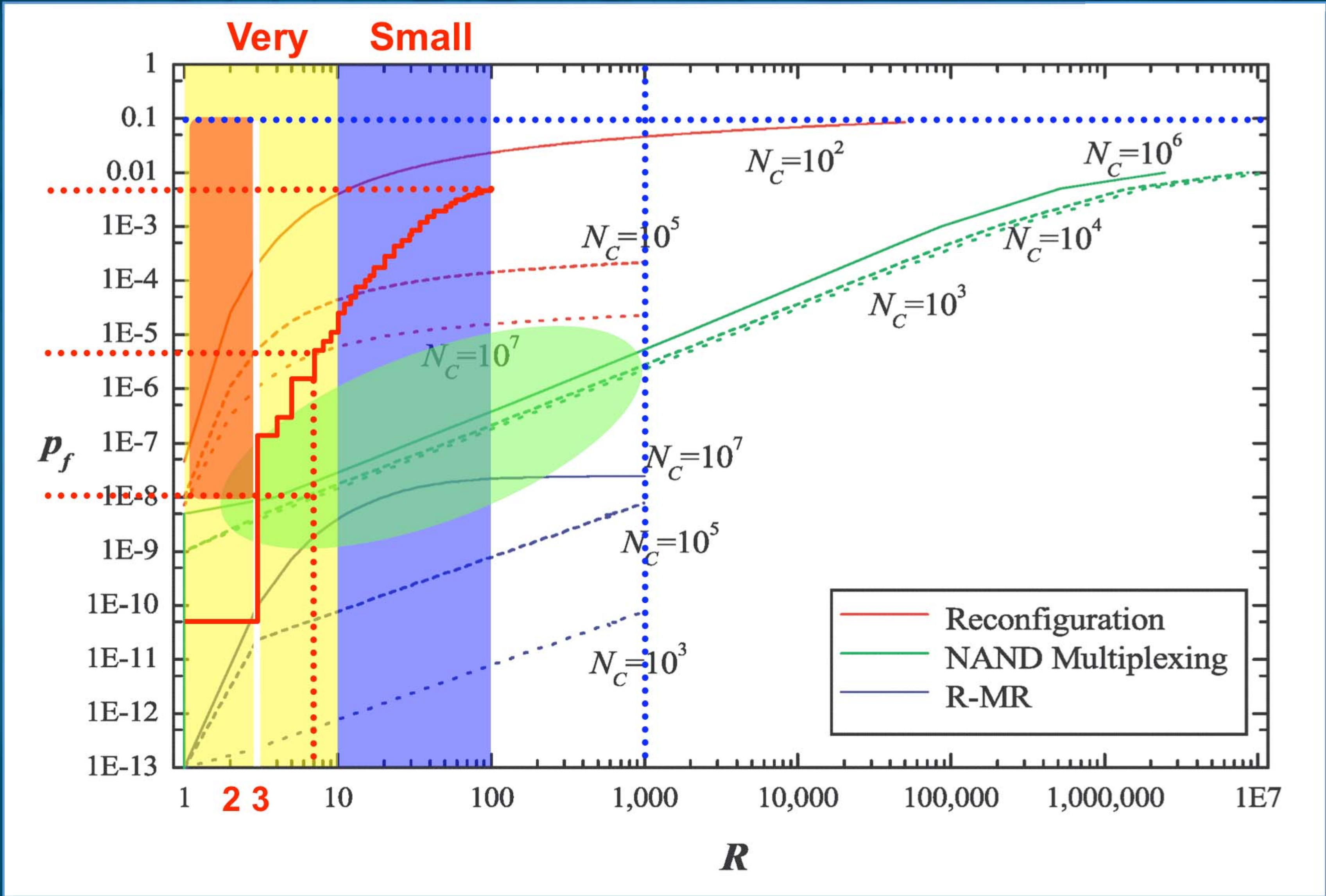


Smaller, more powerful chips allow me to have a smaller …

head !

THANK YOU

Comparison and evaluation



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Reliability …