

Dependable systems with nanometer scale technologies: what is different?

Jacob A. Abraham

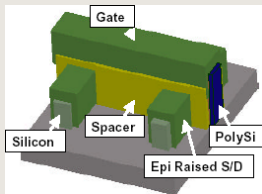
Panel

Third Workshop on Dependable and Secure
Nanocomputing (WDSN09)
Estoril, Portugal

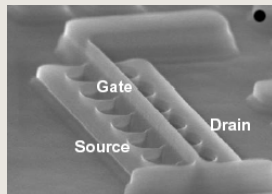
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What is new in technology?

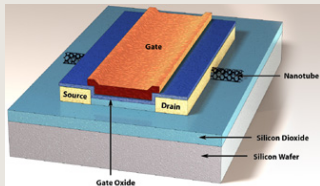
Exotic CMOS device – already here



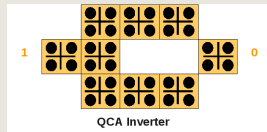
Finfet transistor



New nanotechnologies – in the future?



Carbon Nanotube transistor



Cellular Automata with Quantum Dots

Dealing with Faults

- Predict faults
- Detect errors concurrently with normal operation
- Correct errors and restore state
- Reconfigure system around permanent faults

What do we need to worry about?

- **Faults** (for prediction and off-line testing)
- **Errors** (mechanisms to deal with them during operation)

What about Design Faults and External Attacks?

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What about **Design Faults** and **External Attacks**?

Abstract effects of physical faults to a higher level

- Fault models
 - “Stuck-at”
 - Bridging
 - Delay
 - “Coupling” between memory cells
- Error models
 - Single-bit
 - Unidirectional

Possible surrogate for faults in nanometer-scale technologies

- **Delays in signals**

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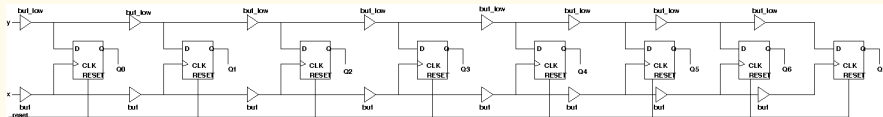
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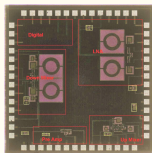
Low-Level Design to Support Dependable Operation

Need to reduce the possibility of too many errors propagating to the higher levels of the system

- Monitoring circuit behavior
- Calibration methods
- Compensation techniques
- **Reminiscent of Analog/RF design techniques!**



Vernier Delay Line for monitoring on-chip signal delay



On-chip detectors in RF chip (940 MHz GSM transceiver in 0.18μ technology)

Dealing with Design “Bugs”, External Attacks

Dealing with complexity

- A system with 300 state elements has more possible states than the number of protons in the universe!
- Guaranteeing that real systems have no bugs is effectively impossible
- Some directions
 - Exploit hierarchy in the design
 - Automated abstractions for verification

Dealing with malicious attacks

- Attacks are focused, and attacker must be assumed to know the design of the system
- Possible to extend control-flow checks for hardware faults to protect against attacks

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Low Levels of the System

- Understand the effects of faults in particular technologies
- Develop appropriate abstract fault and error models
- Develop integrated structures (sensors, monitors, calibration circuits) for supporting correct operation

Higher Levels of the System

- Develop new architectures which are synergistic with the particular technologies
 - Tessellation of regular blocks, for example
 - Necessity for local interconnections for some technologies
- Need to develop new techniques at the software and application levels to support dependable operation

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