Impact of Manufacturing Defects on Carbon Nanotube Logic Circuits

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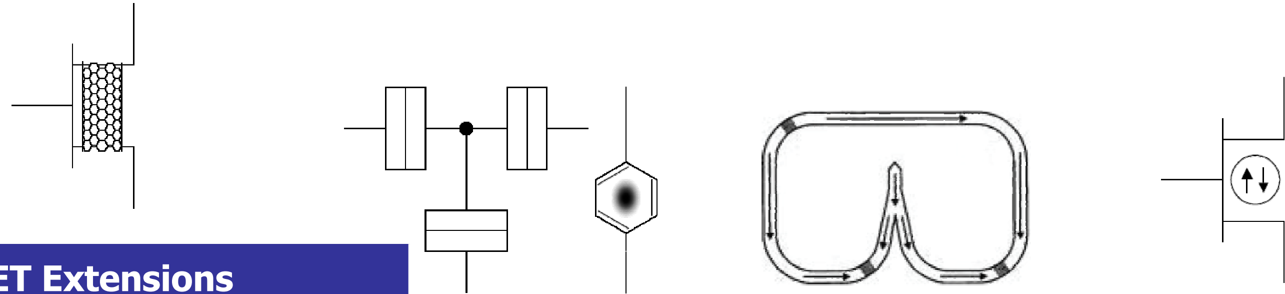
3rd Workshop on Dependable and Secure Nanocomputing

June 29 2009, Portugal

Fault-Tolerant Systems Group

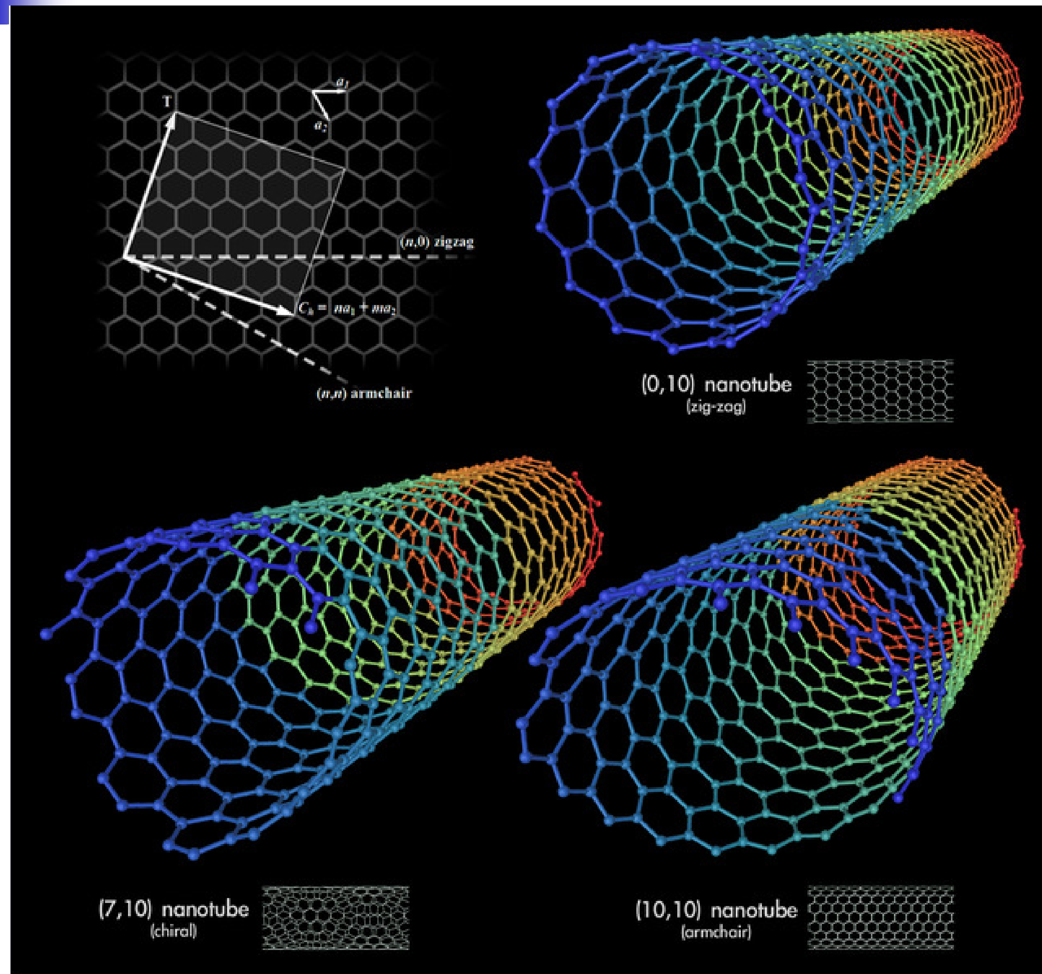
UNIVERSIDAD POLITECNICA VALENCIA

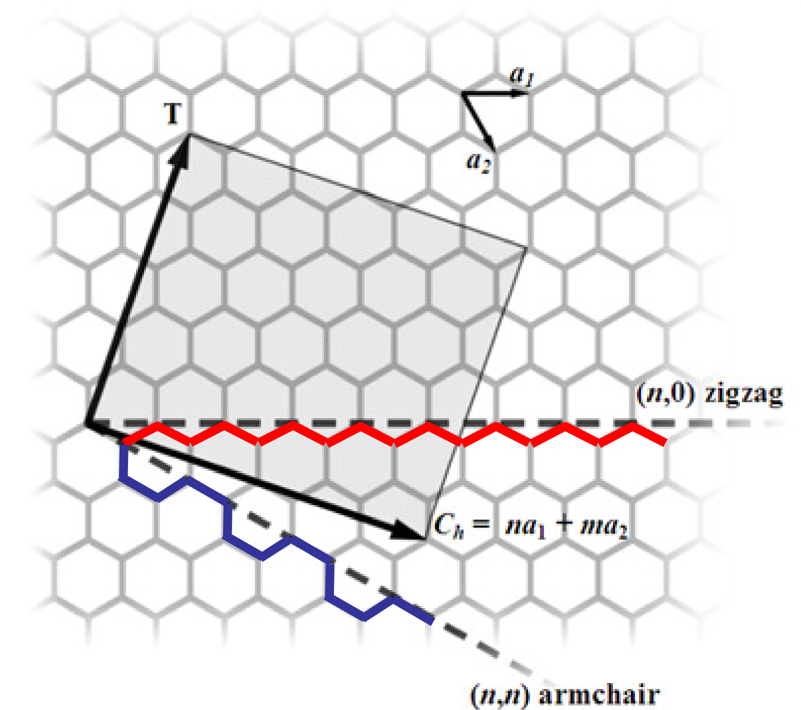
New technologies



	FET Extensions					
Device	**1D structures**	**Channel replacement**	**SET**	**Molecular**	**Ferromagnetic logic**	**Spin transistor**
Typical examples	CNT FET NW FET NW hetero-structures Nanorribon transistors with graphene	III-IV compound semiconductor and Ge channel replacement	SET	Crossbar latch Molecular transistor Molecular QCA	Moving domain wall M: QCA	Spin Gain transistor Spin FET Spin Torque transistor
Research activity	379	62	91	244	32	122

CNTs: Structure





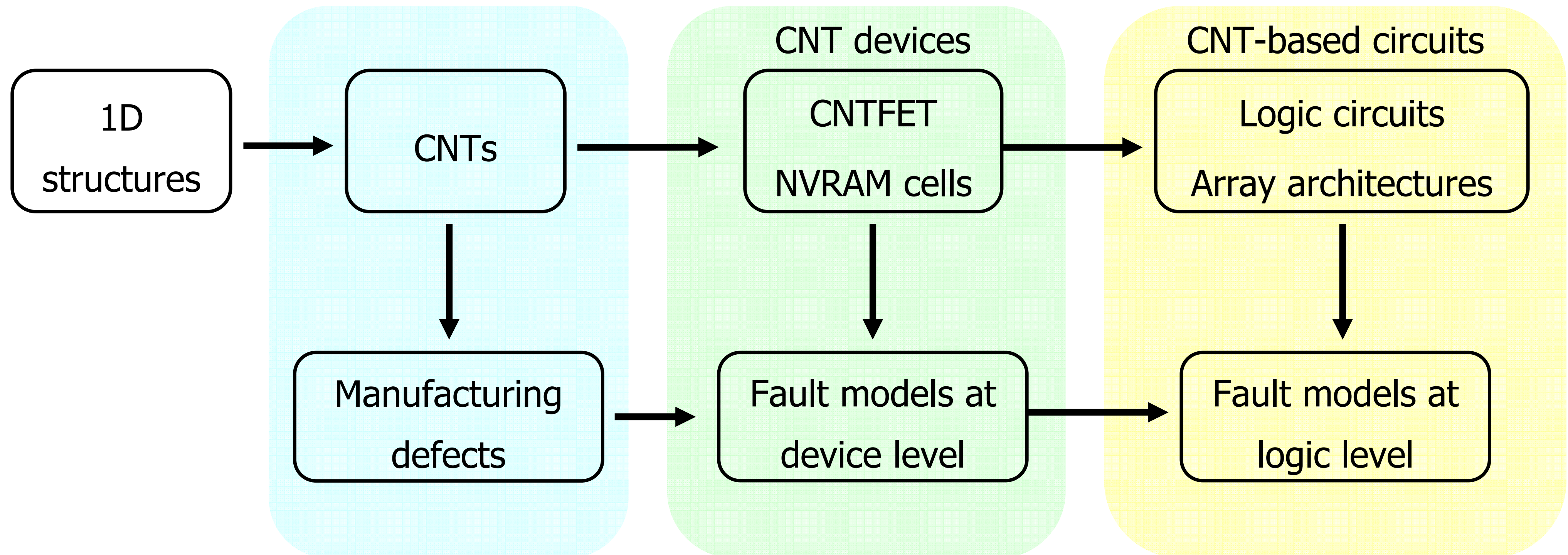
$$d = \frac{|C_h|}{\pi} = \frac{\sqrt{3}}{2\pi} b\sqrt{n^2 + nm + m^2}$$

$$E_g \propto \frac{1}{d}\ eV$$

CNTs: Properties & challenges

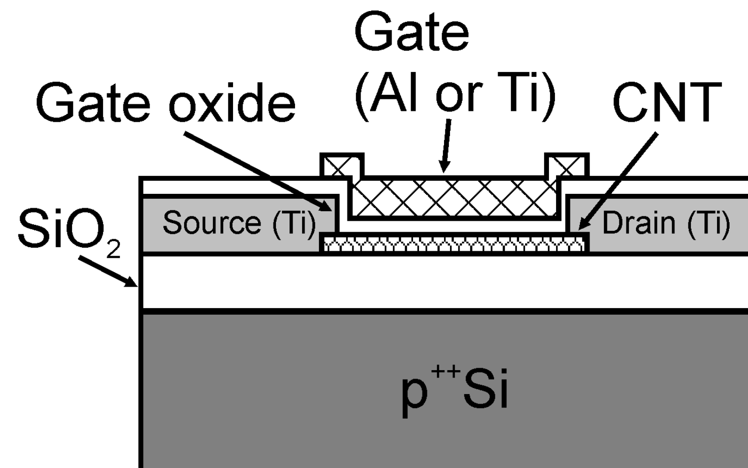
- Properties:
  - Mechanical properties: strength, thermal conductivity
  - Electrical: ballistic transport, excellent conduction properties
  - Size: diameter ~ few nm, length up to several mm
- Challenges of manufacturing at large scale
  - Control of electrical properties (semic. /metallic)
  - Alignment and placement
  - Electrical contact between CNTs and electrodes

Analysis from a dependability viewpoint



Electronic devices with CNTs

- Electric wires → excellent conductors
- CNT-FET → size, gate control, speed



- CNT-based RAMs

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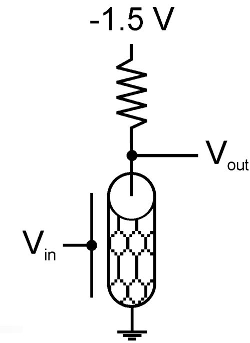
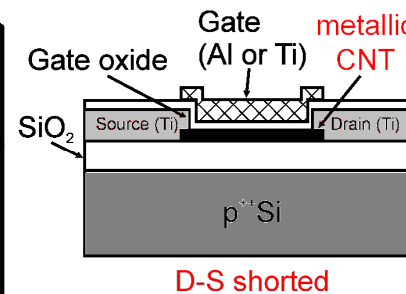
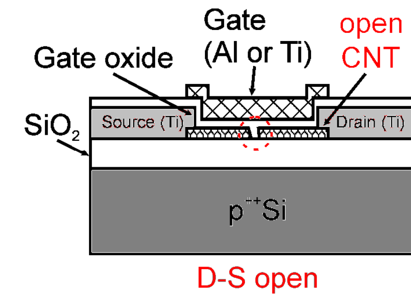
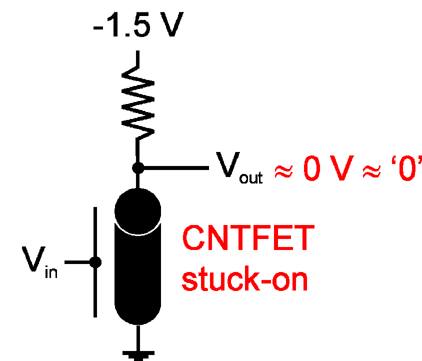
Fault models at logic level
Example: NOT gate

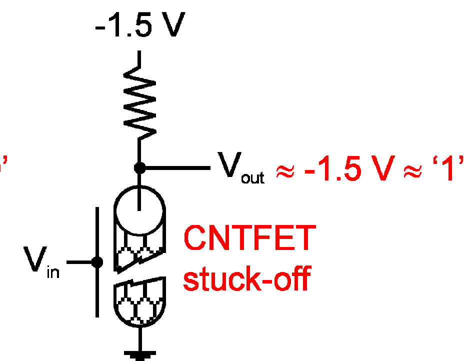


Manufacturing defect	Metallic CNT	Open CNT
Causes and mechanisms	Bad chirality/diameter control	Mechanical stress, bending
Effects on CNT FETs	**Resistive D-S short** Excessive leakage Degraded noise margins Delay variations	D-S open
Fault model at device level	Stuck-on	Stuck-off
Fault model at logic level	Stuck-at-0	Stuck-at-1

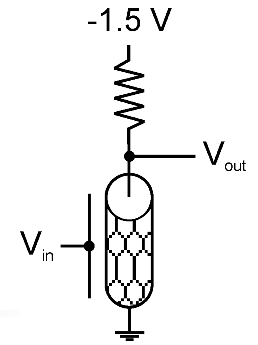




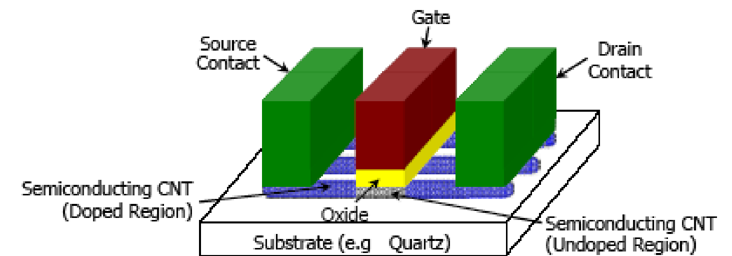


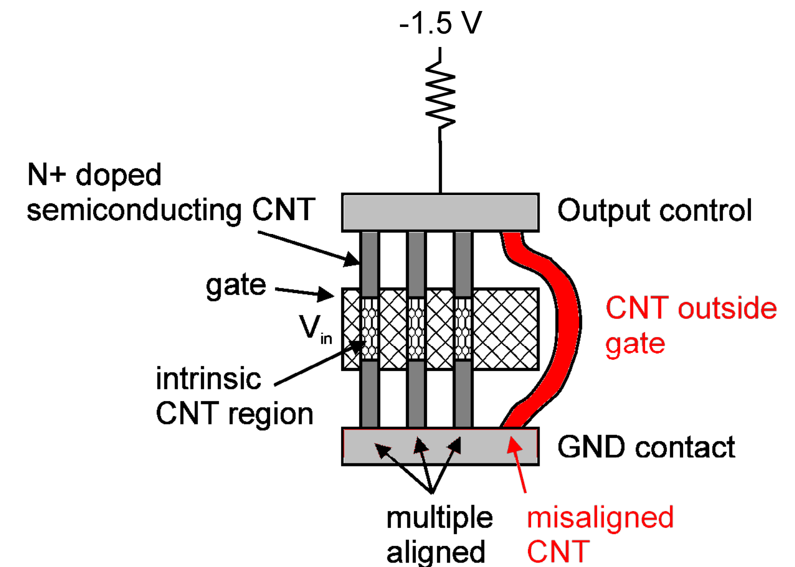


Fault models at logic level Example: NOT gate



Manufacturing defect	Misaligned / Miss-positioned
Causes and mechanisms	CNT under incorrect gate **CNT outside gate**
Effects on CNT FETs	D-S open, connection with other transistors **D-S short**
Fault model at device level	Stuck-on
Fault model at logic level	Stuck-at-0





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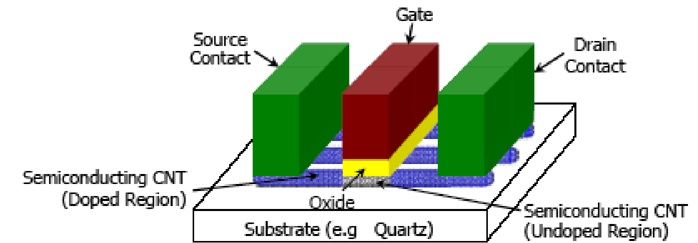
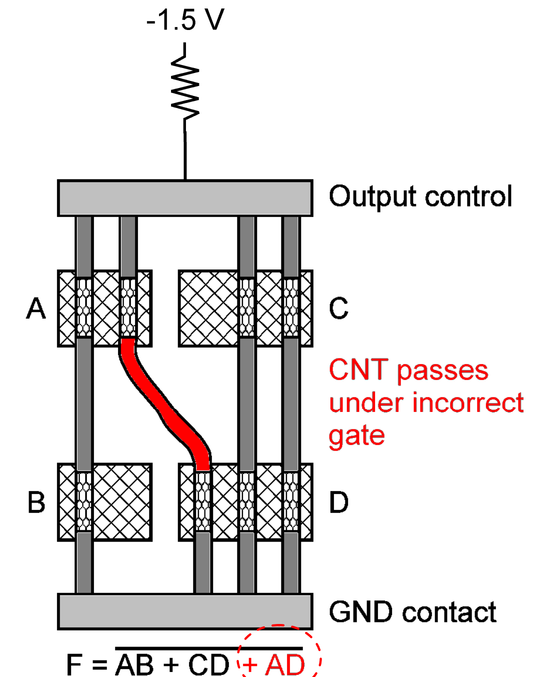
Fault models at logic level
Example: AND-OR-INVERTED gate

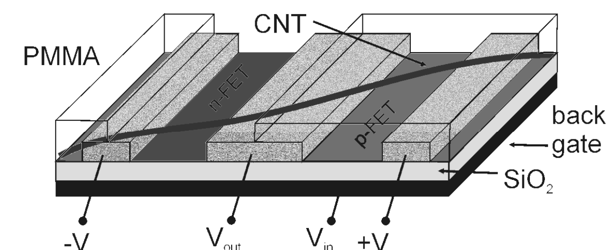
Manufacturing defect	Misaligned / Miss-positioned
Causes and mechanisms	**CNT under incorrect gate** CNT outside gate
Effects on CNT FETs	D-S open, **connection with other transistors** D-S short
Fault model at device level	CNT under incorrect gate
Fault model at logic level	Change of logic function

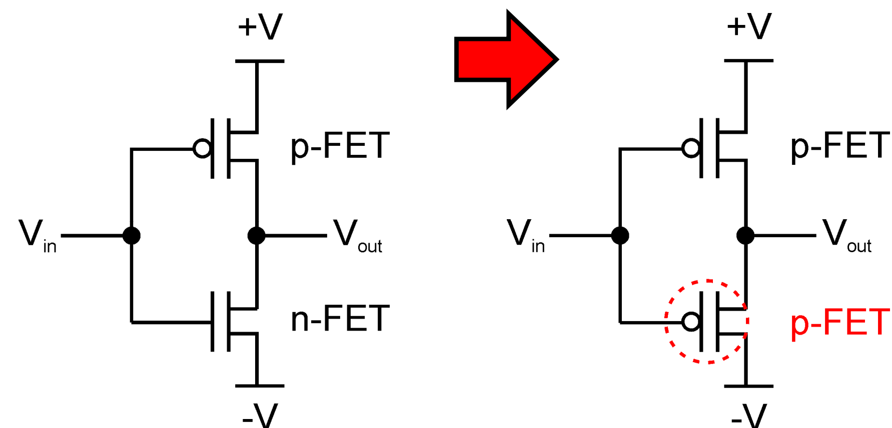




Fault models at logic level
Example: Intramolecular NOT gate

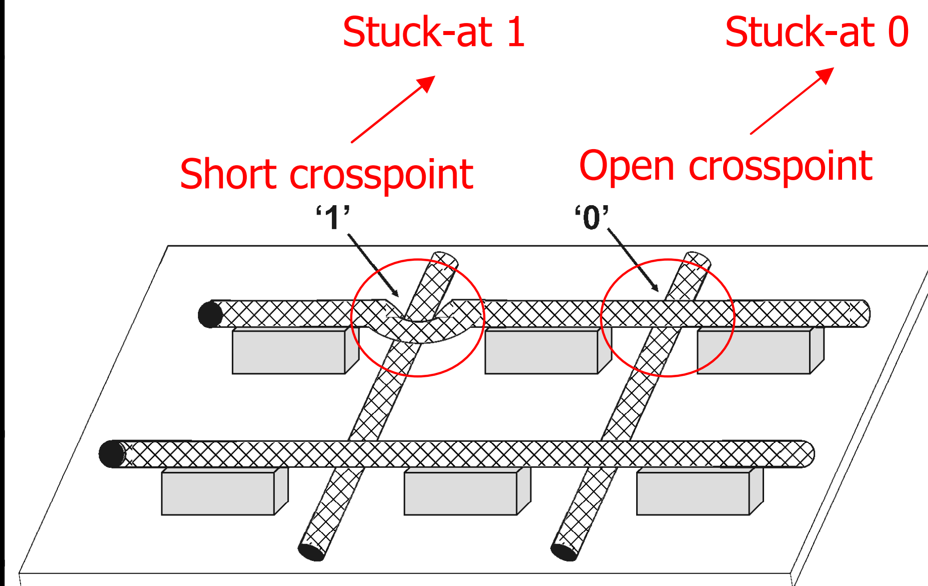
Manufacturing defect	Erroneous doping
Causes and mechanisms	Misaligned PMMA mask
Effects on CNT FETs	Channel cannot be N-doped
Fault model at device level	2 P-CNTFET
Fault model at logic level	Incorrect logic behaviour





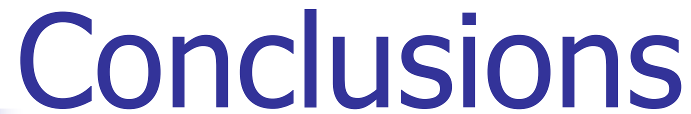
Fault models at logic level Example: NVRAM

Manufacturing defect	Open	Short
Causes and mechanisms	Imperfect contact	Imperfect separation
Effects on CNT FETs	Non-programmable crosspoint	Shorted crosspoint
Fault model at device level	Non-programmable	Shorted
Fault model at logic level	Stuck-at-0	Stuck-at-1



Manufacturing defects and fault models

Defect		Causes and mechanisms	Effects on CNT FET	Fault Models at CNT FET level	Fault Models at logic level
CNT defects	Metallic	Bad chirality control Bad diameter control	Resistive D-S short Excessive leakage Degraded noise margins Delay variations	Stuck-on Delay	Stuck-at (0,1), indetermination Delay
	Misaligned / Miss-positioned	CNT under incorrect gate CNT outside gate	D-S open, connection with other transistors D-S short	Stuck-off Stuck-on	Stuck-at (0,1) Change of logic function Loss of memory behaviour
	Open	Mechanical stress, bending	D-S open	Stuck-off	Stuck-at (0,1) High-impedance Loss of memory behaviour
	Poor contacts Crystallographic defects	Defect CNT-metal contacts Atomic vacancies	Increase of the channel resistance	Delay	Delay
	Parametric variation	Diameter, length, gate oxide thickness	Threshold voltage (V_T) variation Channel resistance variation	Delay	Delay
	Erroneous doping	PMMA mask misalignment	Channel cannot be N-doped	N-type → P-type	Incorrect logic behaviour
Crosspoint defects	Open	Imperfect contact	Non-programmable crosspoint	Non-programmable	Stuck-at 0
	Short	Imperfect separation	Shorted crosspoint	Shorted	Stuck-at 1



Conclusions

- **Manufacturing defects**
  - Similar to SiNWs: Open, poor contacts, erroneous doping, and open/short crosspoints
  - More specific, frequent and troublesome: Conducting (metallic), misaligned/miss-positioned, and parametric variation of the CNTFET channel
- **Fault models at transistor level**
  - Structural similarity to MOSFET transistors, Electronic charge-based devices → Well-known stuck-on, stuck-off and delay
- **Fault models at logic level**
  - CNT-based logic circuits present NMOS- or CMOS-like structures → Traditional stuck-at (0/1), delay, high-impedance and indetermination:
  - Some unusual fault models: Change of logic function, Inverter with 2 P-CNTFETs, Loss of memory behaviour in SRAM cells

Any question?

Thank you for paying attention!

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