

# ON CMOS CIRCUIT RELIABILITY

FROM

THE  
MOSFETS  
AND THE  
INPUT VECTORS



# Structure of the presentation

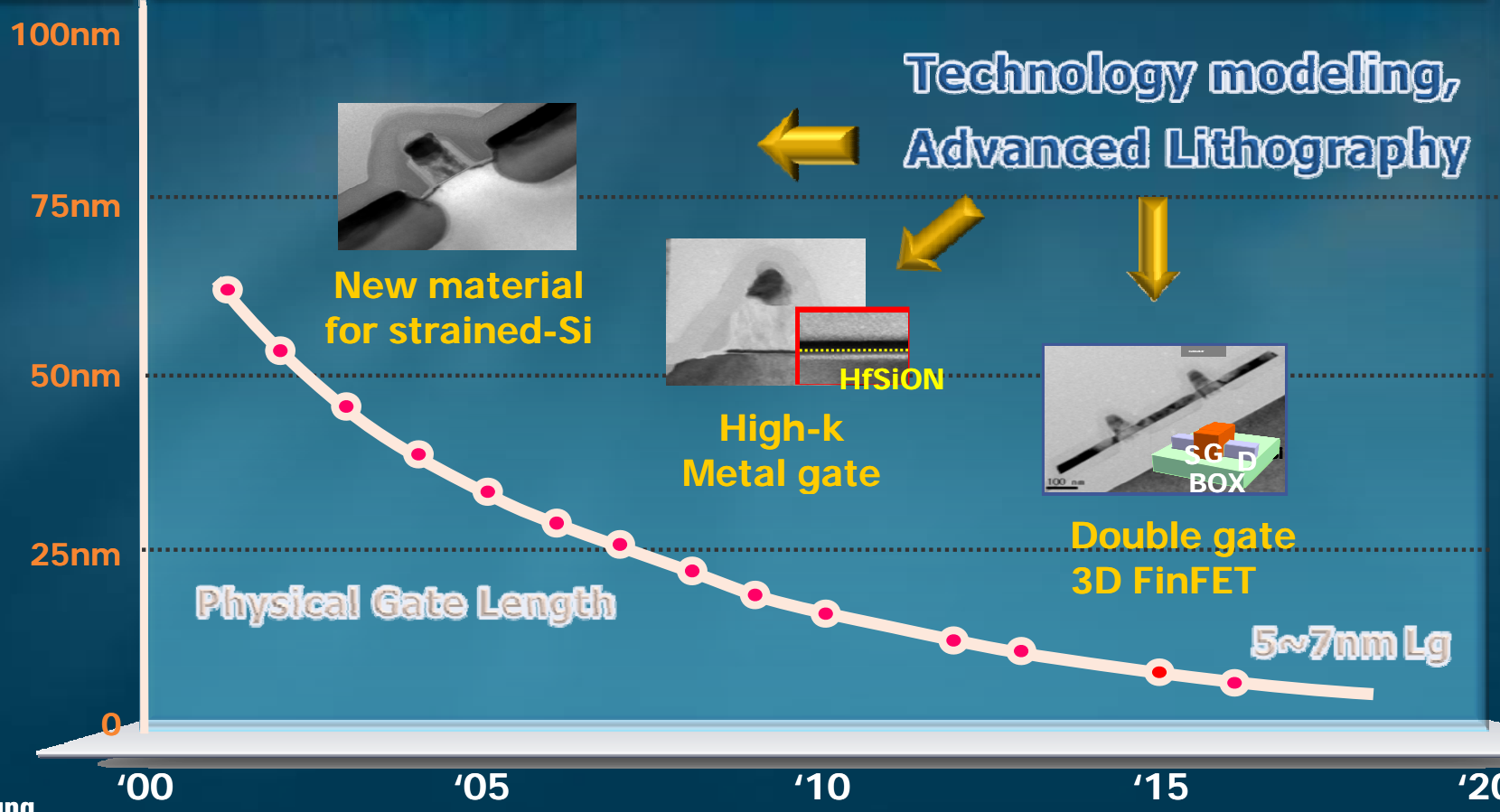
- ◆ **Classical view**
- ◆ **Ubiquitous ... variations**
  - ❖ **Thermal**
  - ❖ **Leakage**
  - ❖ **Vdd**
  - ❖ **Fabrication ...**
- ◆ **Detailed (atomistic) view**
- ◆ **Vth variations**
- ◆ **Gate-level simulations**
- ◆ **Conclusions**



# Classical view

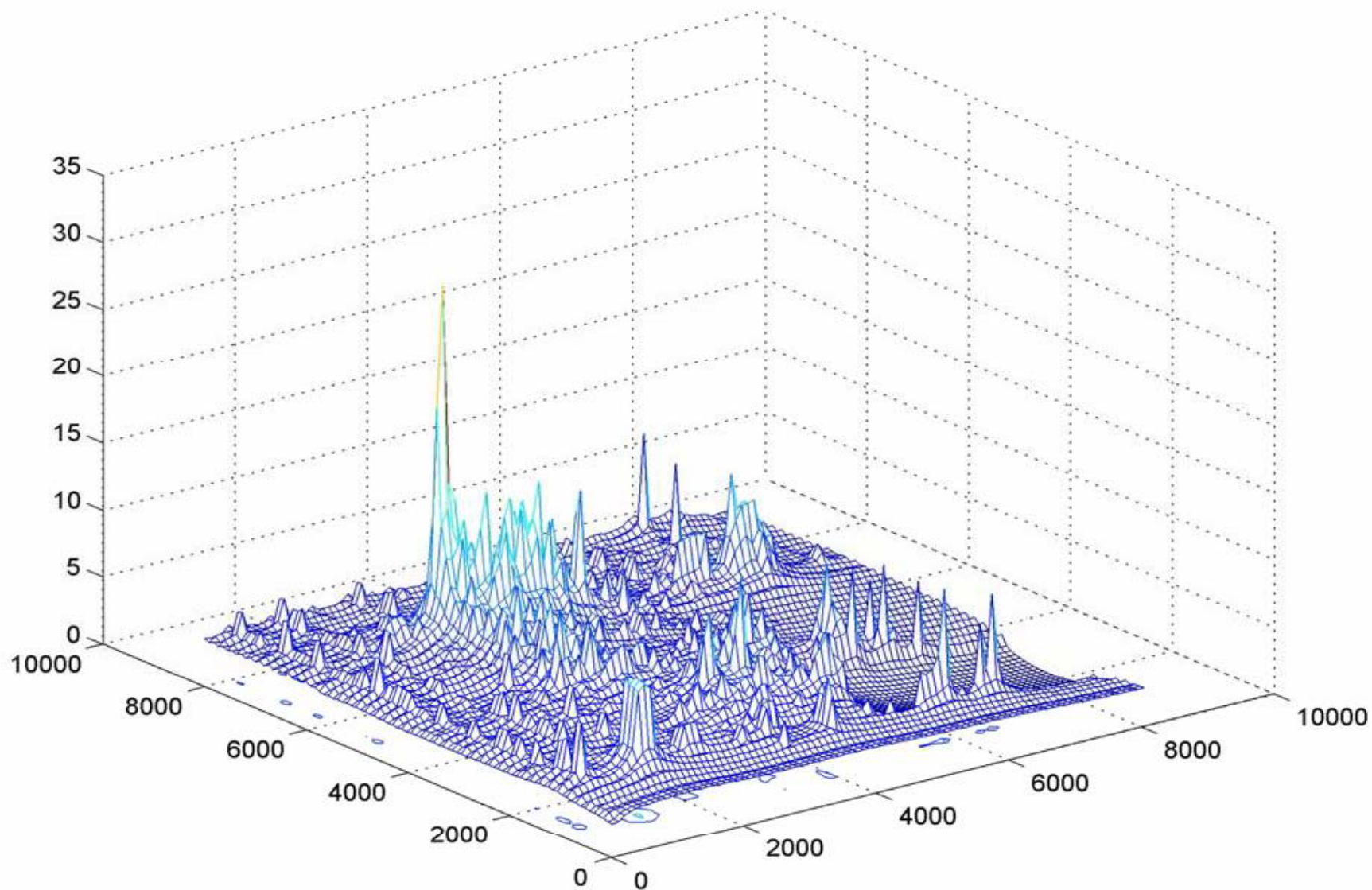
- Nano-scale requires new materials and device structures
- New EDA solutions are needed for technology modeling and advanced lithography

DRAM ½ pitch	90	65	45	32	22	
Logic Generation	130	90	65	32	22	16

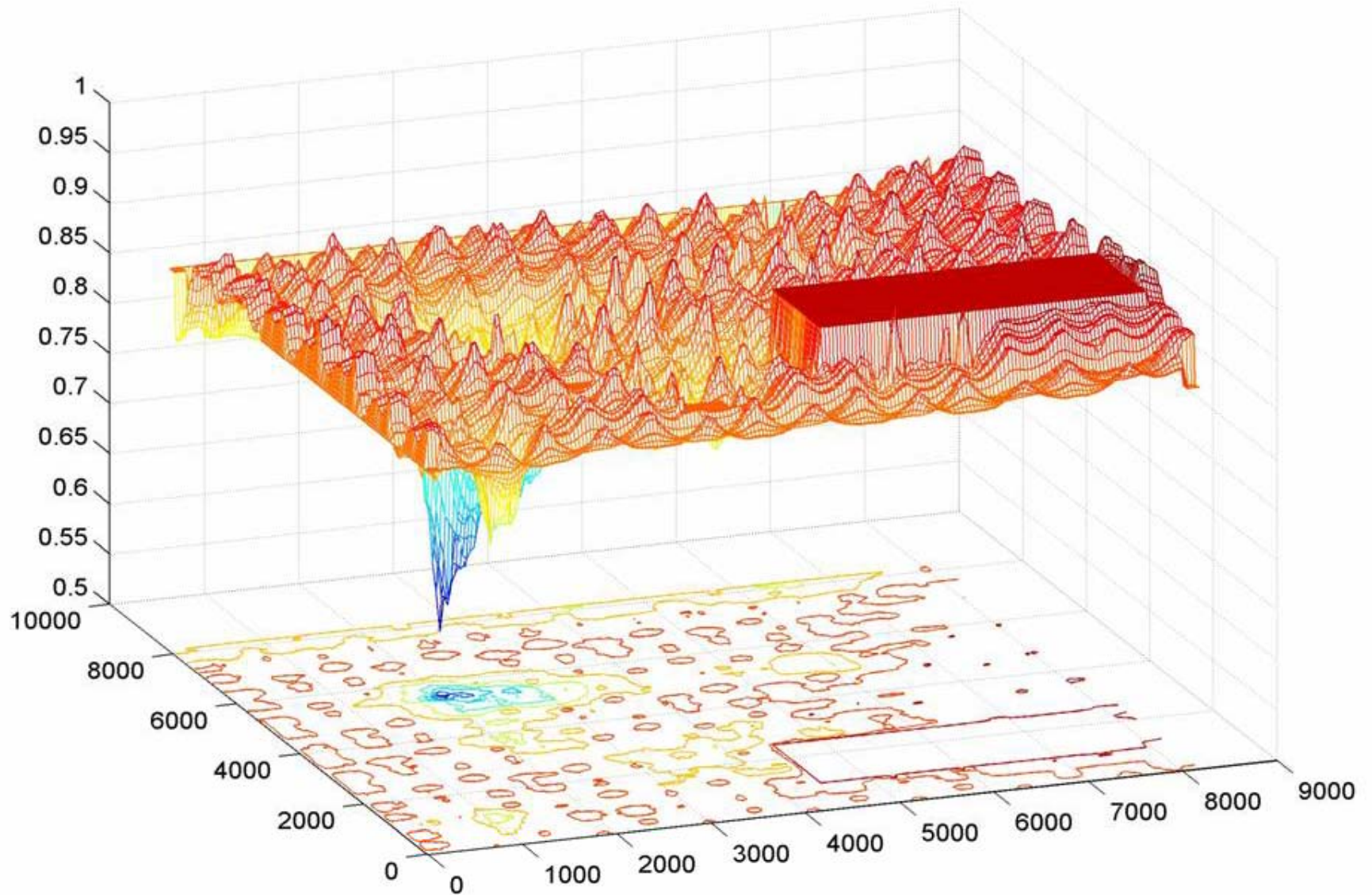


From Samsung

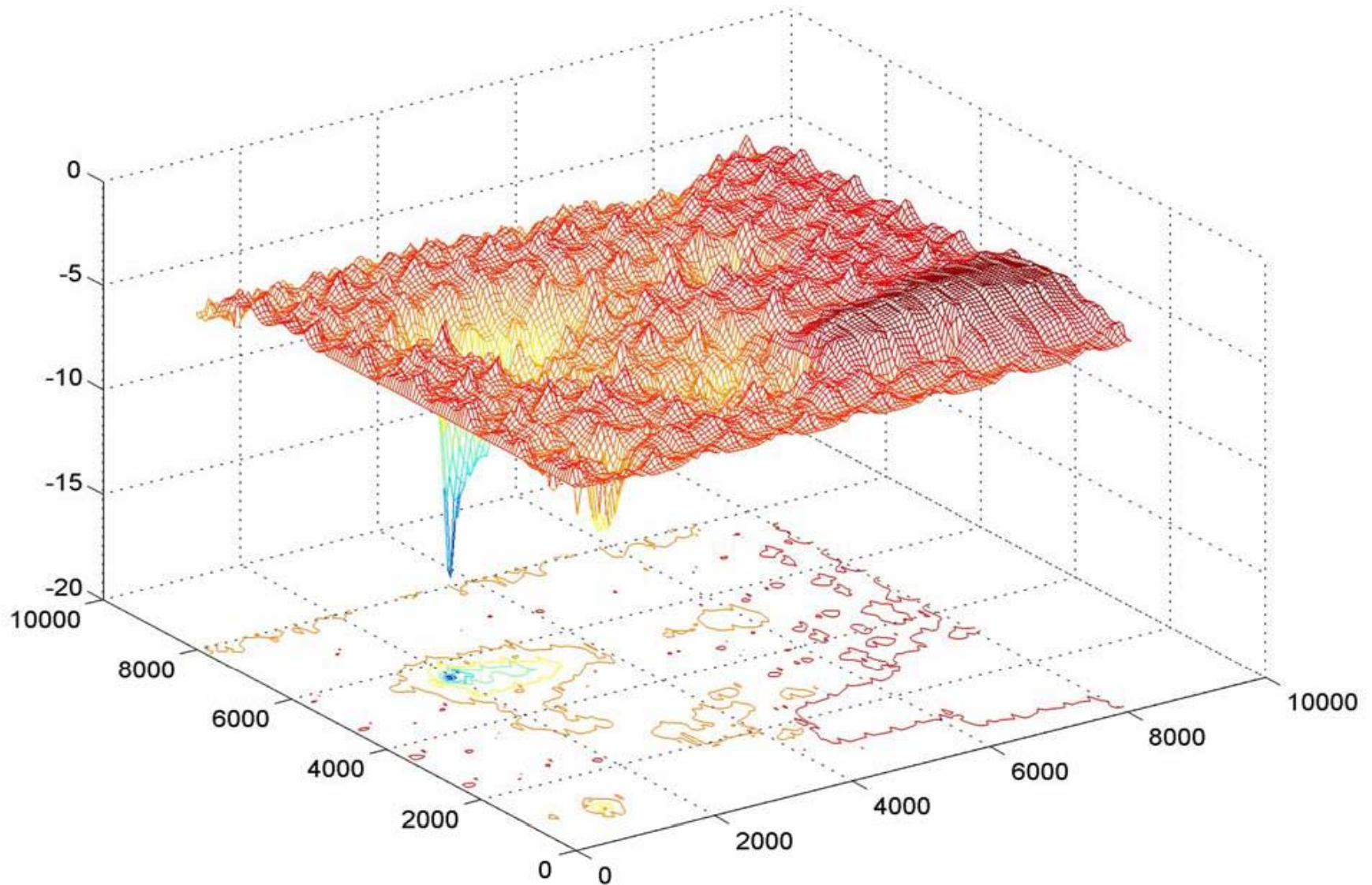
# Variations ... thermal



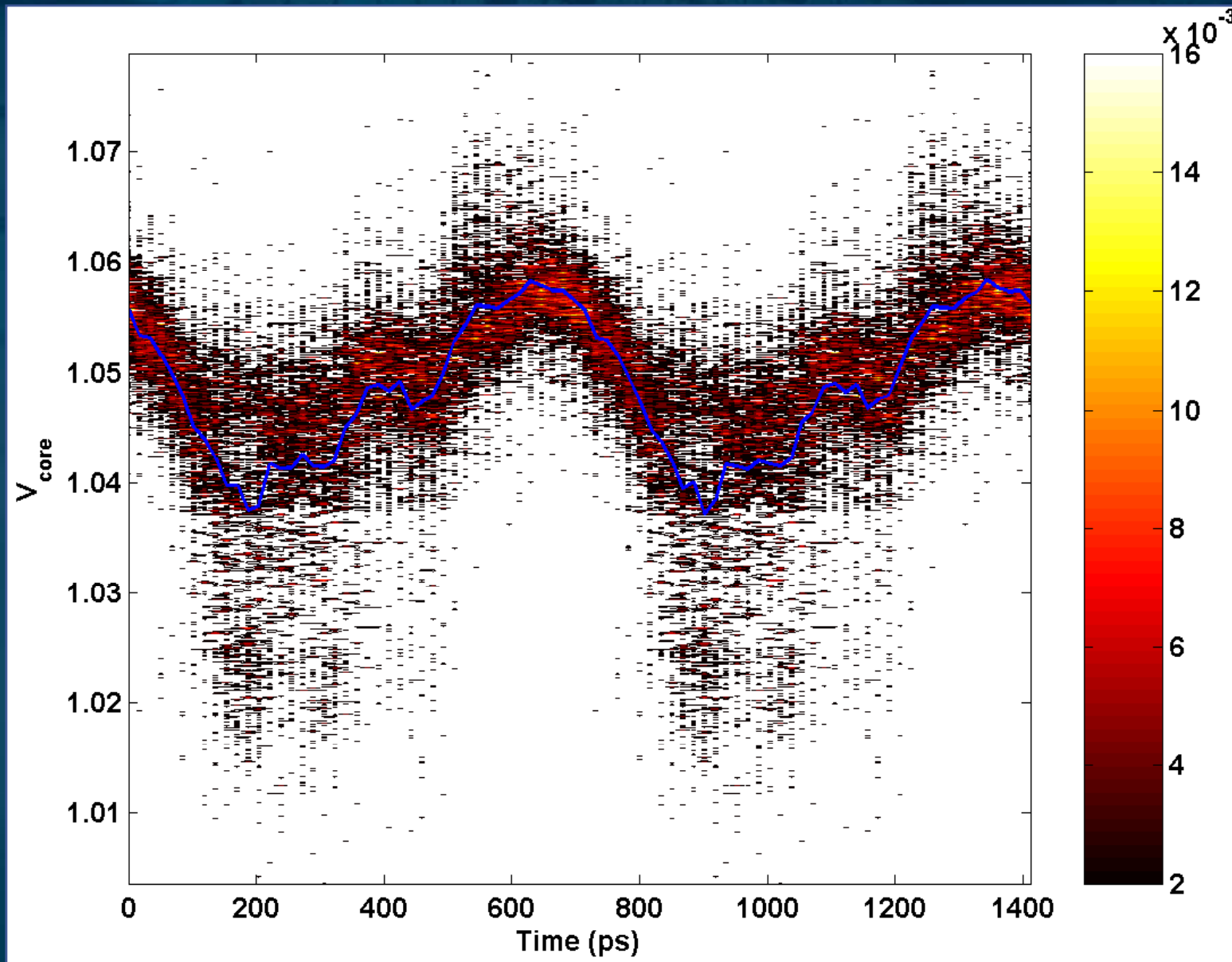
# Variations ... Leakage



# Variations ... $\tau_{dd}$

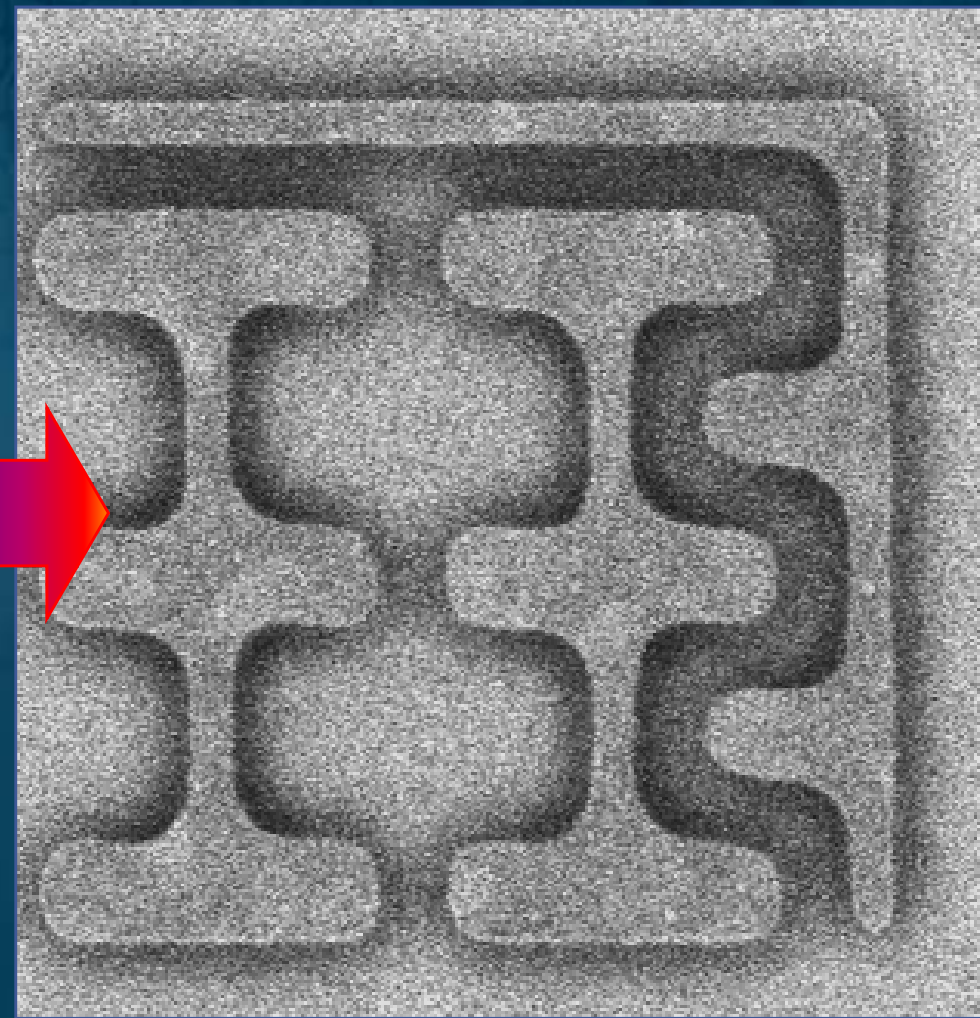
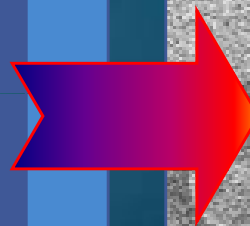
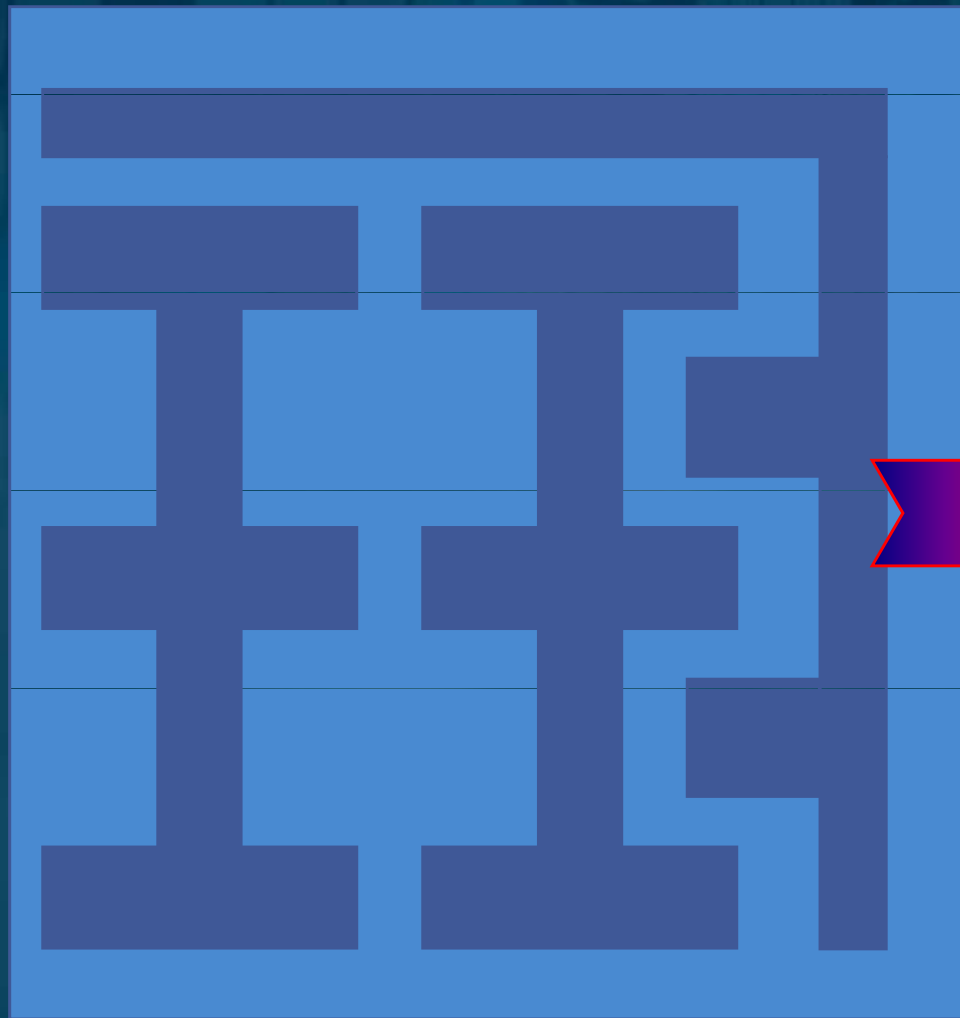


# Odd noise (Itanium, 90nm)



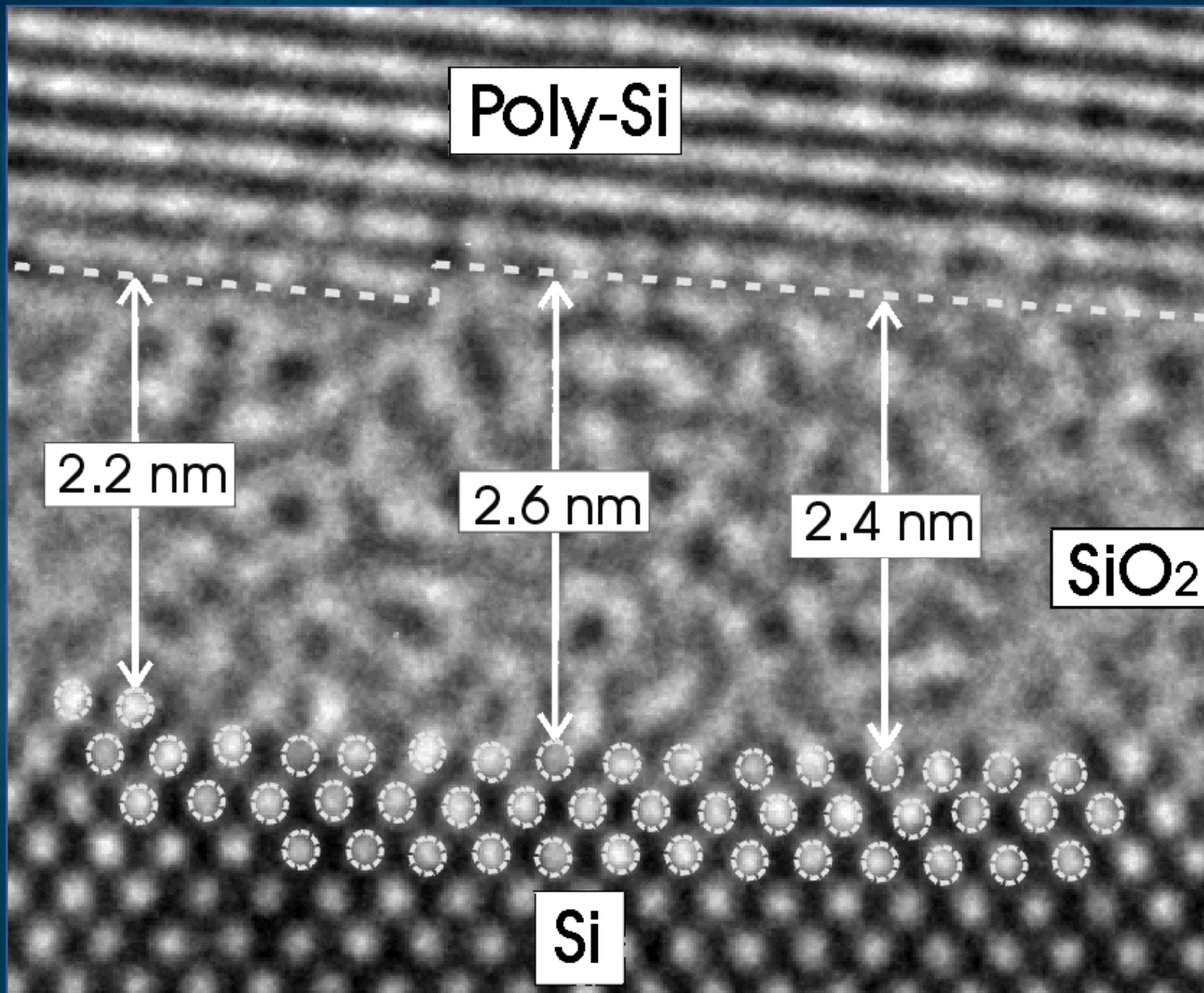
S. Naffziger, B. Stackhouse, T. Grutkowski, D. Josephson, J. Desai, E. Alon, and M. Horowitz  
The Implementation of a 2-Core, Multi-Threaded Itanium Family Processor, *J. Solid-State Circ.*, Jan. 2006

# Variations ... when fabricating

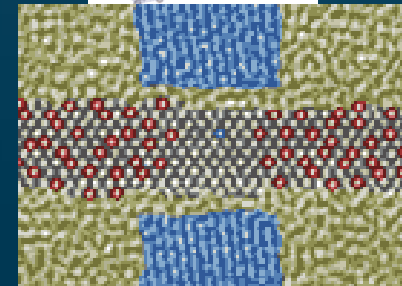
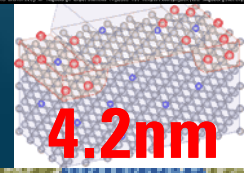
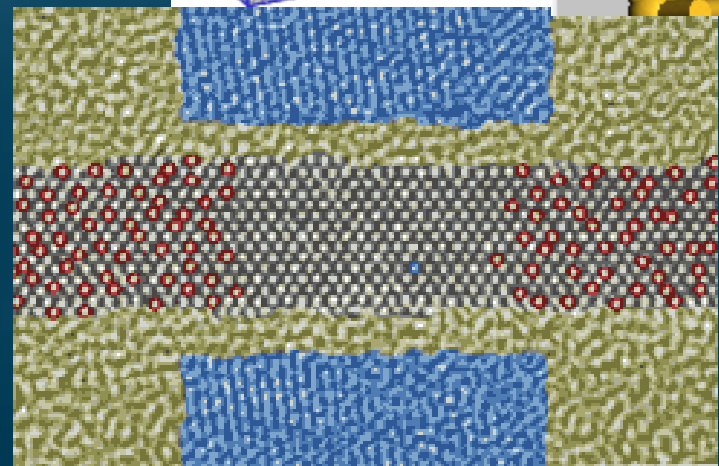
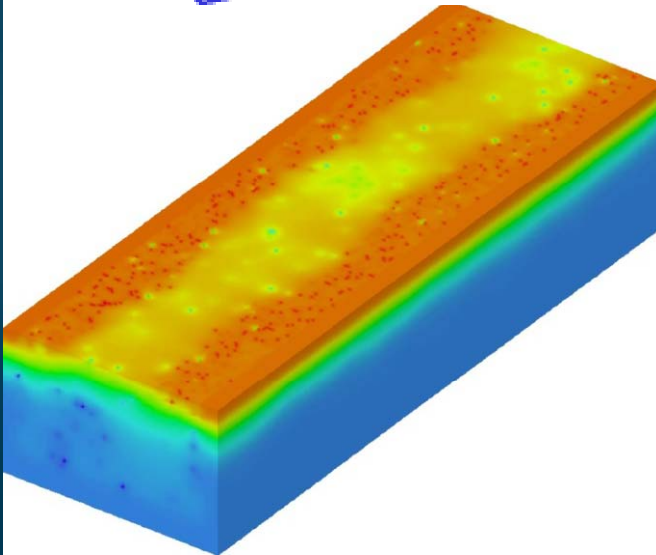
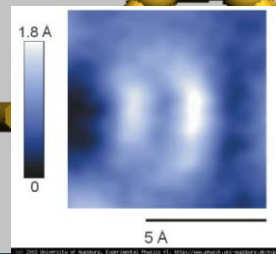
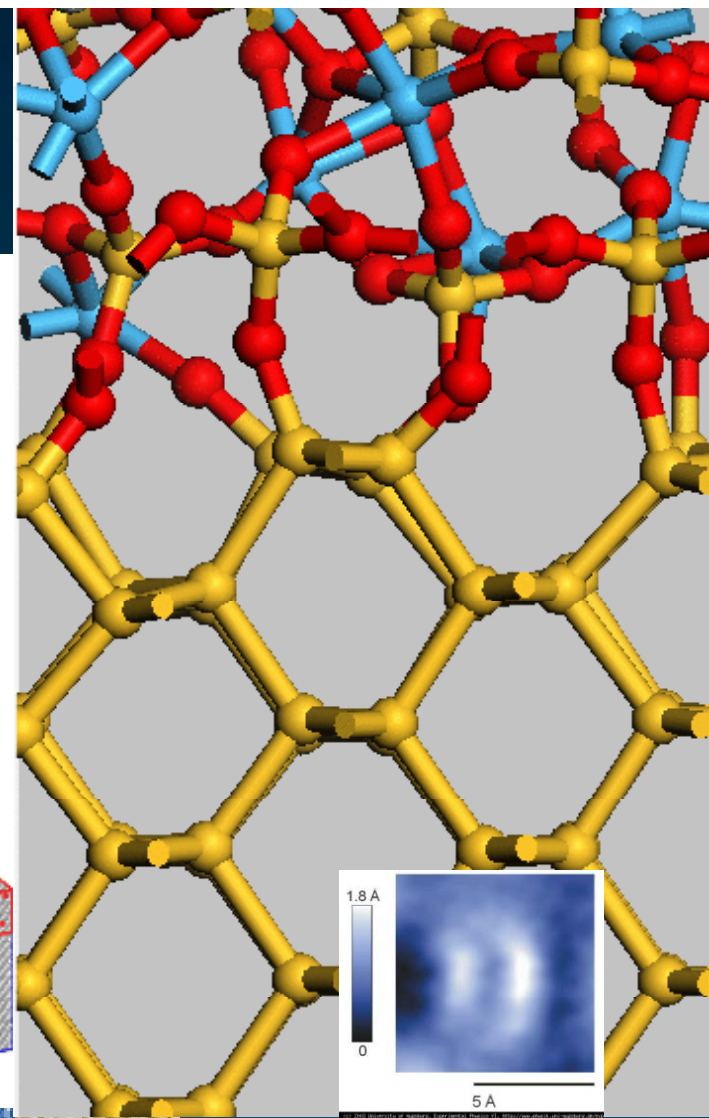
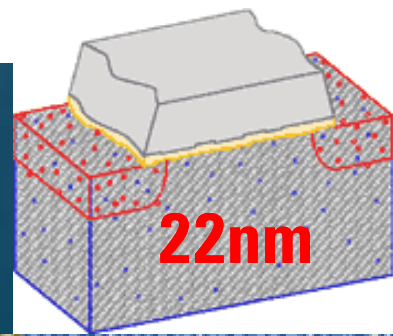
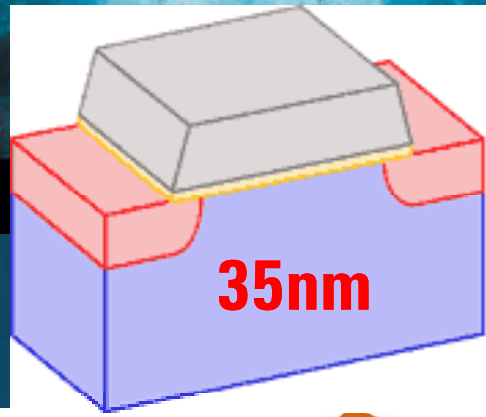
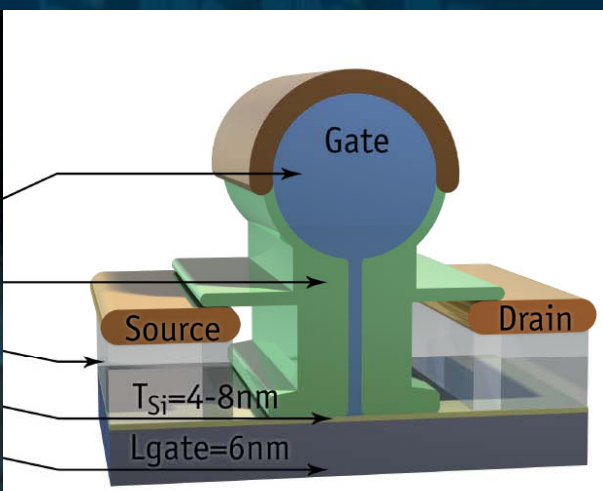
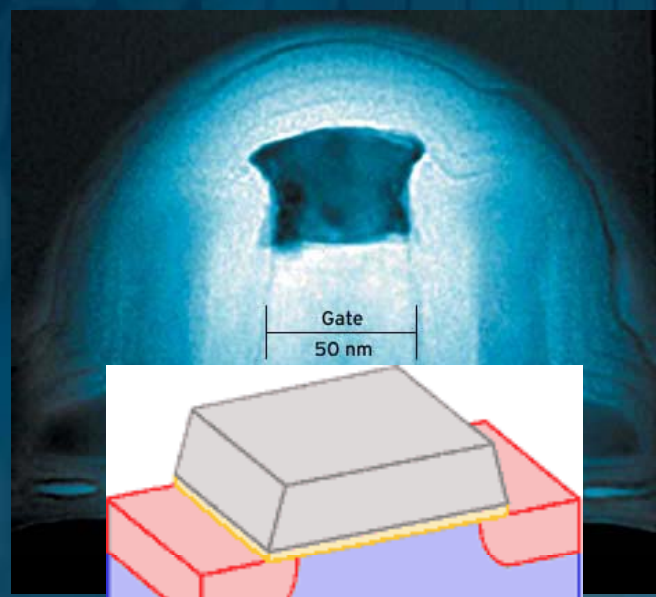




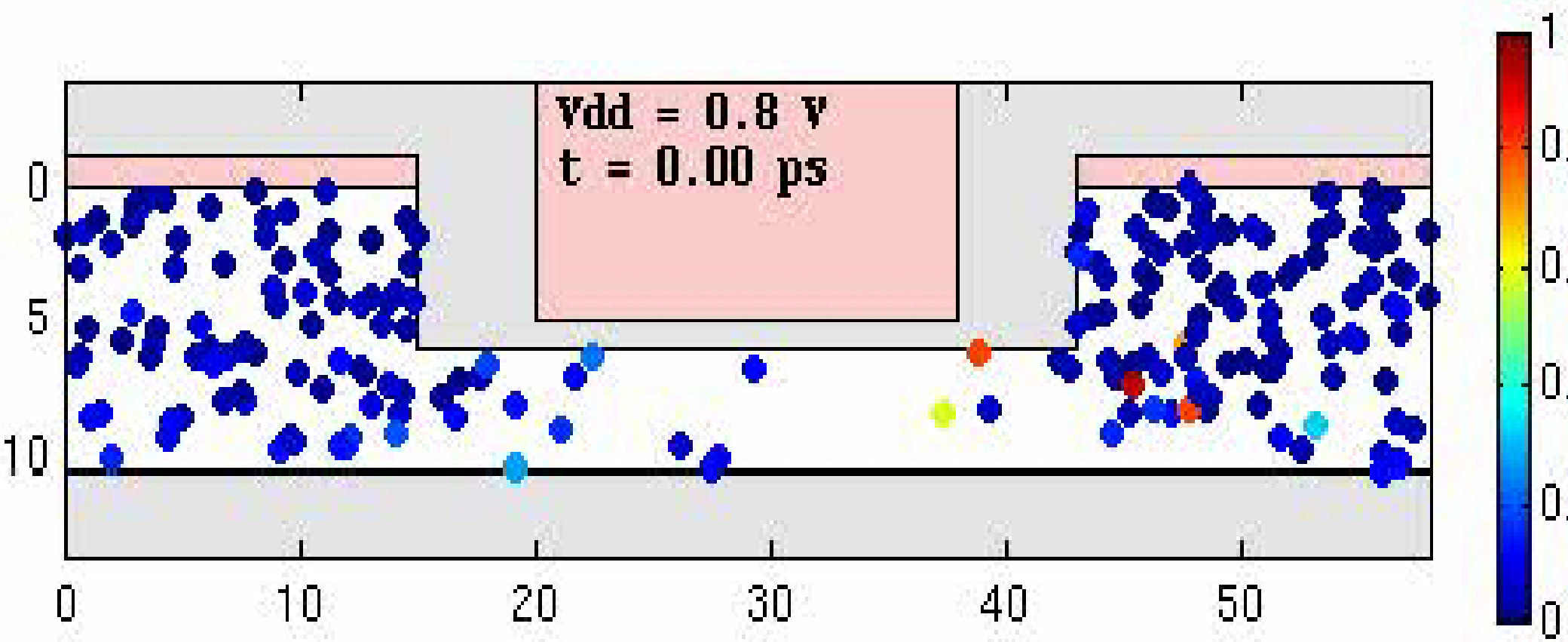
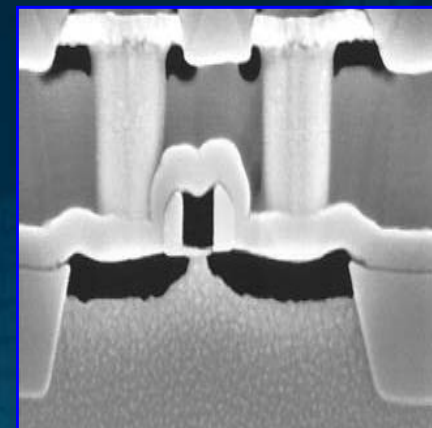
# Variations ... misplacing atoms



# Detailed view (atomistic)



# Counting $e^-$ ...



# *σ<sub>th</sub> variations*

- ◆ **Keyes** **1975**
- ◆ **Hagigava et al.** **1982**
- ◆ **Wong & Taur** **1993**
- ◆ **Mizuno et al.** **1994**
- ◆ **Wong et al.** **1998**
- ◆ **Asenov** **1998**
  
- ◆ **Random dopants, oxide thickness variations, line edge roughness, polysilicon granularity, interface roughness, high-*k* morphology**
- ◆ 
$$\sigma = t_{ox} N_A^{0.45} / (L_{eff} W_{eff})^{1/2}$$

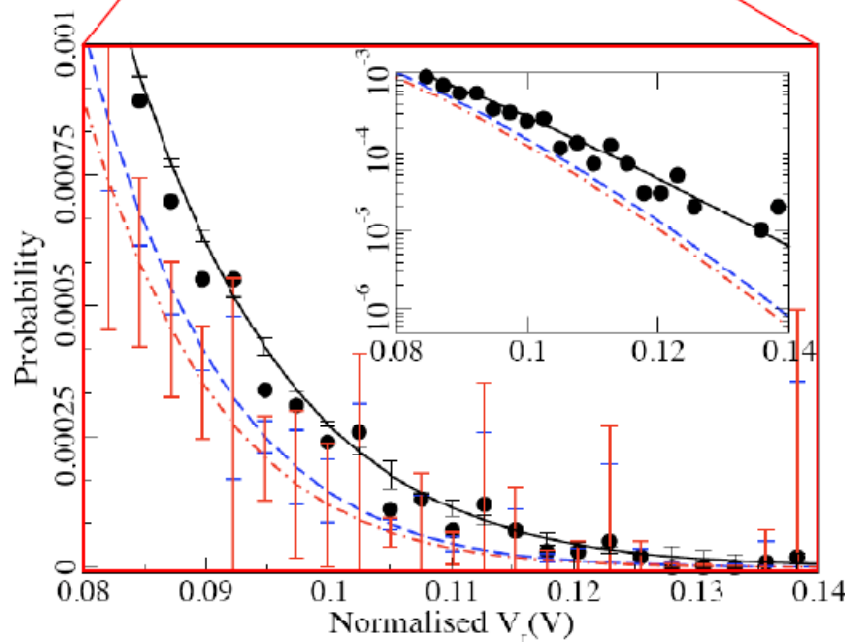
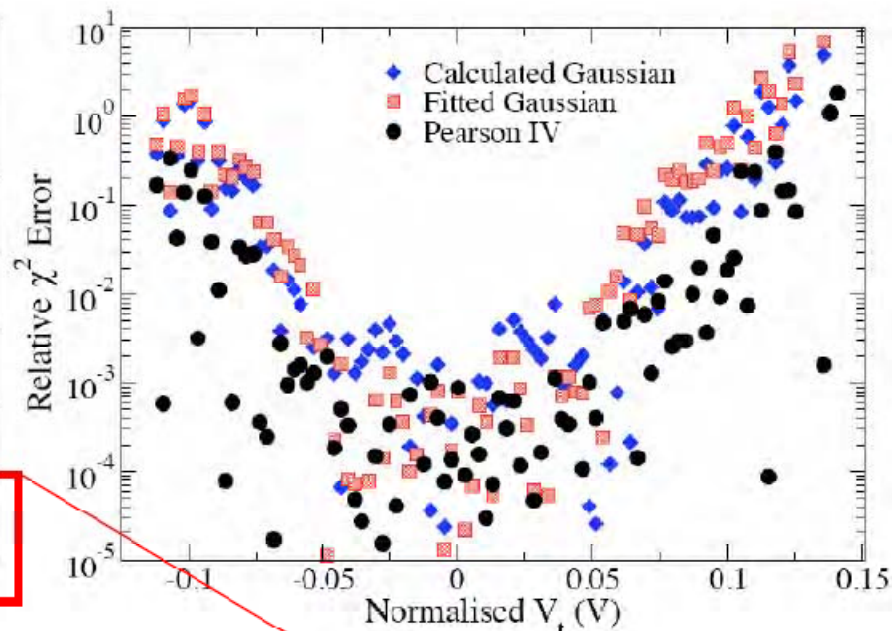
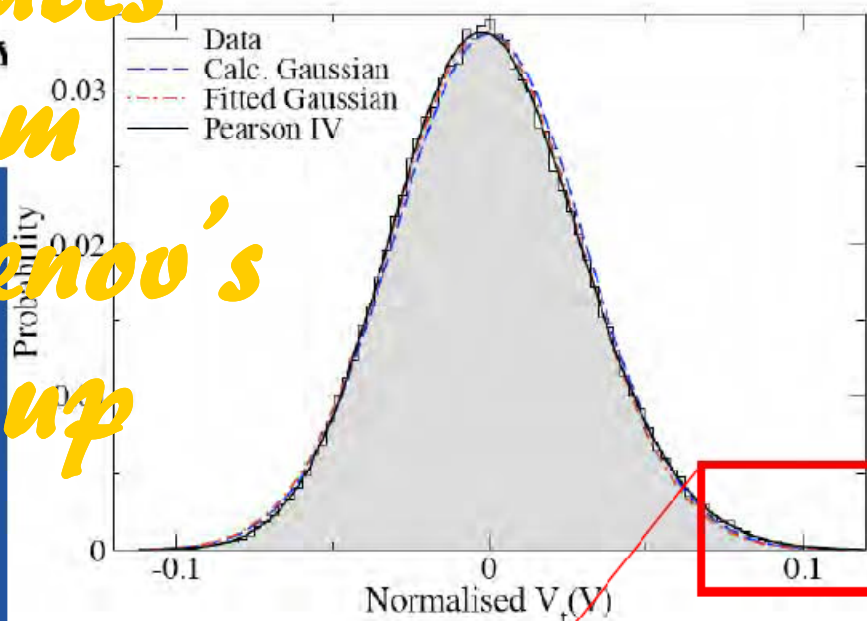
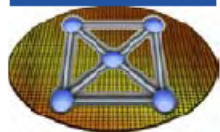
# The true shape of the distribution

Based on the simulation of 100000 transistors

Latest results

from Asenov's group

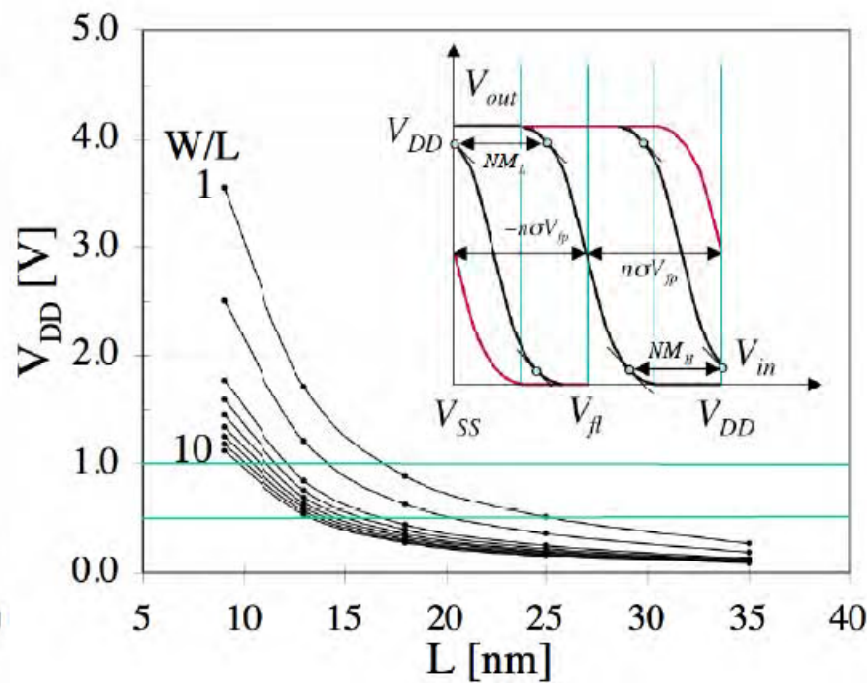
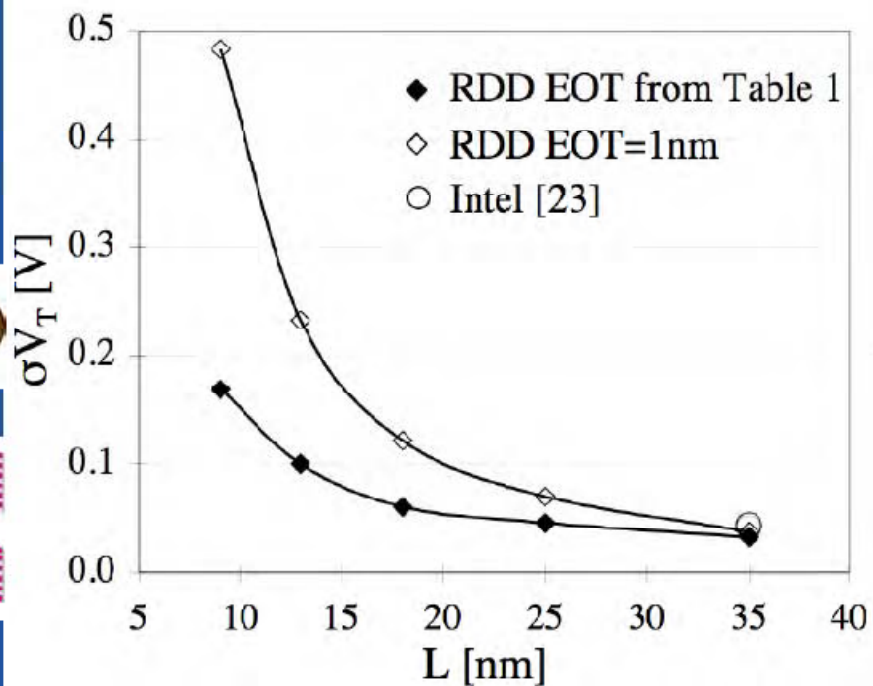
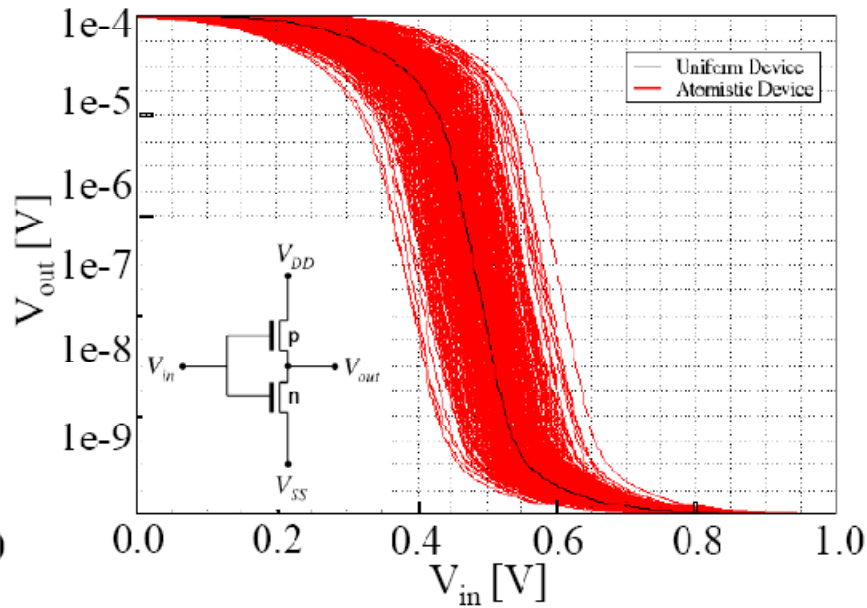
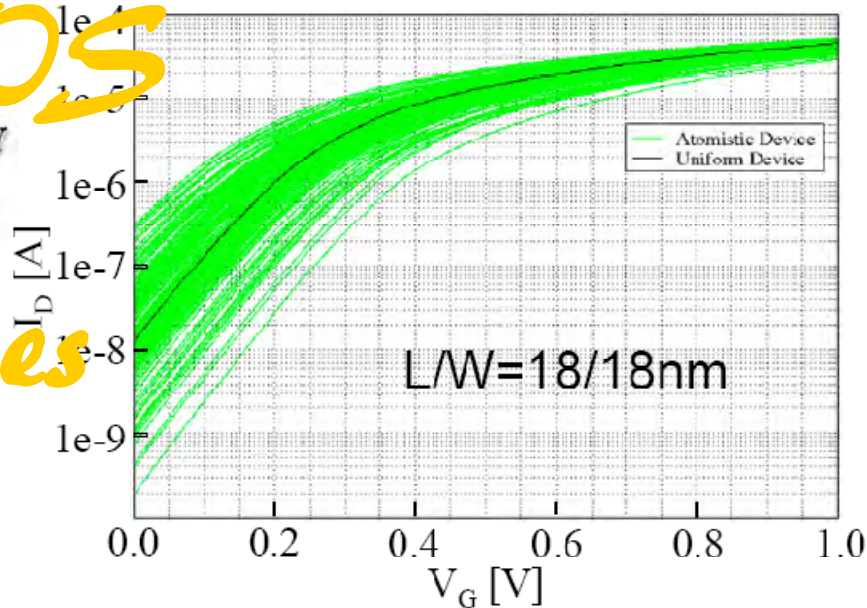
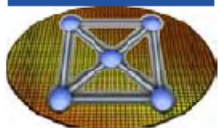
UNIVERSITY of GOSLAV



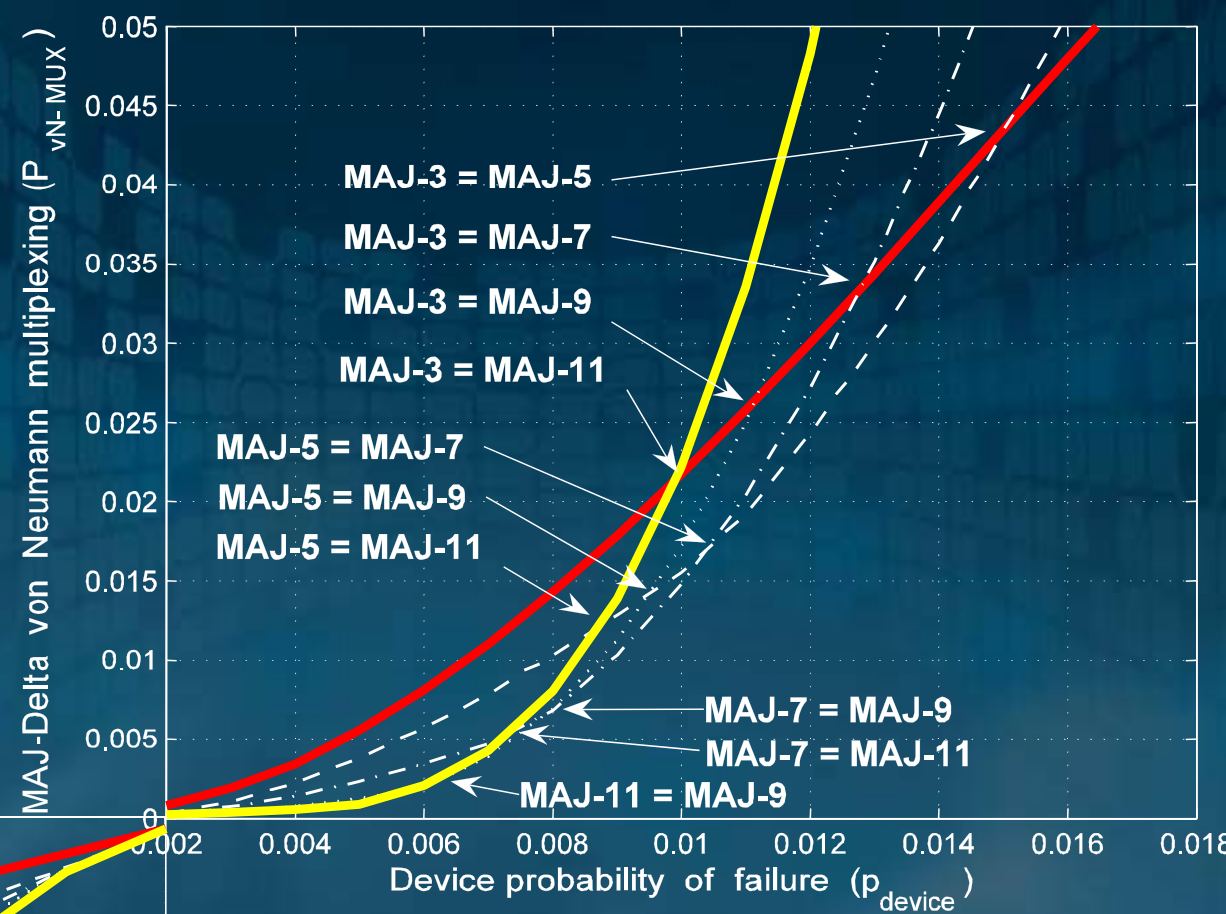
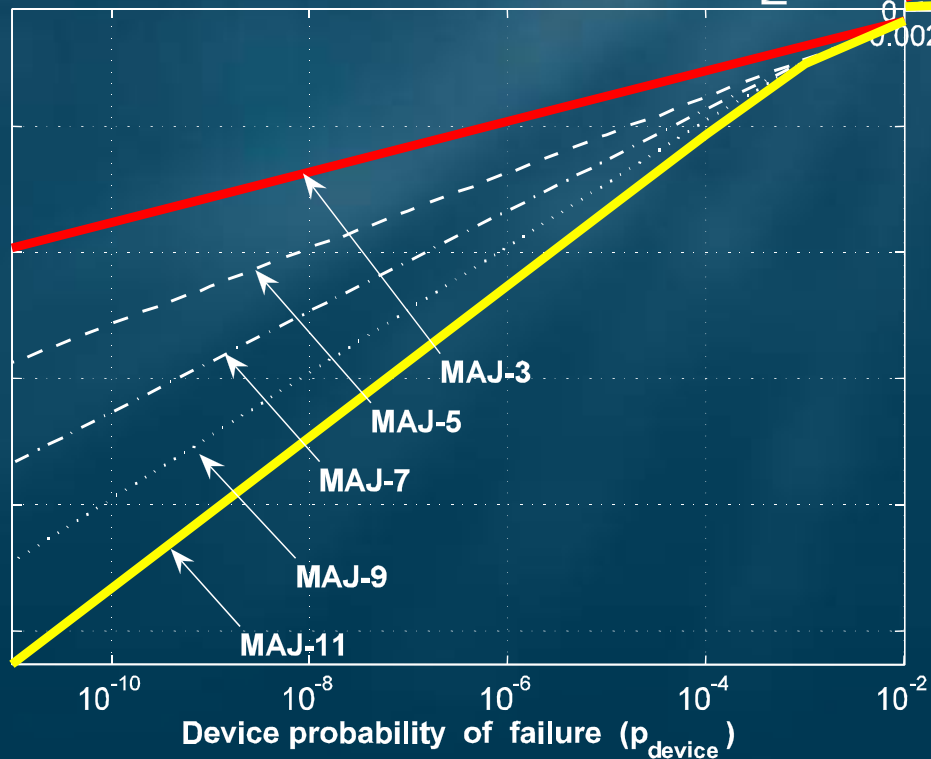
# Hard logic faults

From  
MOS  
to  
gates

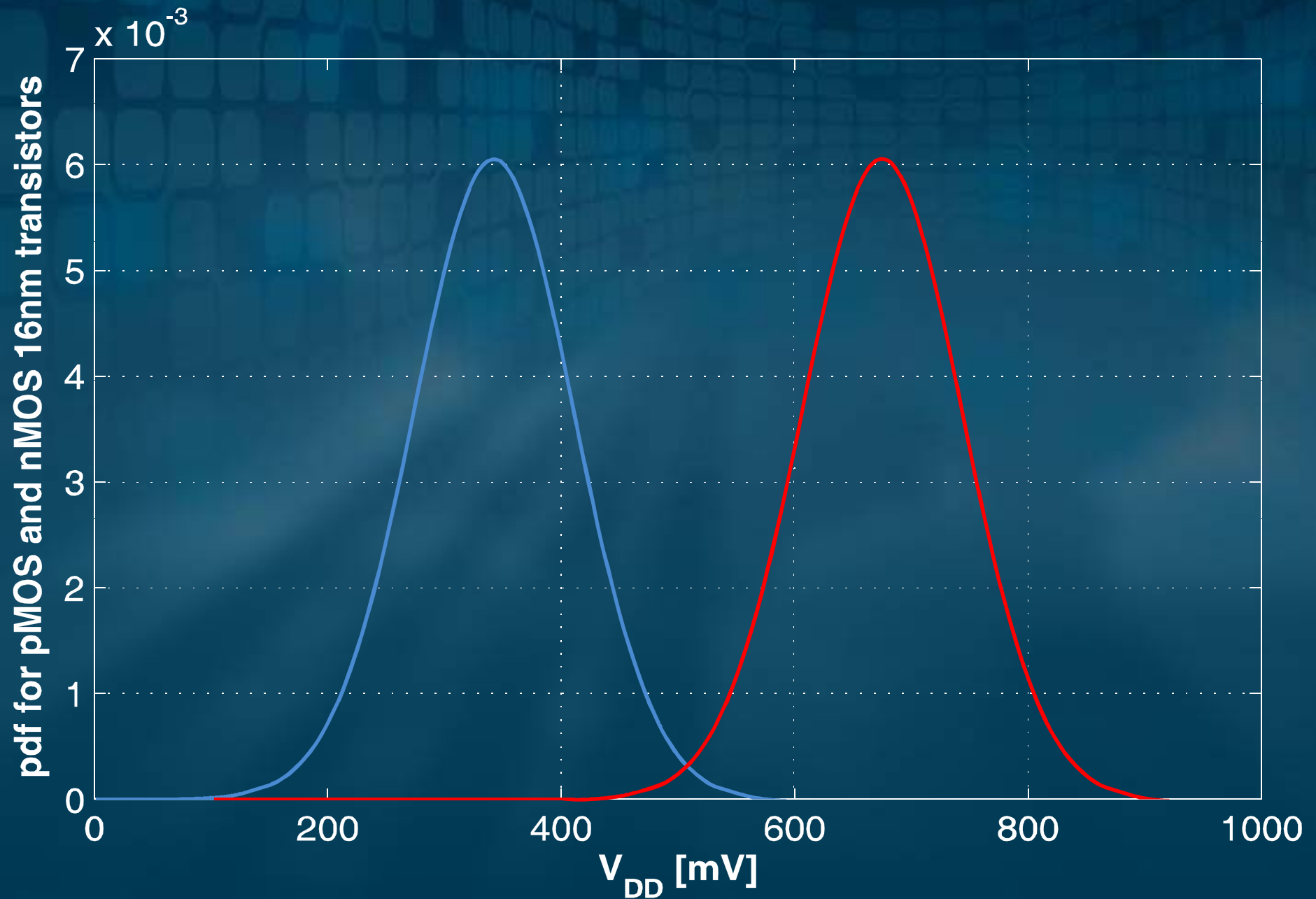
UNIVERSITY  
of  
GALGOW



# Devices get into the picture

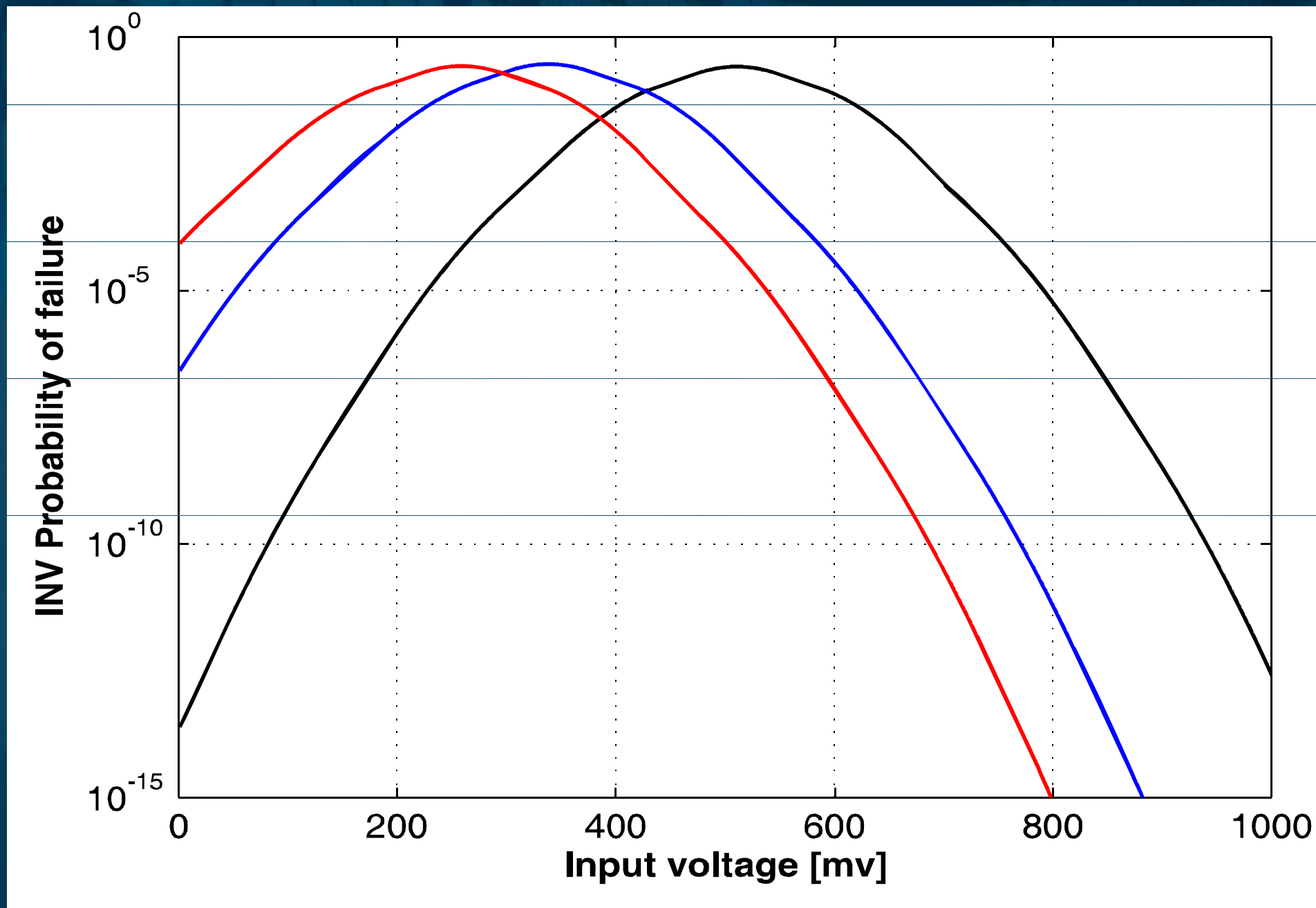


# Probability density functions

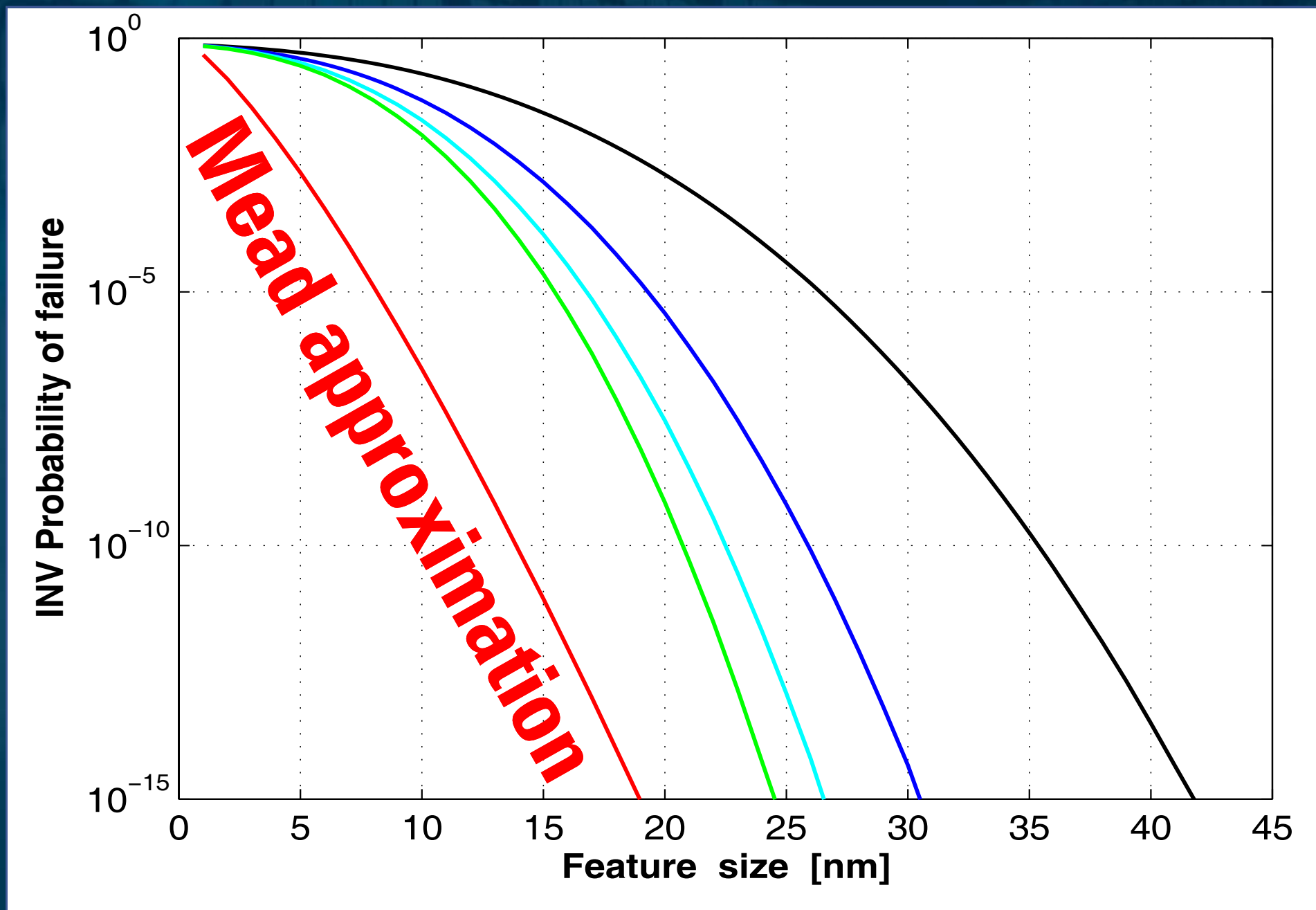




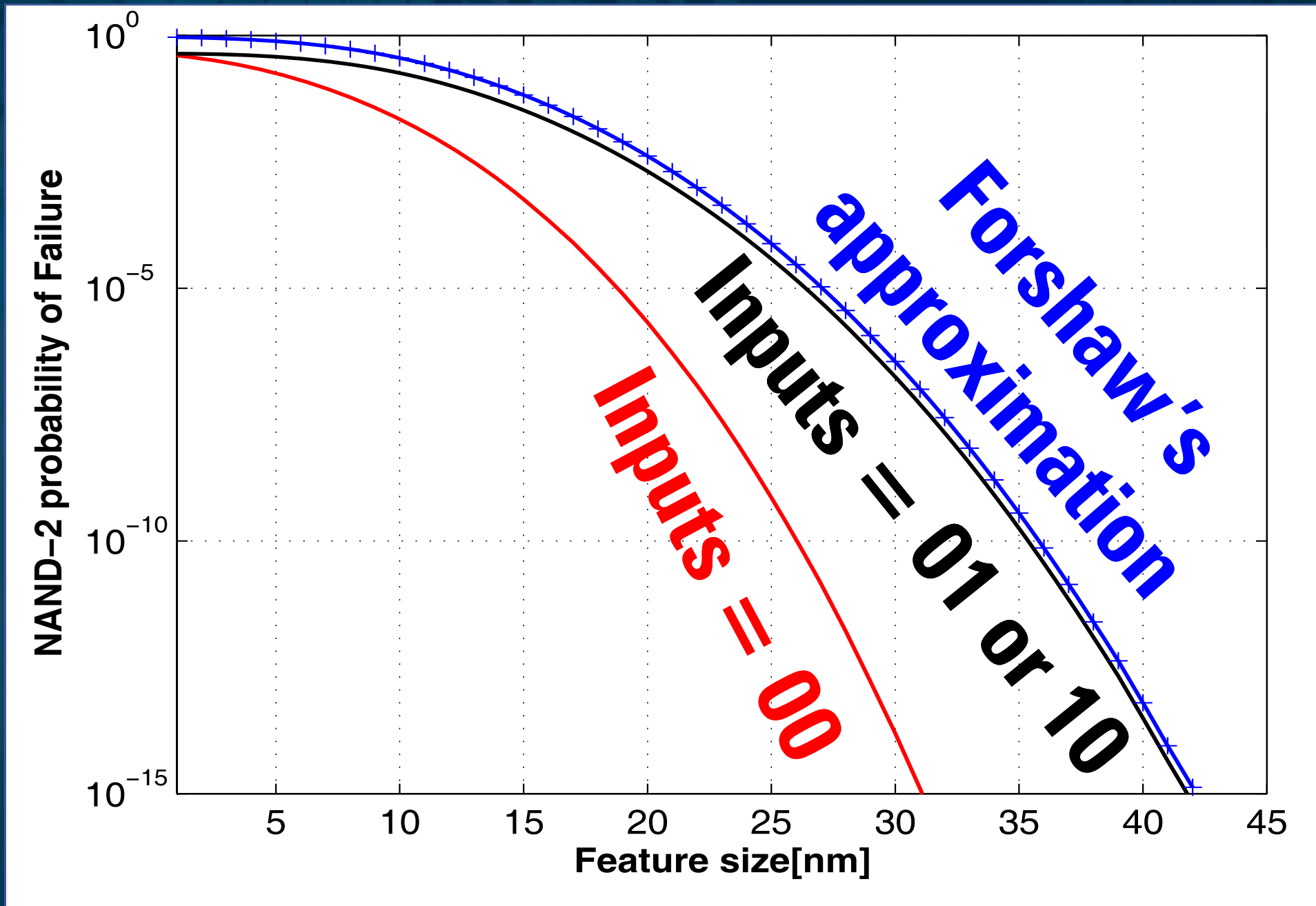
# *nMOS ... $V_{th}$ at $V_{DD}/2, 1/3, 1/4$*



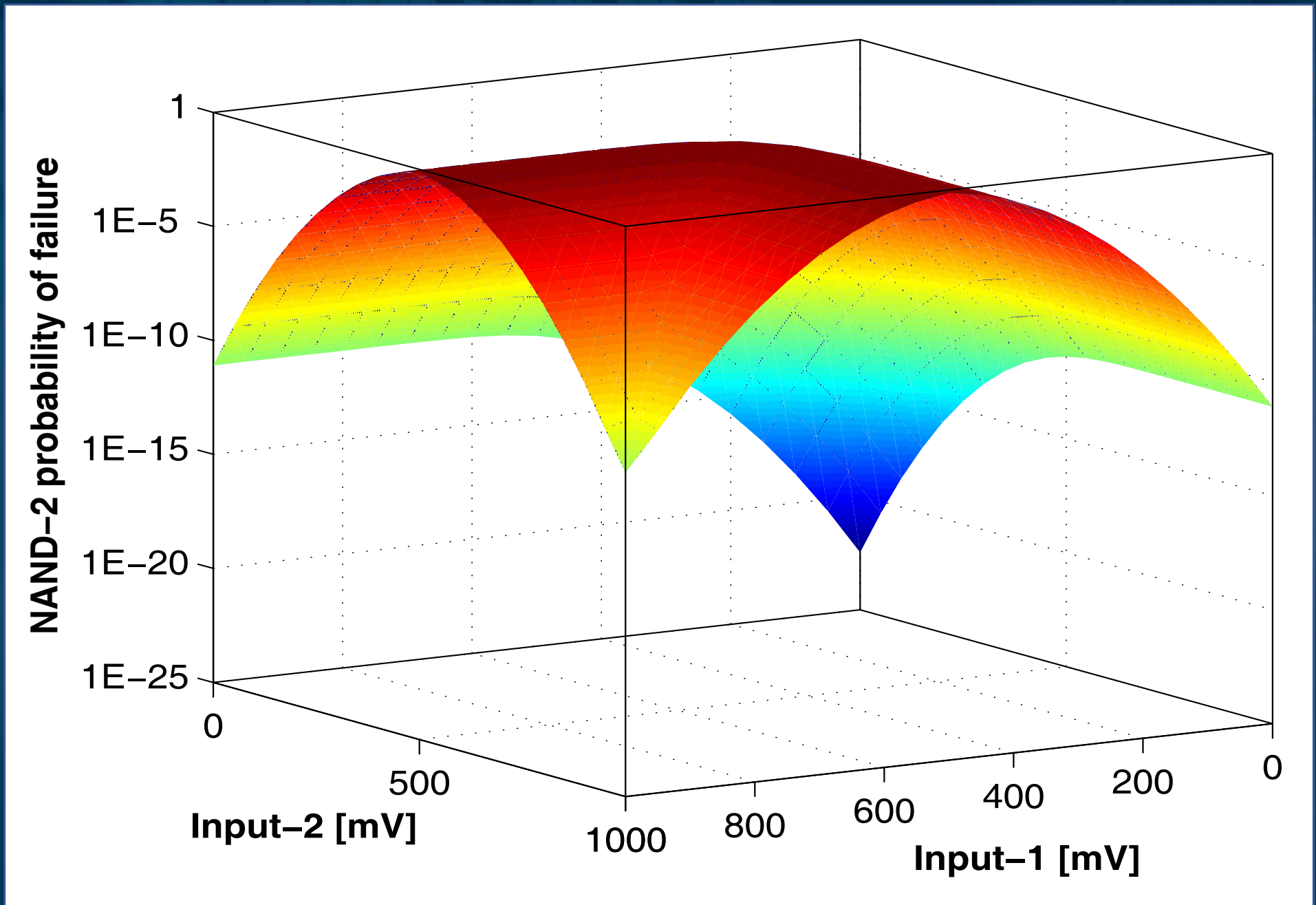
# Inverter (noise at $\sigma_{\text{odd}}/3, /4, /5 \dots$ )



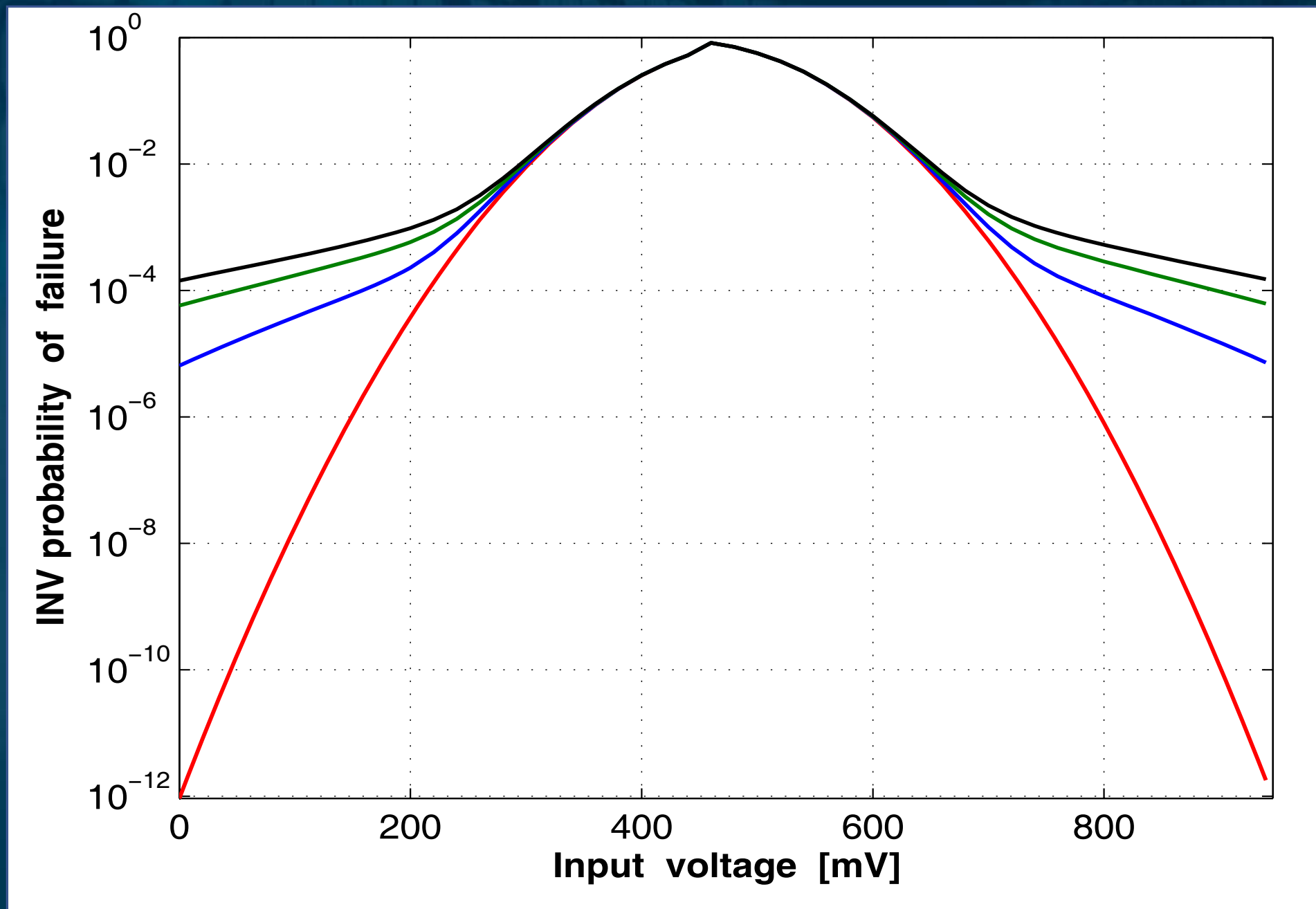
# NAND-2



# NAND-2 ... 3D view



# Inverter ... 2, 1.99, 1.98, 1.97



# Inverter 3D (at 1.97)

NAND-2 probability of failure

1  
1E-2  
1E-4  
1E-6  
1E-8  
1E-10  
1E-12

Input-1 [mV]

800

600

400

200

0

800

600

400

200

0

NAND-2 probability of failure

Input-2 [mV]

500

1000

800

600

400

200

0

Input-1 [mV]



*THANK YOU*

