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2009 Workshop on Dependable and Secure Nanocomputing

Scaling Effects on Neutron-Induced Soft Error in SRAMs Down to 22nm Process

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Macroscopic Mechanism of Terrestrial Neutron Soft-Error

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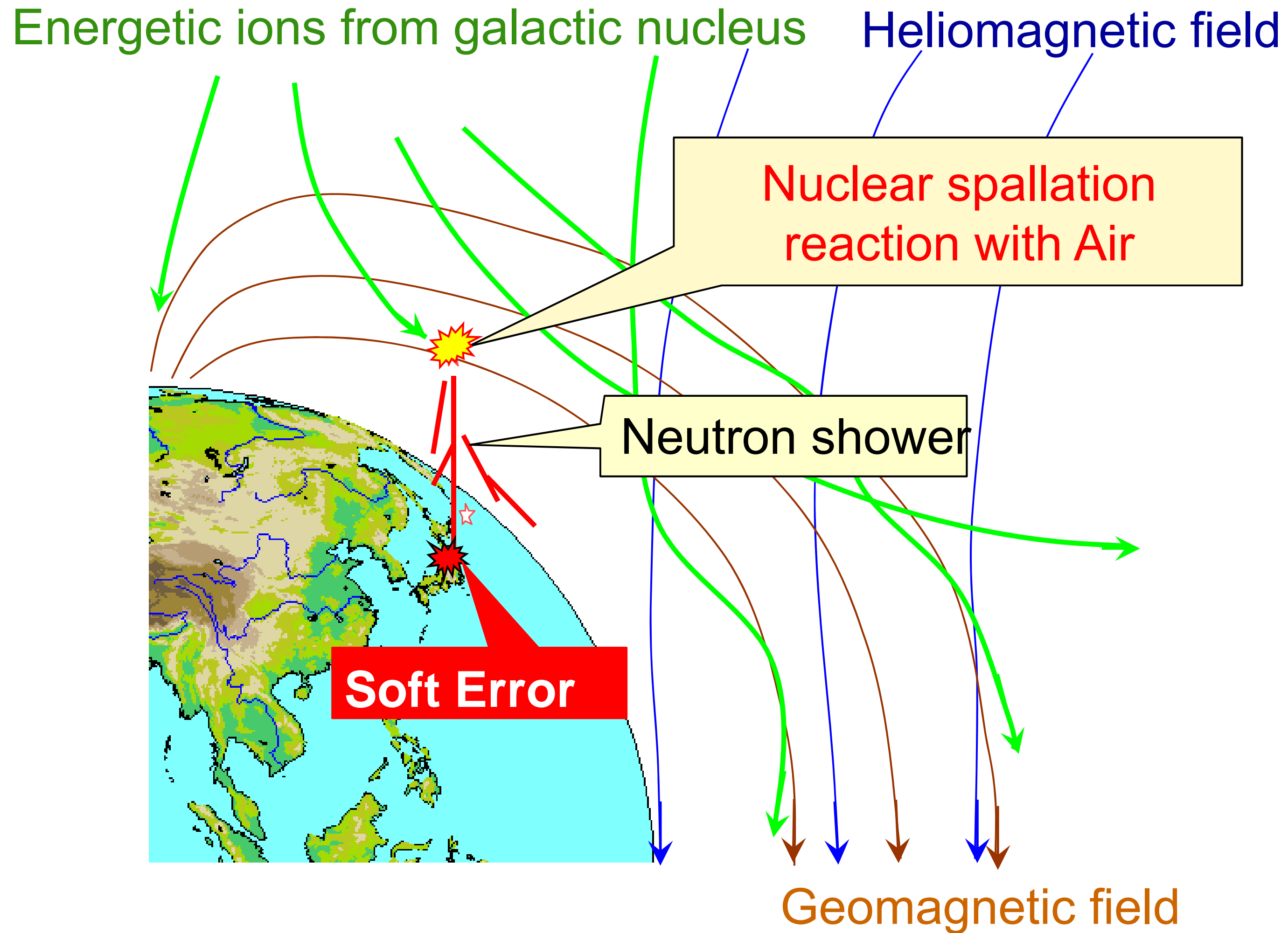

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2 Estimated Neutron Spectrum in Tokyo*

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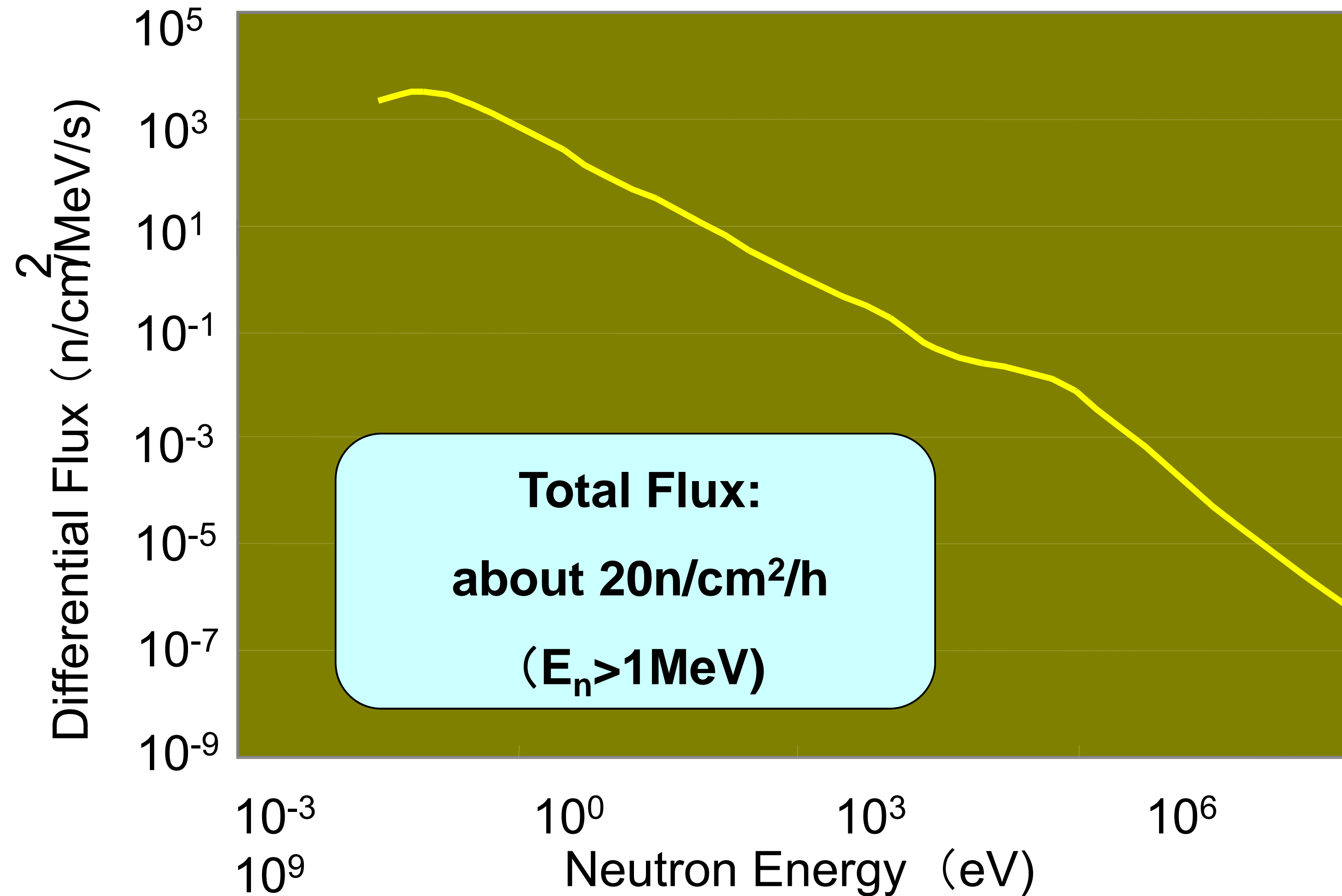

*Estimated from the spectrum at the sea level in NewYork (JESD89A,2006)

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Microscopic Mechanism of Soft-Error

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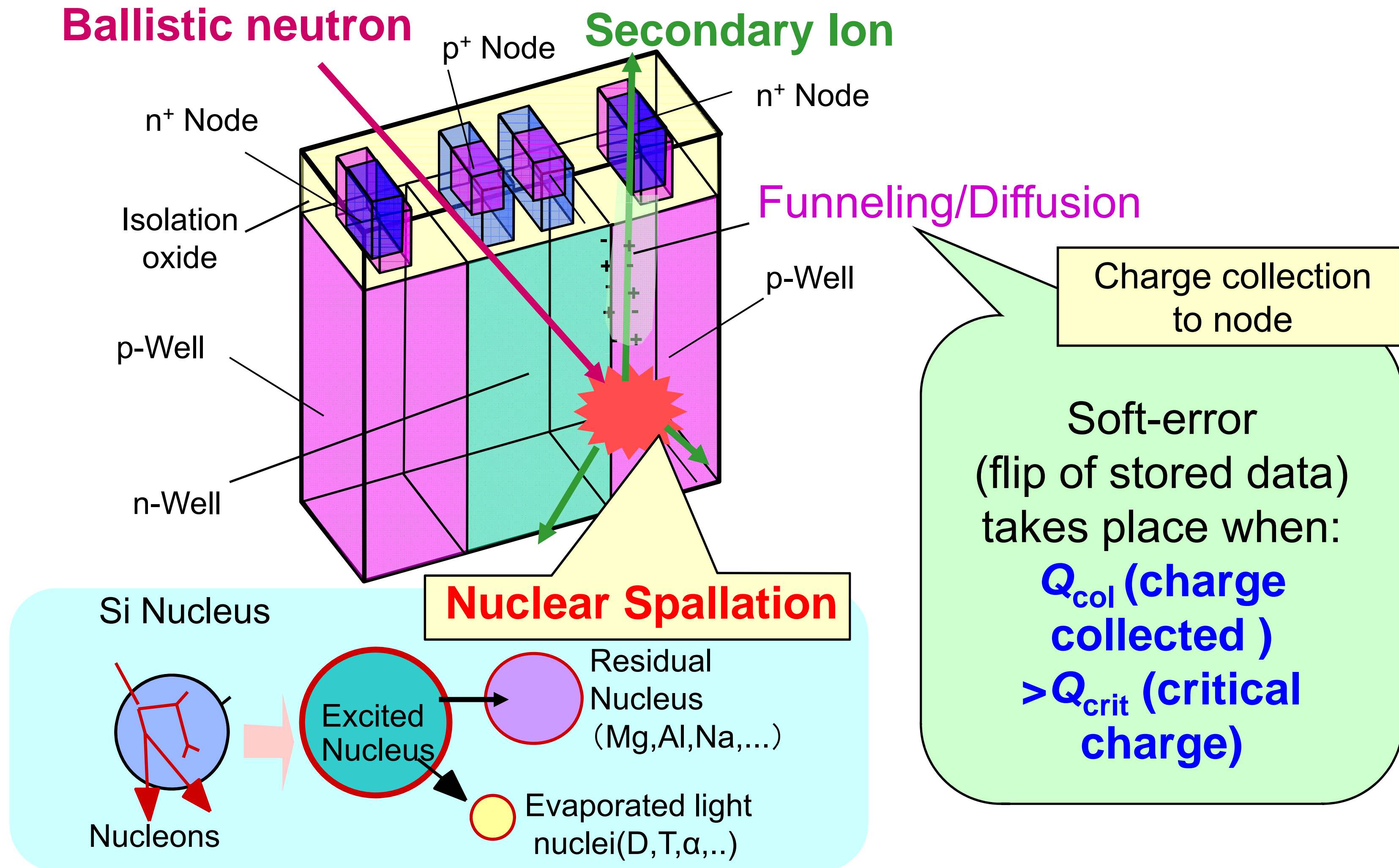

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Current General Trends Retrieved from Literatures

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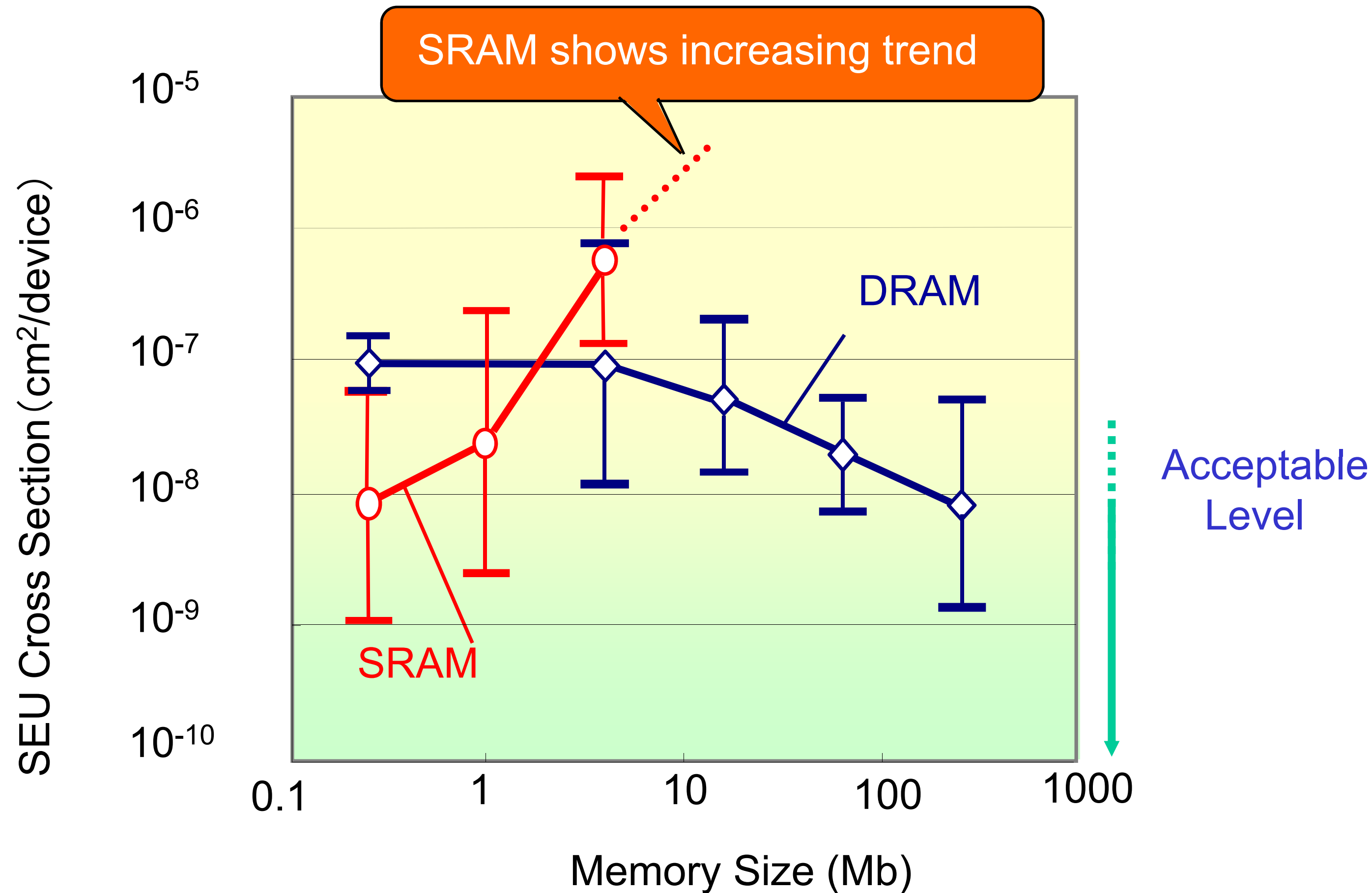

*SEU Cross Section = Errors/number of incident nucleon

Ibe, E., "Current and Future Trend on Cosmic-Ray-Neutron Induced Single Event Upset at the Ground down to 0.1-Micron-Device," The Svedberg Laboratory Workshop on Applied Physics, Uppsala, May,3, No.1 (2001).

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Features in CORIMS Models

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- First-principle model for nuclear spallation reaction
- Realistic model of devices (DRAM. SRAM, FF, SESO, ZRAM…) in 3D dimensions with storage nodes, interlayer oxide, STI, well, depleted zone, deep n-isolation, etc.
- Realistic charge collection models (funneling, drift-diffusion)
- No limit in the number of cells thanks to the Dynamic Cell Shift (DCS) model
- Any data pattern including AllX(All”1” and All”0”) and checkerboard (CB and its compliment)
- Interleaving technique can be implemented, which enables the ECC design.
- Any neutron/proton energy spectrum including environmental/ accelerator neutron spectra can be applied from the data base.

….and more

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SRAM Model

(A) TopView

bit-line

A

A’

Channel

n^+

p^+

p^+

n^+

x

y

z

Bit-Line

Word-Line

V_{dd}

GND

STI

(B) A-A’ Cross Section

n^+

p^+

p^+

n^+

p-Well

p-Well

n-Well

p Substrate

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DCS Method

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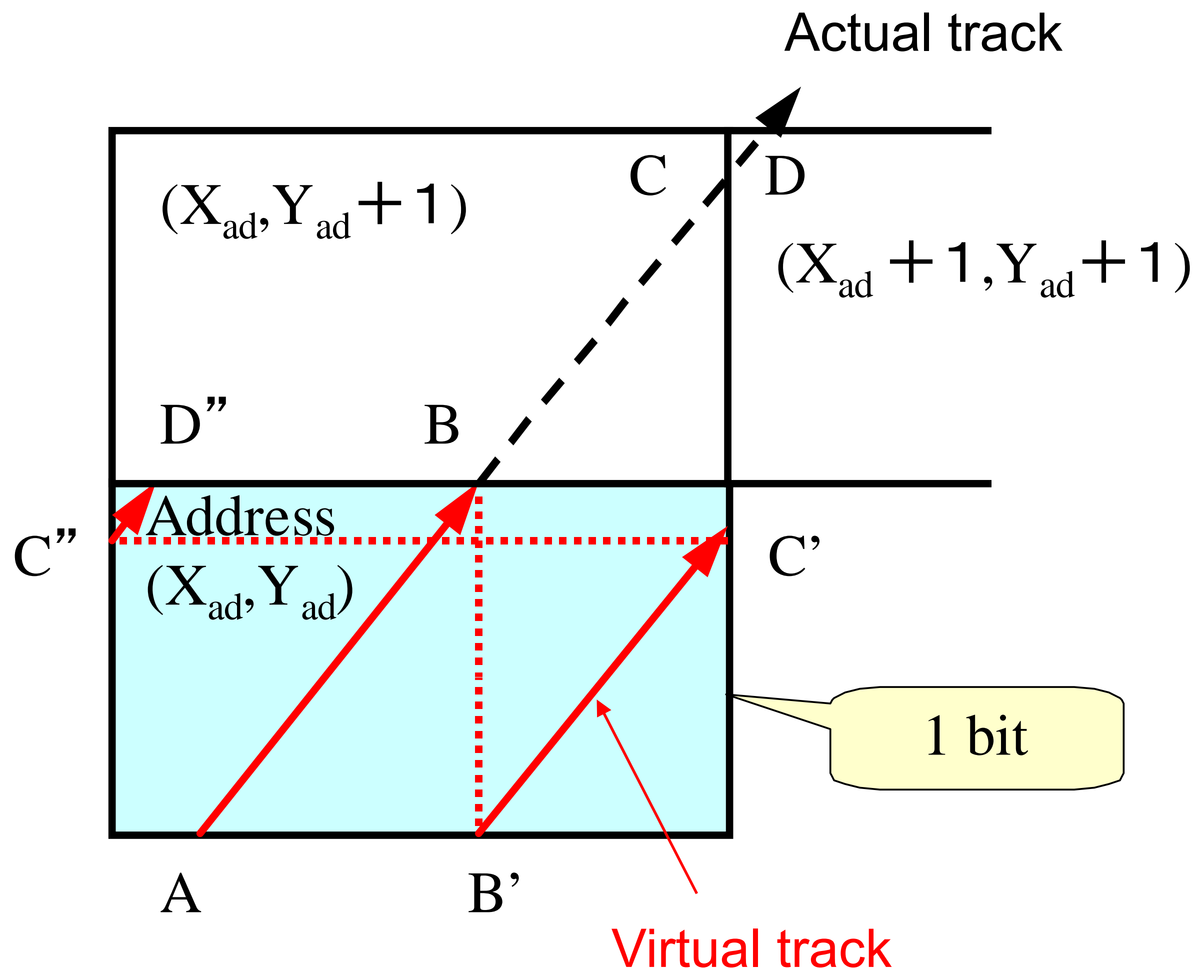

- Enables to calculate ion tracks until it stops without any ion range limit.
- Utilizes only one physical cell model (Does not make an NxN cell array)
- Shifts the ion track parallel when it reaches the cell boundary and the cell physical address is incremented or decremented according to the boundary location.

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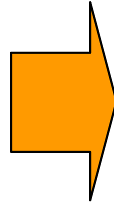
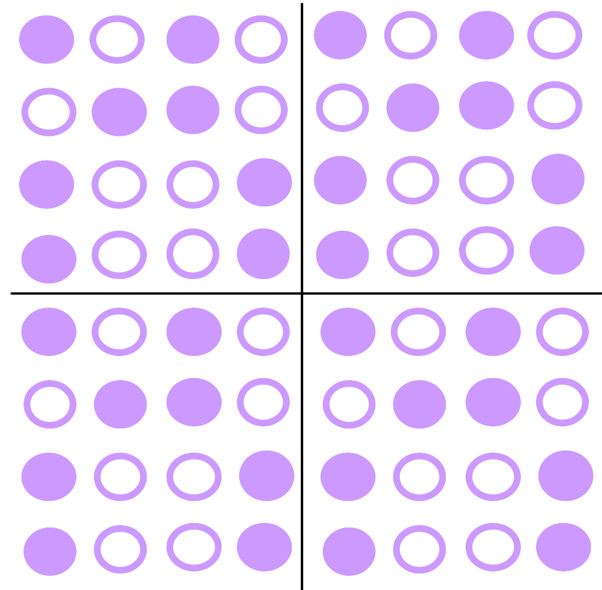
Data Pattern implementation

1	0	1	0
0	1	1	0
1	0	0	1
1	0	0	1

(a)Unit data pattern matrix





Cell with "1" Cell with "0"

(b) Spreading the matrix onto a device

- Define unit data pattern matrix including CB and AllX
- Virtually spread the matrix onto a device and the data in a cell can be calculated according to the physical address.

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Display of Part of Cell Array Matrix and Ion tracks

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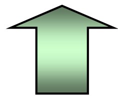
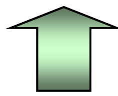
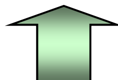
SER Calculation



Error analysis



Ion Track analysis



Nuclear Spallation Spallation

Data Pattern All"1"

Trace the ion track until it stops or gets out of the sensitive layer

Spallation area (1 bit)

Device name 4MLP

Close End

Tracks through node
Tracks through well
Node with data "high"(n^+)

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Validations of the Model

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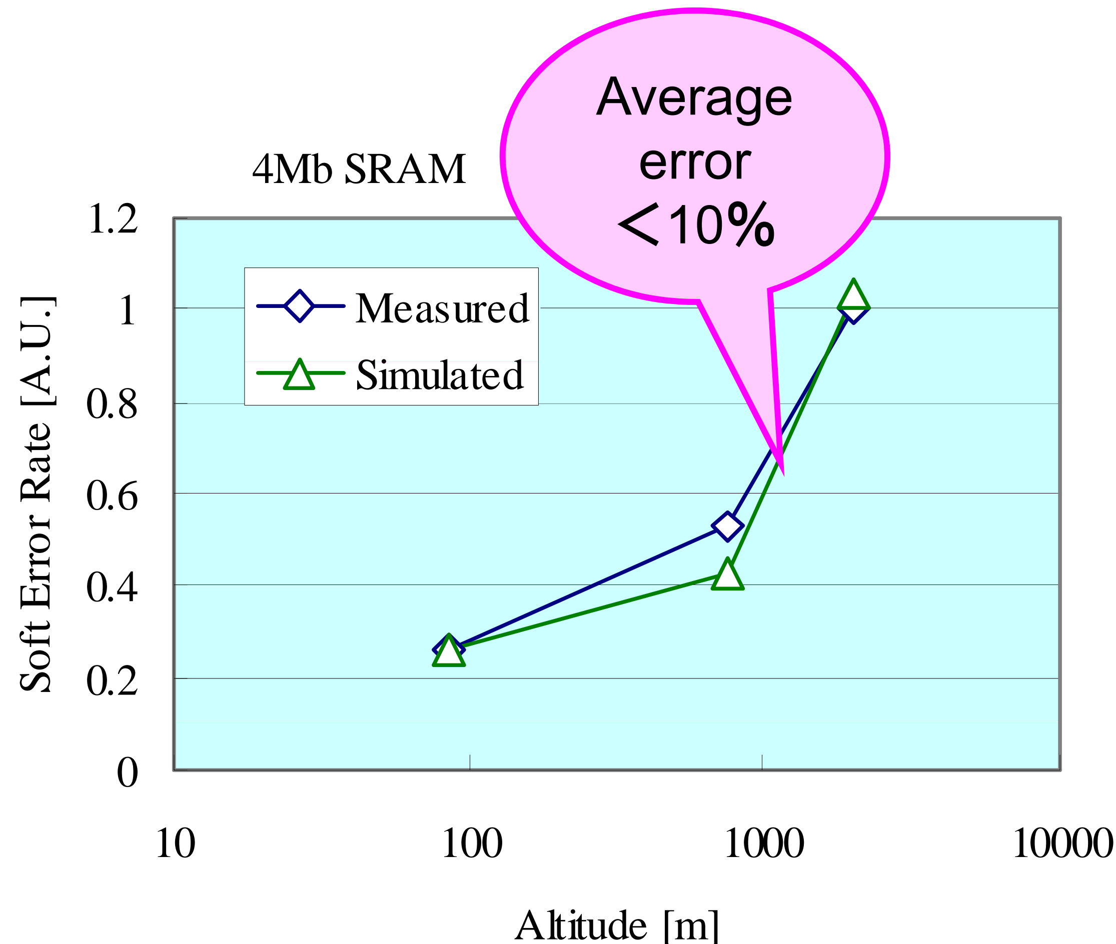
Comparison between measured and simulated SERs in three different locations in Japan



- Within 20% error for simulations of experiments in :

-TSL (Uppsala, Sweden)

-CYRIC (Sendai, Japan)

-LANSCE(Los Alamos, USA)

-RCNP(Osaka, Japan)

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Assumed Road Map

Assumptions

- Cell area decreases by half for each down-scaling.
- Density doubles.
- Critical charge decreases by half

(In principle, critical charge is in proportion to parasitic capacitance which again in proportion to cell area)

- Depth profile does not change
- Operation voltage does not change

Design rule	SRAM property		
	Cell area	Density	Qcrit
nm	A.U.	Mbit	A.U.
130	2.1	16	3.2
90	1	32	1.6
65	0.5	64	0.8
45	0.25	128	0.4
32	0.125	256	0.2
22	0.06	512	0.1

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Major Simulation Results(CB)

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Design rule	SER (A.U)		MCUratio	MCU maximum size	Maximum bit multiplicity
nm	per device	per Mbit	%	bit	bit
130	1	1	7	459	10
90	2.0	1.00	14.8	14940	16
65	3.2	0.81	21.2	114170	19
45	4.4	0.55	27.2	118665	48
32	6.1	0.38	38.5	1932765	52
22	7.0	0.22	46	463638	175

- SER /Mbit decreases with down-scaling but SER /device increase x7 from 130nm to 22 nm.
- MCU ratio increases x7 from 130nm to 22nm
- MCU maximum size (MxN bits rectangular area that includes failed bits) exceed as many as 1Mbits in the extreme case.
- Maximum bit multiplicity exceeds as many as 100 bit for 22nm process.

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Spread in Failed Bit Map for All Errors

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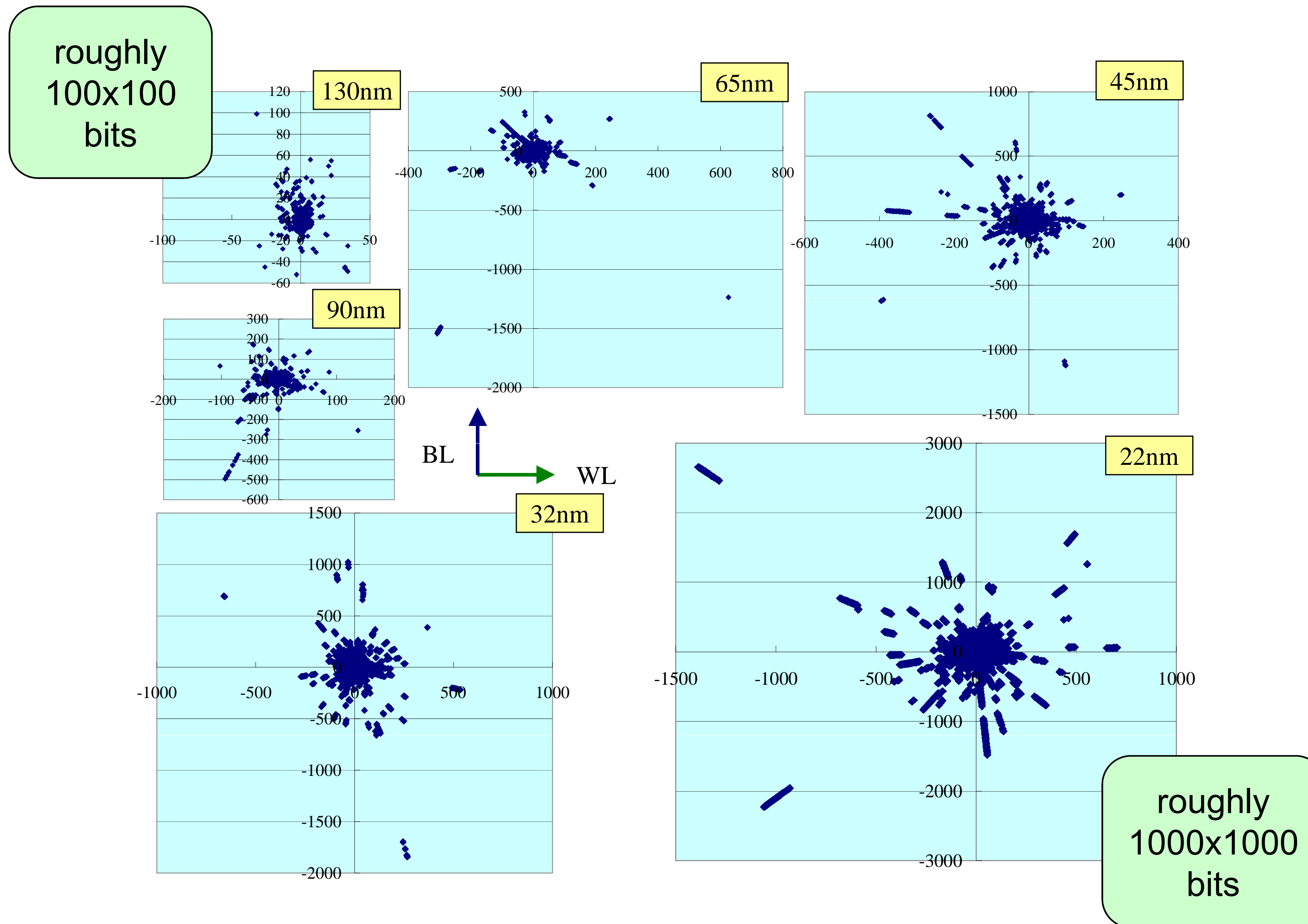

*Spallation reaction location is the origin.

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Shifts in SEU Cross Section

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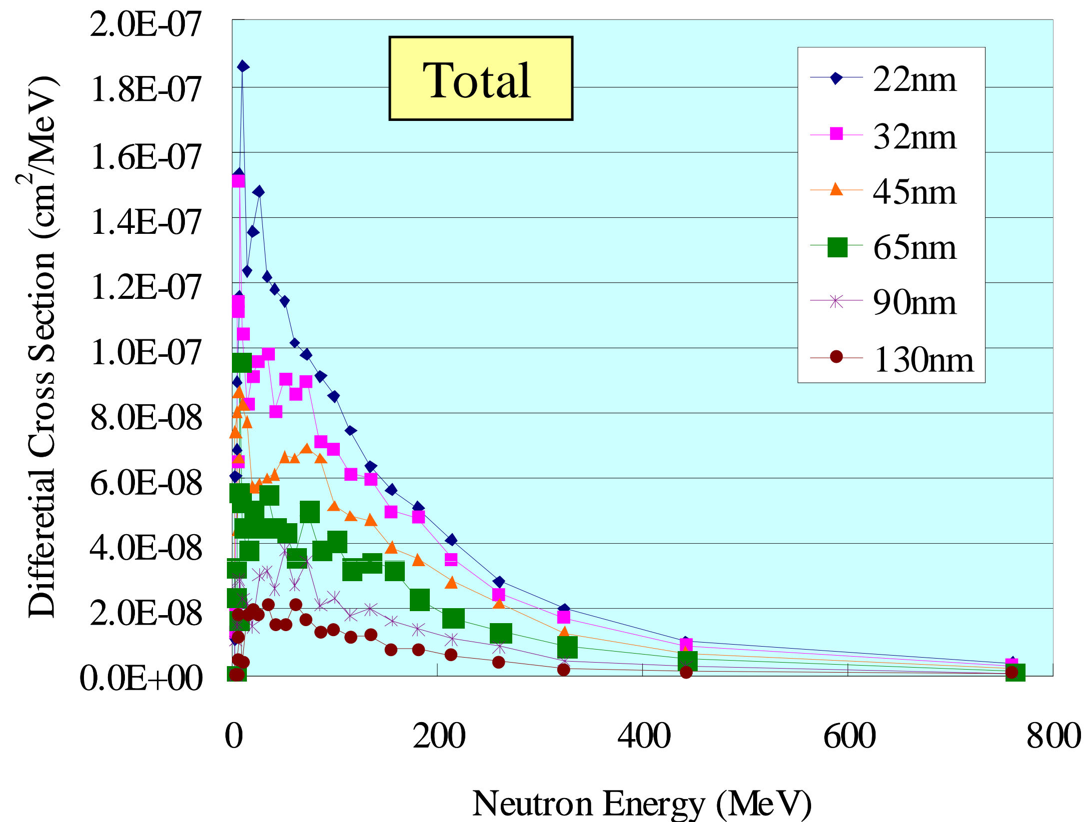

- SEU includes SBU(Single Bit Upset) and MCU(Multi Cell Upset).
- The peak in the cross section curves becomes more apparent and appears at lower energies with down-scaling
- The shape of the cross section curves changes from saturation curve (130nm) to exponential-like curves with down scaling
- Contribution of lower energy neutron become more significant with down-scaling

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Changes in MCU Cross Section

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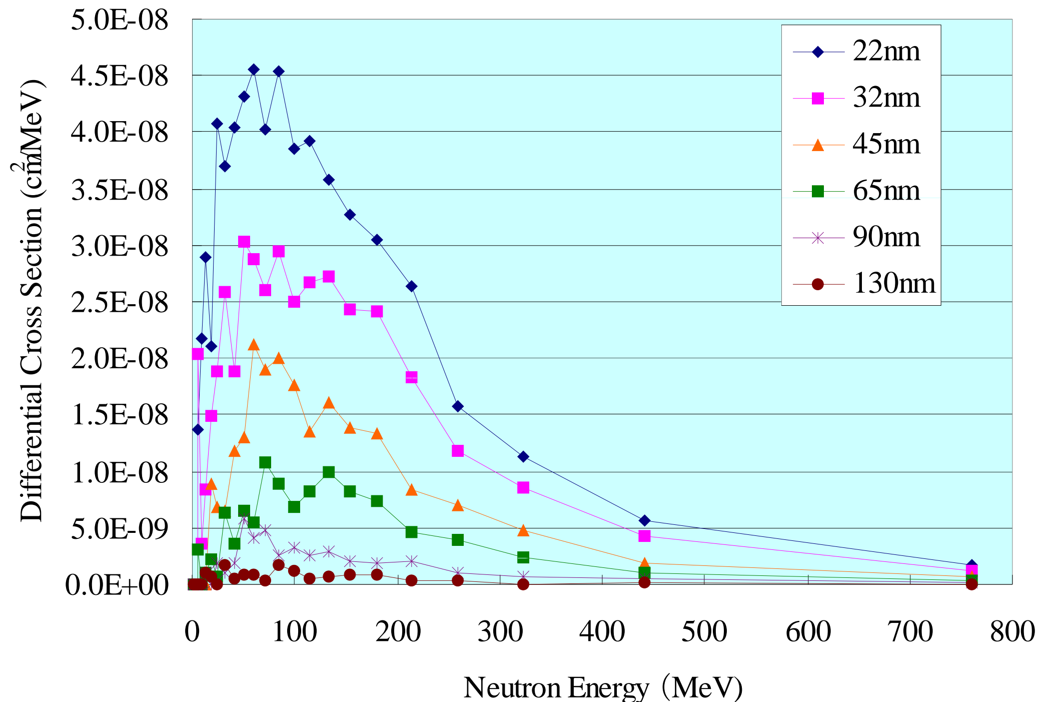

- The shape of the MCU cross section curves does not change significantly with the peak location roughly at 60-100MeV.
- The shape of the MCU cross section curves is basically exponential-like for the higher neutron energy than about 100MeV.
- Comparison with the SEU cross section indicates that SBU is dominant below 100 MeV and become more significant with down-scaling.

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Shifts in Bit Multiplicity

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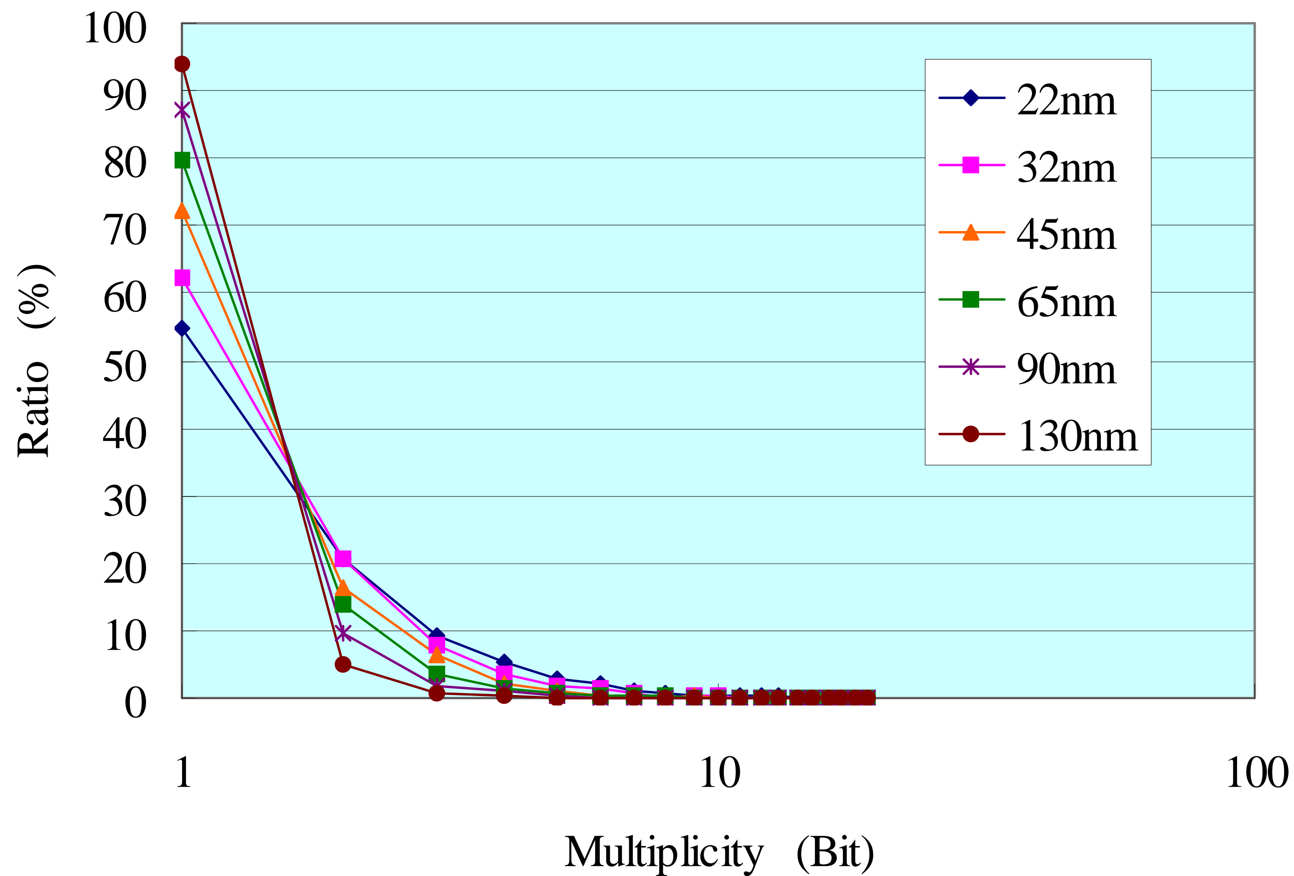

■Bit multiplicity increases with down-scaling

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Factors that Affect Prediction Accuracy

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Factor	Assumption	Possible trend	Influence
Operation voltage	constant	decrease	Q_{crit}↓ SER↑
Depth profile	constant	shallower and denser	SER↓
Gate oxide material	SiO_2	HfO (high k)	Q_{crit}↑ SER↓
Inter-layer isolation	SiO_2	Low-k	Q_{crit}↓ SER↑

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Implications for Logic Devices

■Increases in MCU bit multiplicity and in MCU size imply that MNU(Multi Node Upset:Multiple faults in nodes in a logic device) takes more often and in wider area.

■ Increase in MNU may impair radiation-hardened device with redundancy nodes like DICE.

■ Increase in MNU also implies that logic devices in the vicinity may be failed simultaneouly resulting in impairing redundancy circuits like DMR, TMR and so on.

■Nobel radiation hardening techniques have to be developed for logic devices and systems with a large number of logic devices with reasonable speed/power/area overheads. Interactive countermeasures among device/component/system layers will be effective.

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Summary

- Soft-error rates per device in SRAMs will increase x7 from 130nm to 22nm process.
- As SRAM is scaled down to smaller size, soft error rate is dominated more significantly by low energy neutrons (<10MeV)
- The area affected by one nuclear reaction spreads over 1M bits area and bit multiplicity of multi-cell upset become as high as 100 bits and more.
- The discussions are extended to the MNU of logic devices and systems. Development of interactive countermeasures among device/component/system layers is proposed to cope with the real threats in the future.

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Reference

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- **T. Nakamura, M. Baba, E. Ibe, Y. Yahagi and H. Kameyama, Terrestrial Neutron-Induced Soft-Errors in Advanced Memory Devices, World Scientific, 2008**

Thank you for your attention!

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