Trading Off Dependability and Cost for Nanoscale High Performance Microprocessors: The Clock Distribution Problem

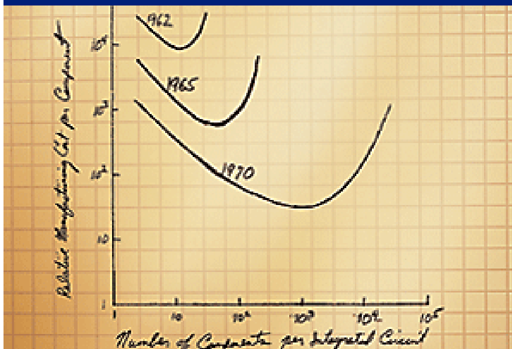
Cecilia Metra

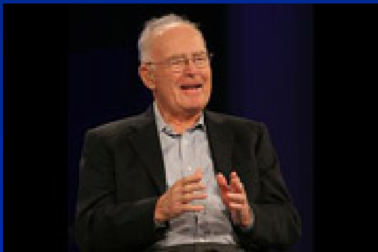
ARCES - DEIS – University of Bologna

cecilia.metra@unibo.it

Scaling of Microelectronic Technology

- **Scaling of microelectronic technology:**
  - ↑ IC complexity and ↑ IC performance.





MOORE'S LAW

transistors

10,000,000,000
1,000,000,000
100,000,000
10,000,000
1,000,000
100,000
10,000
1,000

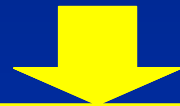
1970 1975 1980 1985 1990 1995 2000 2005 2010

Dual-Core Intel® Itanium® 2 Processor
Intel® Itanium® 2 Processor
Intel® Itanium® Processor
Intel® Pentium® 4 Processor
Intel® Pentium® III Processor
Intel® Pentium® II Processor
Intel® Pentium® Processor
Intel486™ Processor
Intel386™ Processor
286
8086
8080
8008
4004

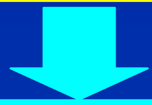
Courtesy of Intel Corporation *Intel Techn. Journal, 2007*

Scaling and Clock Due Dependability Risks

- **But scaling comes together with:**
  - **↑ IC complexity → ↑ # of switching elements → ↑ power supply noise**
  - **↑ operation frequency → time margins ↓**
  - **↑ likelihood of fabrication defects**
  - **↑ entity of on-die process variations**



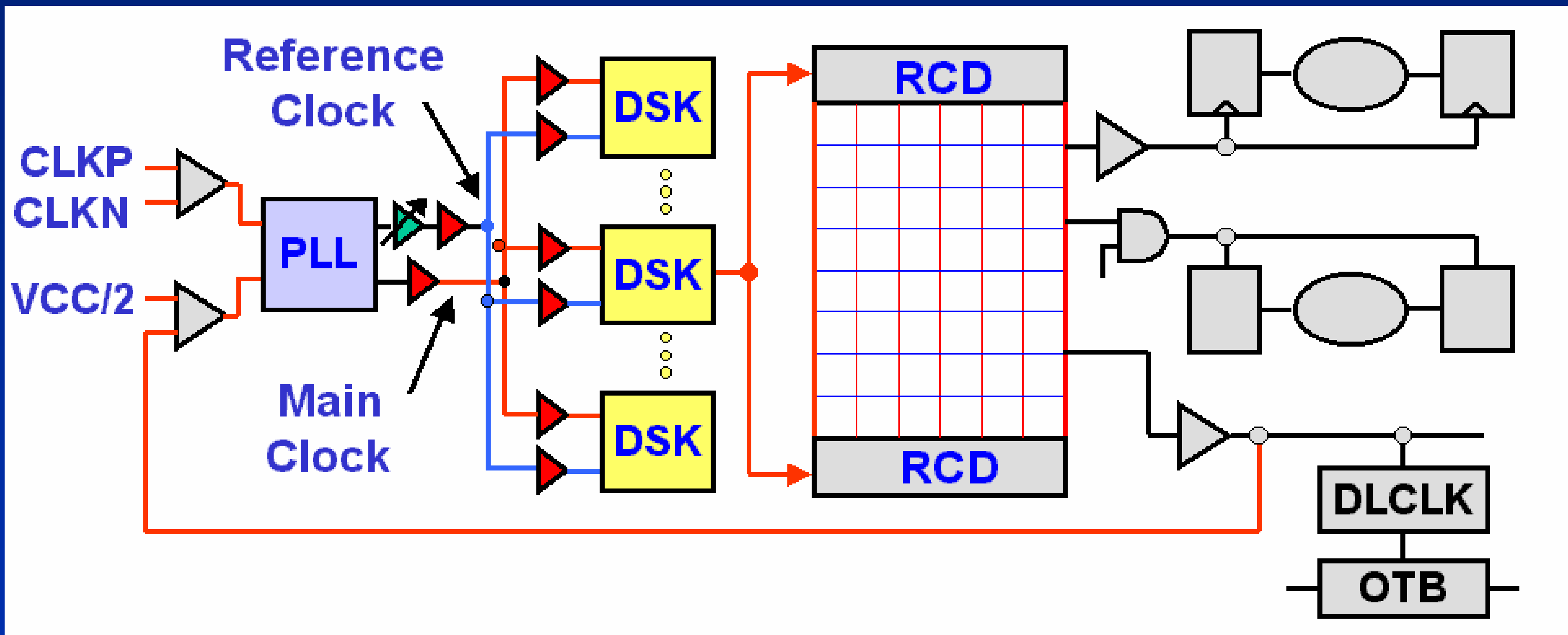
↑ difficulties in ensuring limited skew, jitter and correct duty cycle for all clock signals of a synchronous system



↓ System Dependability

Clock Distribution

- **Complex network**, spreading out throughout the whole chip (horizontally and vertically).



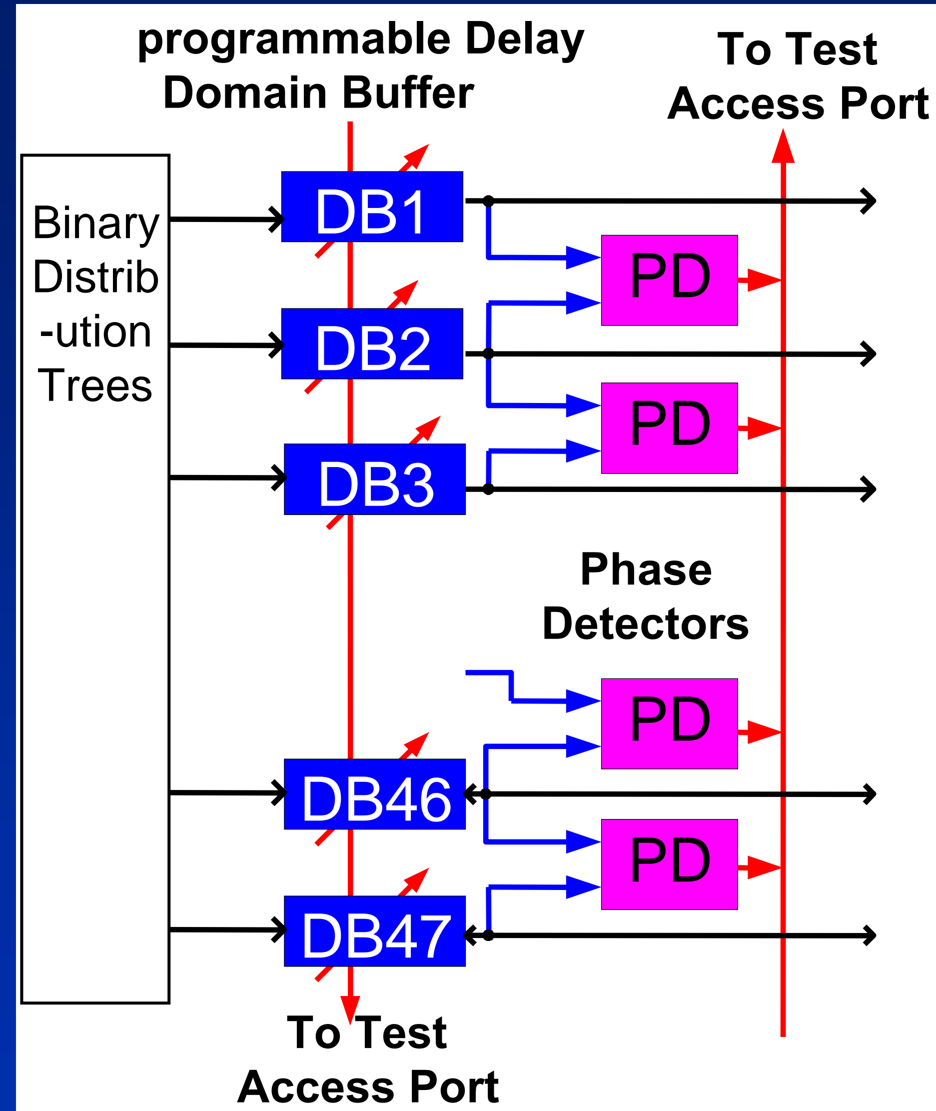
S. Tam, S. Rusu, U.N. Desai, R. Kim, J. Zhang, I. Young, "Clock Generation and Distribution for the First IA-64 Microprocessor", IEEE J. of Solid-State Circuits, Vol. 35, No 11, pp. 1545 - 1552 , 2000.

Clock Compensation

- ODCS (On Die Clock Shrink):
  - intended to compensate duty cycle variations (mainly due to parameter variations) at the PLL output
- DSK (DeSKew buffers):
  - intended to compensate skew (mainly due to parameter variations) at the global clock level

DSK Example: Pentium®4

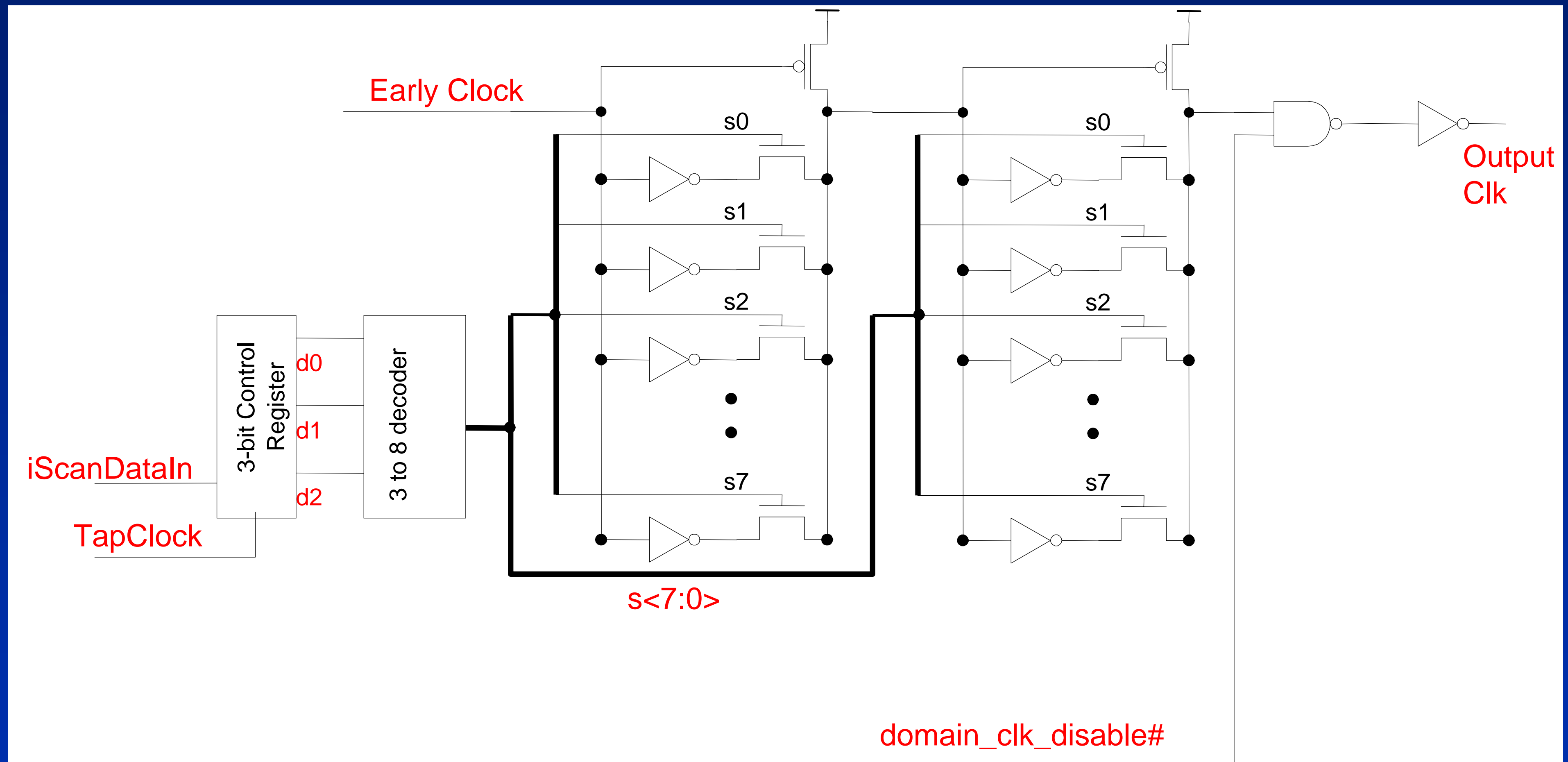
- Intel™ Pentium®4 example:
  - **PD:** Phase Detectors
  - **DB: programmable Delay Buffers,** whose programming bits can be fixed permanently



N.A. Kurd, J.S. Barkatullah, R.O. Dizon, T.D. Fletcher, P.D. Madland, "A Multigigahertz Clocking Scheme for the Pentium® 4 Microprocessor", IEEE J. of Solid State Circuits, Vol. 36, No. 11, Nov. 2001, pp. 1647-1653.

DSK Example: Pentium®4 (cnt'd)

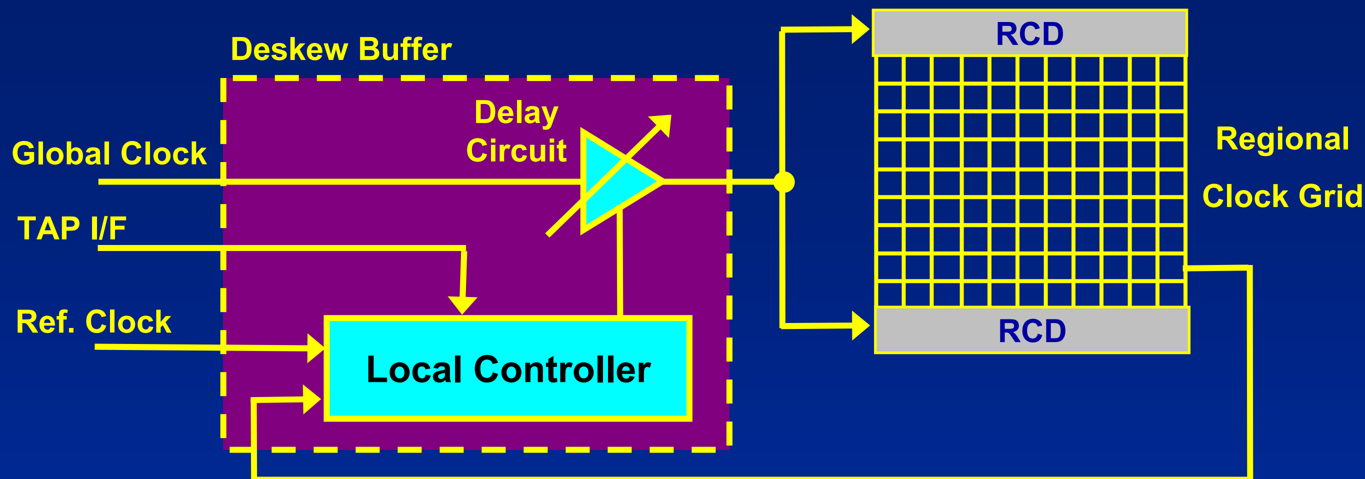
- Programmable Delay Buffer:



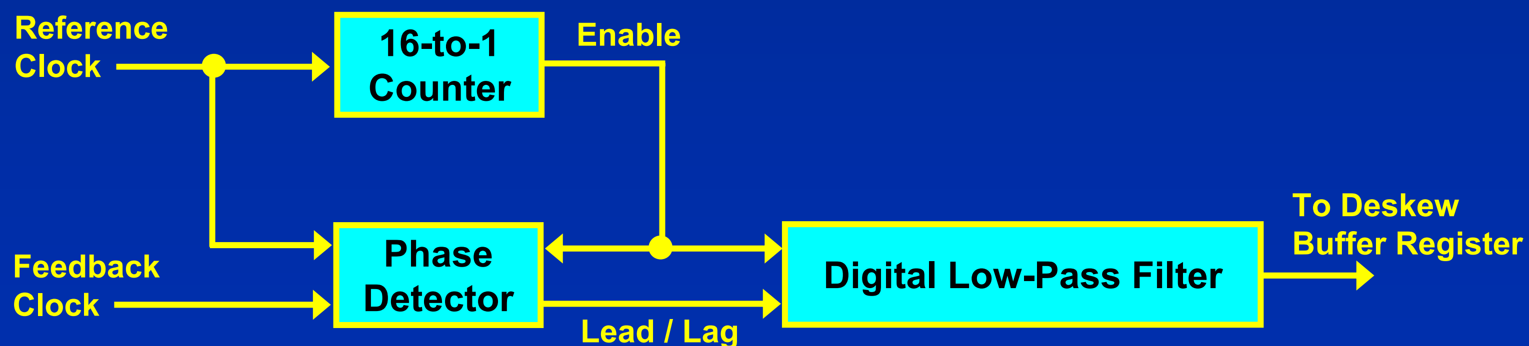
N.A. Kurd, J.S. Barkatullah, R.O. Dizon, T.D. Fletcher, P.D. Madland, "A Multigigahertz Clocking Scheme for the Pentium® 4 Microprocessor", IEEE J. of Solid State Circuits, Vol. 36, No. 11, Nov. 2001, pp. 1647-1653.

DSK Example: Itanium® - 1st gen

❑ DSK architecture:



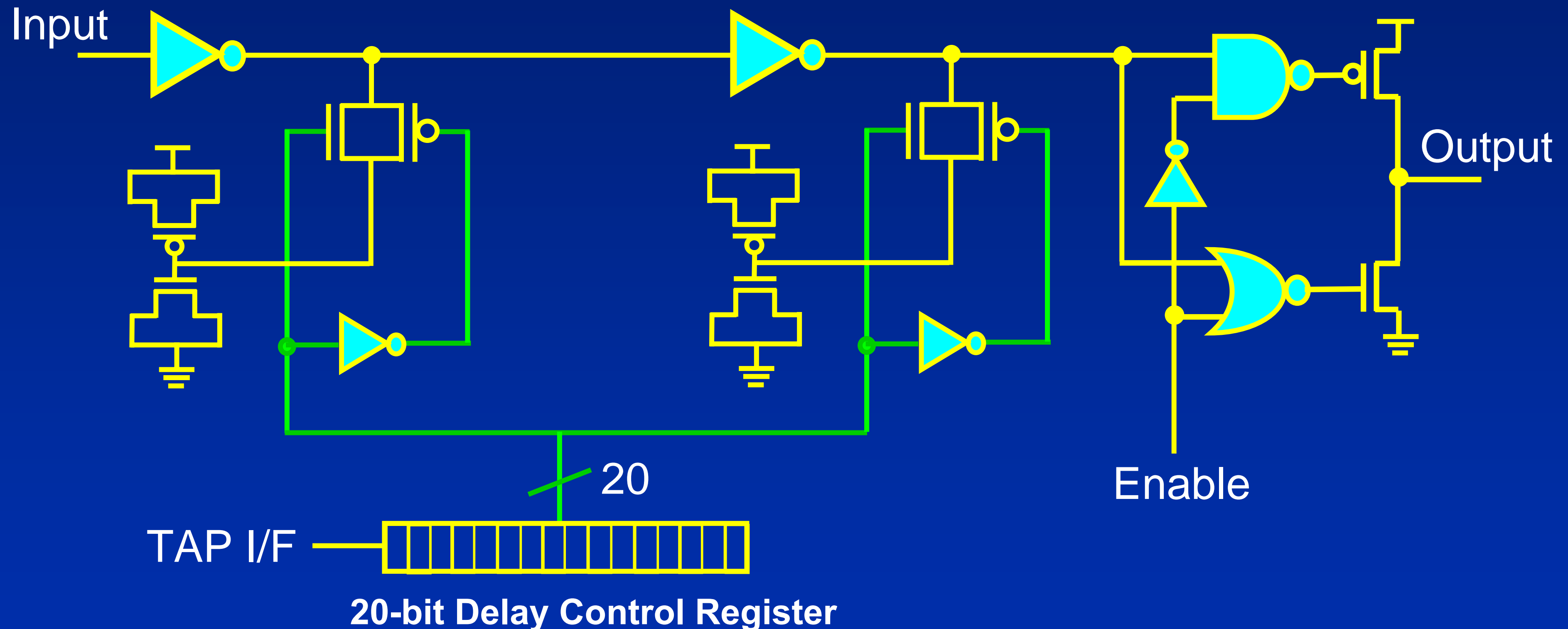
❑ DSK local controller:



S. Tam, S. Rusu, U.N. Desai, R. Kim, J. Zhang, I. Young, "Clock Generation and Distribution for the First IA-64 Microprocessor", IEEE J. of Solid-State Circuits, Vol. 35, Nov. 2000, pp. 1545-1552.

DSK Example: Itanium® - 1st gen (cnt'd)

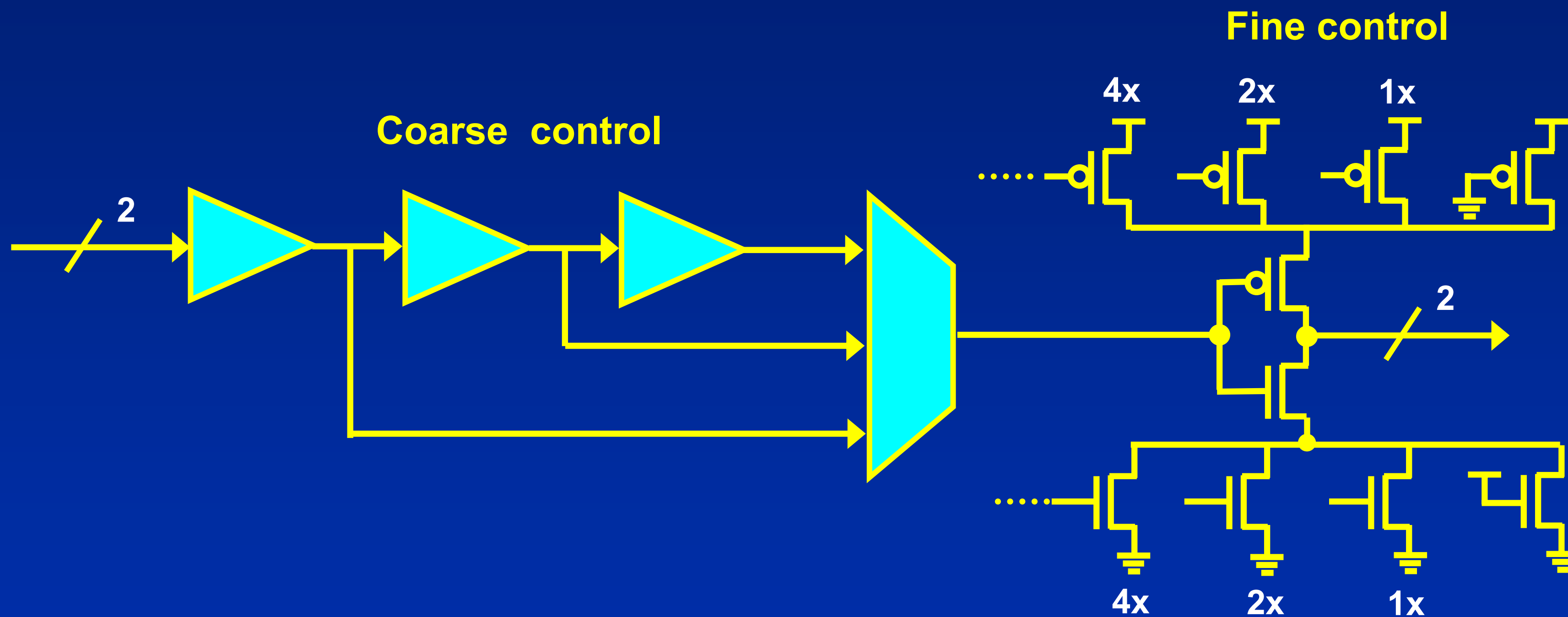
❑Variable Delay Circuit:



S. Tam, S. Rusu, U.N. Desai, R. Kim, J. Zhang, I. Young, "Clock Generation and Distribution for the First IA-64 Microprocessor", IEEE J. of Solid-State Circuits, Vol. 35, Nov. 2000, pp. 1545-1552.

DSK Example: Itanium® - 2nd gen

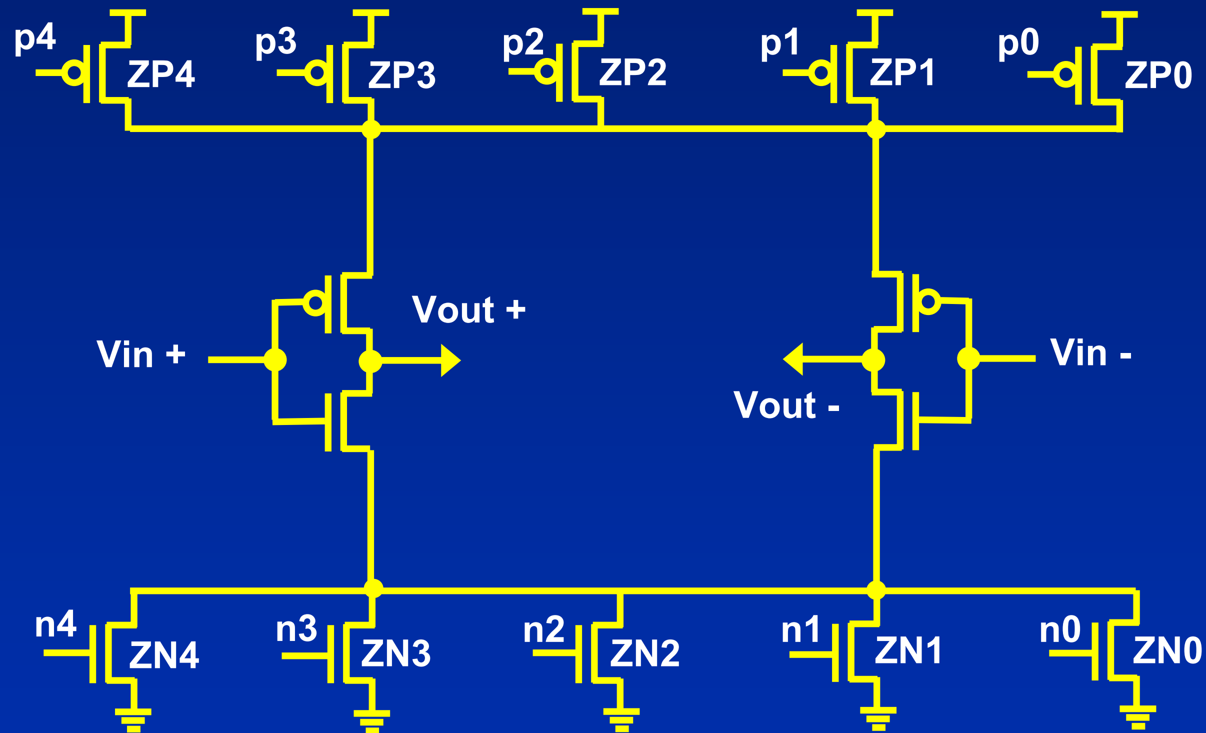
- Variable Delay Circuit:



F. E. Anderson, J. S. Wells, E. Z. Berta, "The Core Clock System on the Next-Generation Itanium™ Microprocessor", in Proc. of IEEE Int. Solid-State Circuits Conference, Digest of Technical Papers (ISSCC 2002), Vol. 2, 2002, pp. 110 – 424.

DSK Example: Itanium® - 3rd gen

- Variable Delay Circuit (for fine delay adjustment):



S. Tam, R. Limaye, U. Desai, "Clock Generation and Distribution for the 130-nm Itanium 2 Processor® with 6-MB On-Die L3 Cache", IEEE J. of Solid-State Circuits, Vol. 39, No. 4, April 2004, pp. 636-642.

Attempts at Clock Correctness

- **DeSKew strategies** intended to compensate **skew** (mainly due to parameter variations) at the **global clock level**

But are parameter variations the only attempt at clock signal correctness ?

Or can clock signals get also (directly/indirectly) involved by faults occurring during fabrication, or in the field ?

And how this will change with technology scaling ?

Can Clock Signals Get Directly Involved by Faults ?

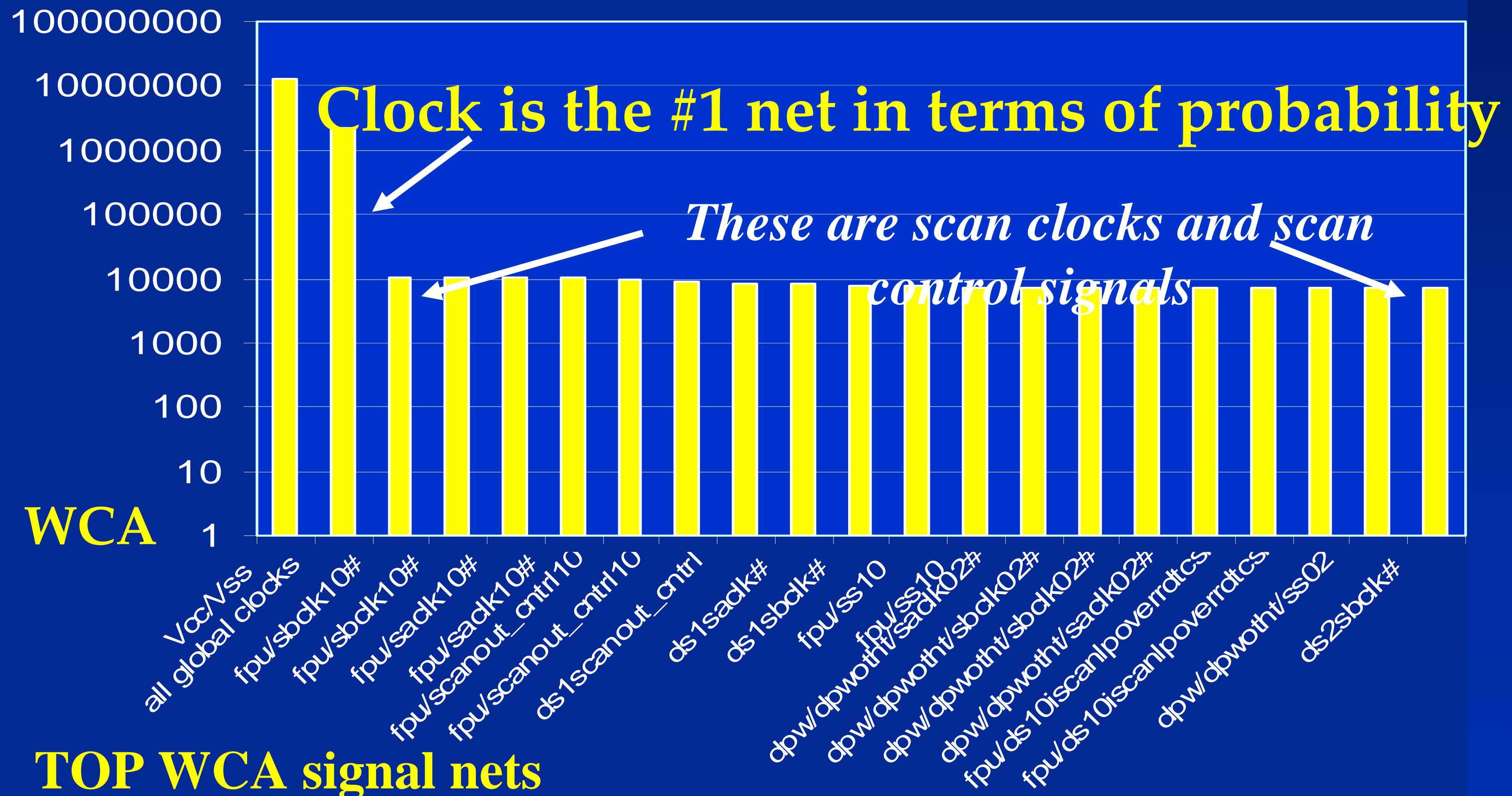
- Inductive Fault Analysis (IFA) performed on the *Intel® Itanium®* microprocessor proved [1] that:

  - after the most likely Vcc-Vss bridging fault (BF),

BFs directly involving a *CK* signal and Vcc (or Vss) are the most likely !

[1] C. Metra, S. Di Francescantonio, TM Mak, "Implications of Clock Distribution Faults and Issues with Screening Them during Manufacturing Testing," IEEE Trans. on Computers, Vol. 53, No. 5, May 2004, pp. 531-546.

Can Clock Signals Get Directly Involved by Faults ? (cnt'd)



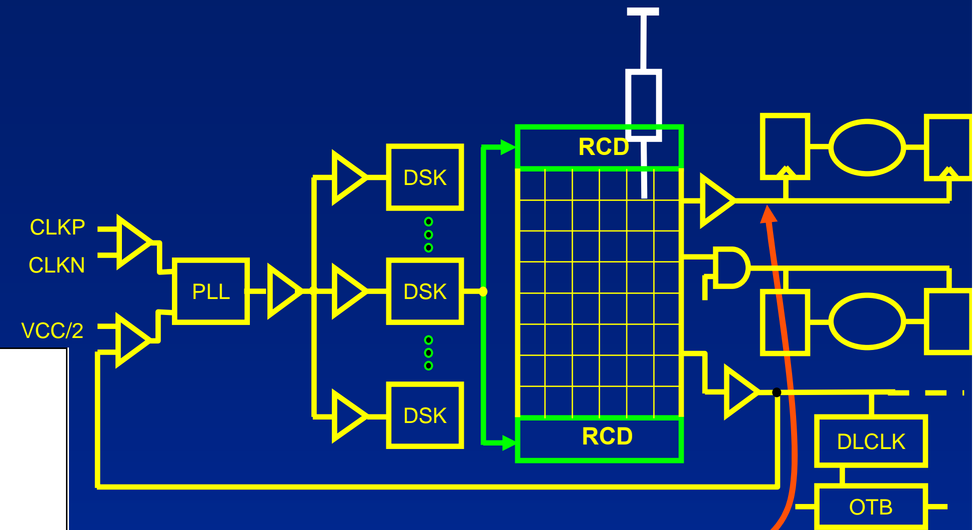
C. Metra, S. Di Francescantonio, TM Mak, "Implications of Clock Distribution Faults and Issues with Screening Them during Manufacturing Testing," IEEE Trans. on Computers, Vol. 53, No. 5, May 2004, pp. 531-546.

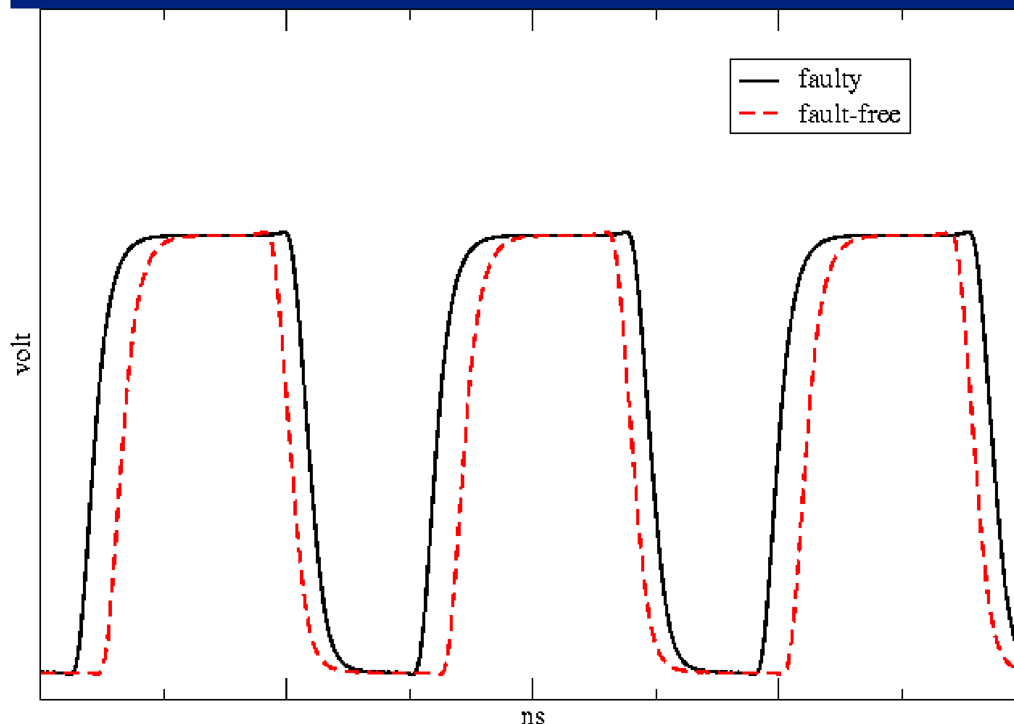
Can Clock Signals Get Directly Involved by Faults ? (cnt'd)

- **Electrical level simulations of the *Itanium*® clock distribution network, with BFs emulated by resistances in the [0-10kΩ] range, proved [1] that:**
  - **the most likely effects of clock faults are the occurrence of *duty cycle variations* which can occur also at the *local clock level***

[1] C. Metra, S. Di Francescantonio, TM Mak, "Implications of Clock Distribution Faults and Issues with Screening Them during Manufacturing Testing," IEEE Trans. on Computers, Vol. 53, No. 5, May 2004, pp. 531-546.

Can Clock Signals Get Directly Involved by Faults ? (cnt'd)





Voltages at a leaf of the clock tree with a 50 Ω BF to Vcc

duty cycle variation at the local clock level!

C. Metra, S. Di Francescantonio, TM Mak, "Implications of Clock Distribution Faults and Issues with Screening Them during Manufacturing Testing," IEEE Trans. on Computers, Vol. 53, No. 5, May 2004, pp. 531-546.

Can Clock Signals Get Directly Involved by Faults ? (cnt'd)

- Clock signals can also get directly involved by faults [1]
- Such clock faults:
  - are orders of magnitude more likely than other faults [1]
  - may produce effects observable only at a local level [1]
  - are likely to result in duty-cycle variations [1]
  - will be increasingly more likely with technology scaling
- If not screened out or compensated, such faults might compromise the correct operation of the microprocessor in the field

[1] C. Metra, S. Di Francescantonio, TM Mak, "Implications of Clock Distribution Faults and Issues with Screening Them during Manufacturing Testing," IEEE Trans. on Computers, Vol. 53, No. 5, May 2004, pp. 531-546.

Can Clock Signals Get Indirectly Involved by Faults ?

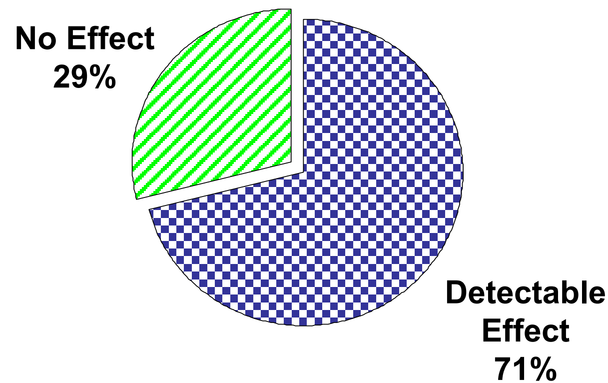
- Electrical level simulations of the *Pentium 4®* microprocessor adjustable delay clock buffers [2] with injected:
  - transistor stuck-ons (SONs),
  - transistor stuck-opens (SOPs),
  - node stuck-ats (SAs),
  - BFs (R in the [0-6kΩ] range)

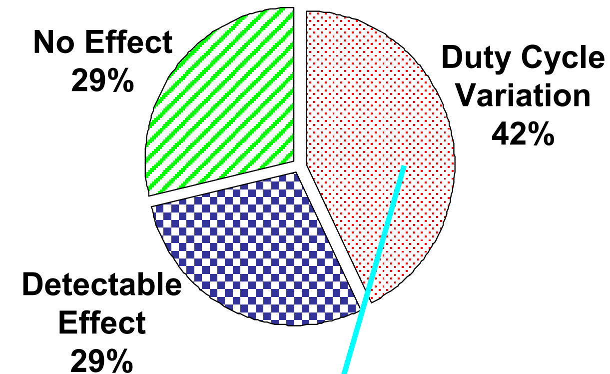
proved that:

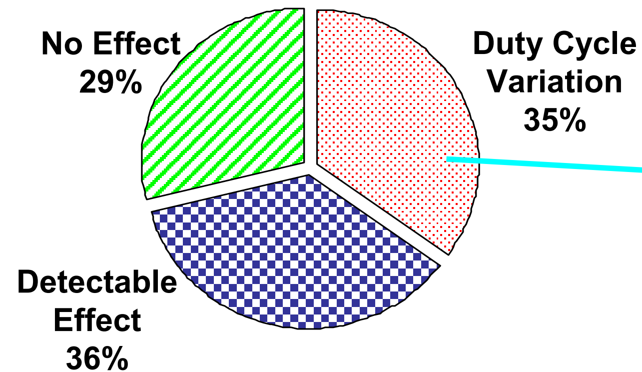
- such faults are very likely to result in output clocks with incorrect duty-cycle [2].

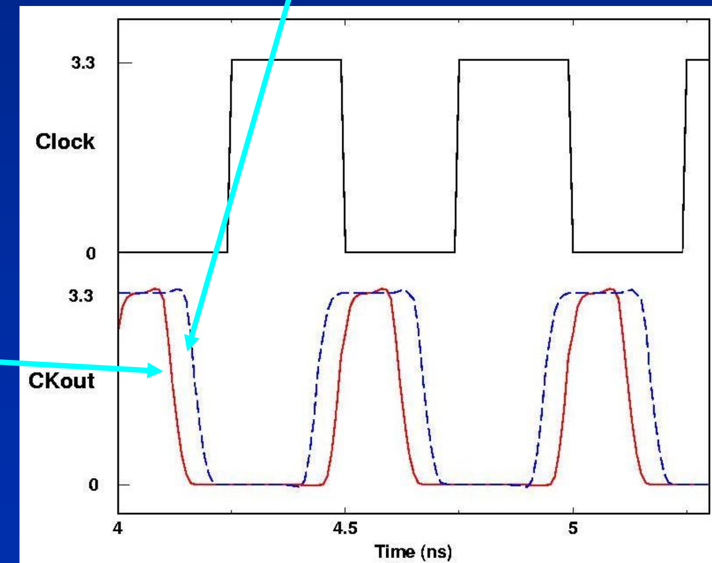
[2] C. Metra, D. Rossi, TM Mak, "Won't On-Chip Clock Calibration Guarantee Performance Boost and Product Quality?", IEEE Trans. on Computers, Vol. 56, No. 3, March, 2007, pp. 415-428.

Effects of Faults Affecting Clock Buffers



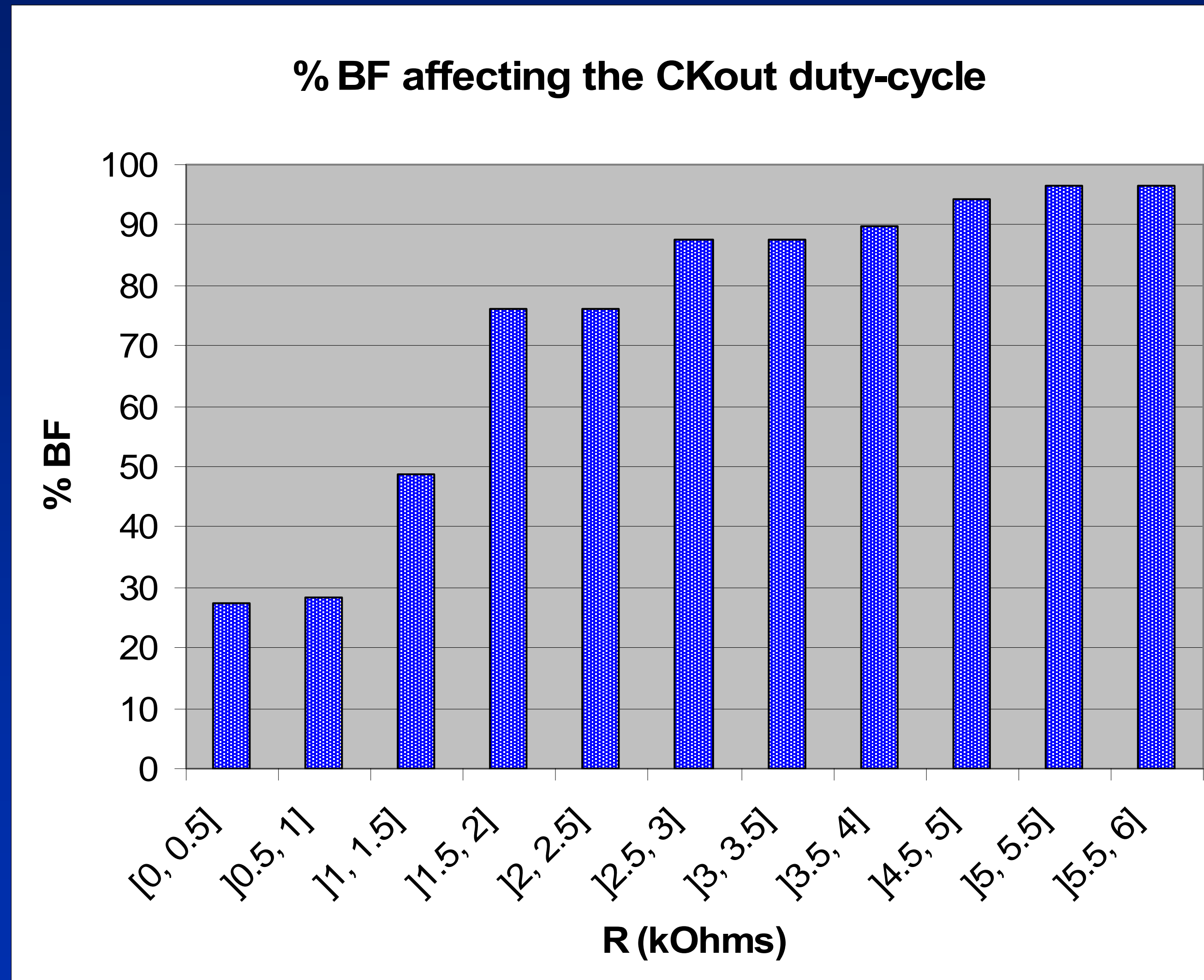






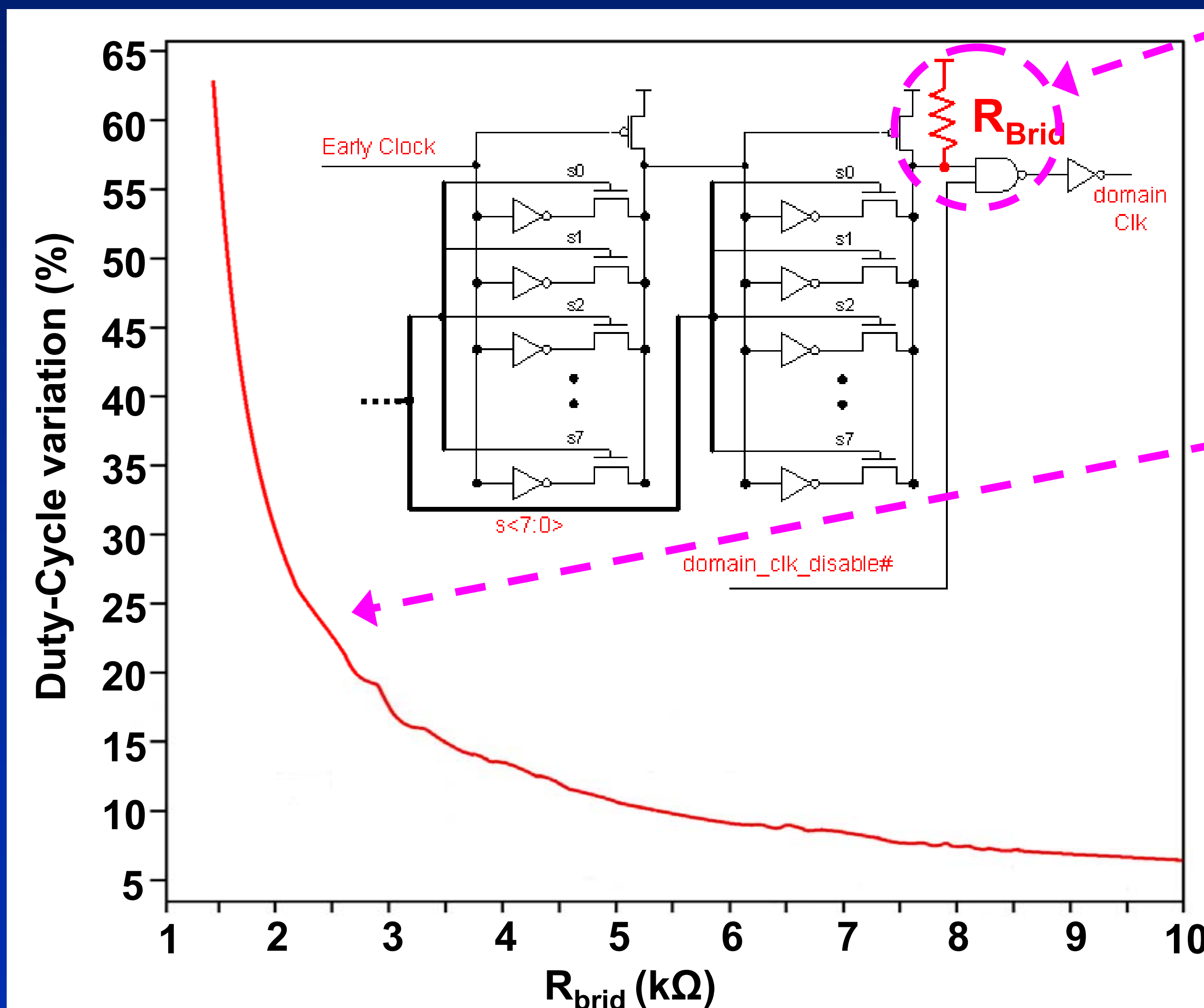
C. Metra, D. Rossi, TM Mak, "Won't On-Chip Clock Calibration Guarantee Performance Boost and Product Quality?", IEEE Trans. on Computers, Vol. 56, No. 3, March, 2007, pp. 415-428.

Effects of Faults Affecting Clock Buffers (cnt'd)



C. Metra, D. Rossi, TM Mak, "Won't On-Chip Clock Calibration Guarantee Performance Boost and Product Quality?", IEEE Trans. on Computers, Vol. 56, No. 3, March, 2007, pp. 415-428.

Produced Duty-Cycle Variations Can be Significant

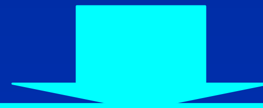


- Example of a BF between **Vcc** and the **buffer output.**
- **High duty-cycle variations** for values of **connecting resistance ≤ 4kΩ!**

C. Metra, D. Rossi, TM Mak, "Won't On-Chip Clock Calibration Guarantee Performance Boost and Product Quality?", IEEE Trans. on Computers, Vol. 56, No. 3, March, 2007, pp. 415-428.

Can Clock Signals Get Indirectly Involved by Faults ? (cnt'd)

- Clock signals can also get indirectly involved by faults (which directly affect clock buffers) [2]
- Such clock faults:
  - are likely to result in duty-cycle variations, which can be very significant [2]
  - will be increasingly more likely with technology scaling
- If not screened out or compensated, such faults might compromise the correct operation of the microprocessor in the field



Dependability Risks !

[2] C. Metra, D. Rossi, TM Mak, "Won't On-Chip Clock Calibration Guarantee Performance Boost and Product Quality?", IEEE Trans. on Computers, Vol. 56, No. 3, March, 2007, pp. 415-428.

Clock Faults' Due Dependability Risks: Solutions ?

Can clock faults be screened out through manufacturing (structural or functional) testing ?

Or can their effect be compensated?

Can Clock Faults Be Tested Out ?

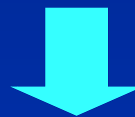
- Generally, **no specific testing** procedure is adopted for clock faults
- However, **can clock faults be indirectly detected** during manufacturing testing (*e.g.*, **structural or functional testing) ?**
  - It has been verified that clock fault indirect detection through
    - **structural testing is not likely [1]**
    - **functional testing is not likely [3]**

[1] C. Metra, S. Di Francescantonio, TM Mak, "Implications of Clock Distribution Faults and Issues with Screening Them during Manufacturing Testing," IEEE Trans. on Computers, Vol. 53, No. 5, May 2004, pp. 531-546.

[3] C. Metra, D. Rossi, M. Omaña, J.M. Cazeaux, TM Mak, "Can Clock Faults Be Detected Through Functional Test ?", Proc. of IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems (DDECS'06), pp. 168—173, 2006.

Can Clock Faults Be Tested Out ? (cnt'd)

- **Detecting clock faults through structural testing is not likely [1]:**
  - **depending on the structural test technique, anywhere between 59% and up to 88% of possible clock faulty conditions may be not detected.**



Inability of Structural Testing to Guarantee Clock Faults' Detection

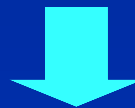
[1] C. Metra, S. Di Francescantonio, TM Mak, "Implications of Clock Distribution Faults and Issues with Screening Them during Manufacturing Testing," IEEE Trans. on Computers, Vol. 53, No. 5, May 2004, pp. 531-546.

Can Clock Faults Be Tested Out ? (cnt'd)

- Detecting clock faults through **functional testing** is not likely [3]:
  - Results for all long/short paths **of 10 considered ISCAS'85 benchmarks**

$$AvP_{det} = \sum \frac{P_{det}(i)}{n} \qquad i = 1, 2, \ldots, n = 10$$

Mod(Δ_{DC} %)	10%	20%	30%	40%	50%
$AvP_{det\text{-}sp}$	23 %	33 %	43 %	44 %	44 %
$AvP_{det\text{-}lp}$	24 %	27 %	33 %	34 %	35 %



Inability of Functional Testing to Guarantee Clock Faults' Detection

[3] C. Metra, D. Rossi, M. Omaña, J.M. Cazeaux, TM Mak, "Can Clock Faults Be Detected Through Functional Test ?", Proc. of IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems (DDECS'06), pp. 168—173, 2006.

Clock Faults' Due Dependability Risks: Solutions ?

Can clock faults be screened out through manufacturing (structural or functional) testing ?

No guarantee

Or can their effect be compensated?

Can CKF Effect Be Compensated ?

- Compensation schemes are intended to compensate skew mainly due to parameter variations at the global clock level
- CKFs' most likely effect is to produce duty cycle variations, which:
  - can be very significant
  - can occur also at the local level only
- Compensation schemes could be modified to deal with CK faults, but

their cost would be very high

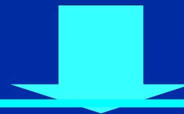
Clock Faults' Due Dependability Risks: Solutions ?

Can clock faults be screened out through manufacturing (structural or functional) testing ?

No guarantee

Or can their effect be compensated?

NO (unless high cost)



Need for Testing Approaches and/or Correction Schemes to Increase Dependability at Affordable Costs

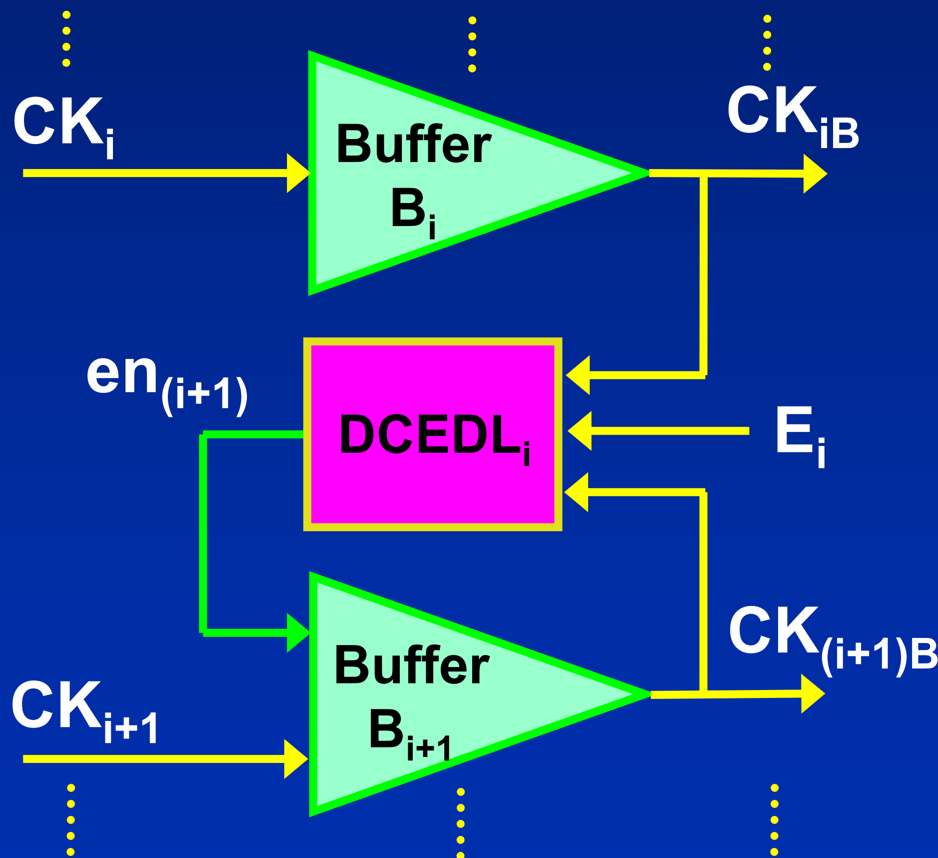
Example of
Low Cost Testing Approach for Clock Faults

- It has been proposed [4]:
  - to make CFs' most likely effects (i.e., duty-cycle variations) result in clock stuck-at faults (S@) →
  - catastrophic effects →
  - easy detection through conventional manufacturing test

[4] C. Metra, M. Omaña, TM. Mak, S. Tam, "Novel Approach to Clock Fault Testing for High Performance Microprocessors", in IEEE Proc. VLSI Test Symposium, 2007, pp. 441-446.

Possible Hardware Implementation

- Insertion of Duty-Cycle Error Detect and Latch blocks ($DCEDL_i$) among physically adjacent (local and global) CK buffers.

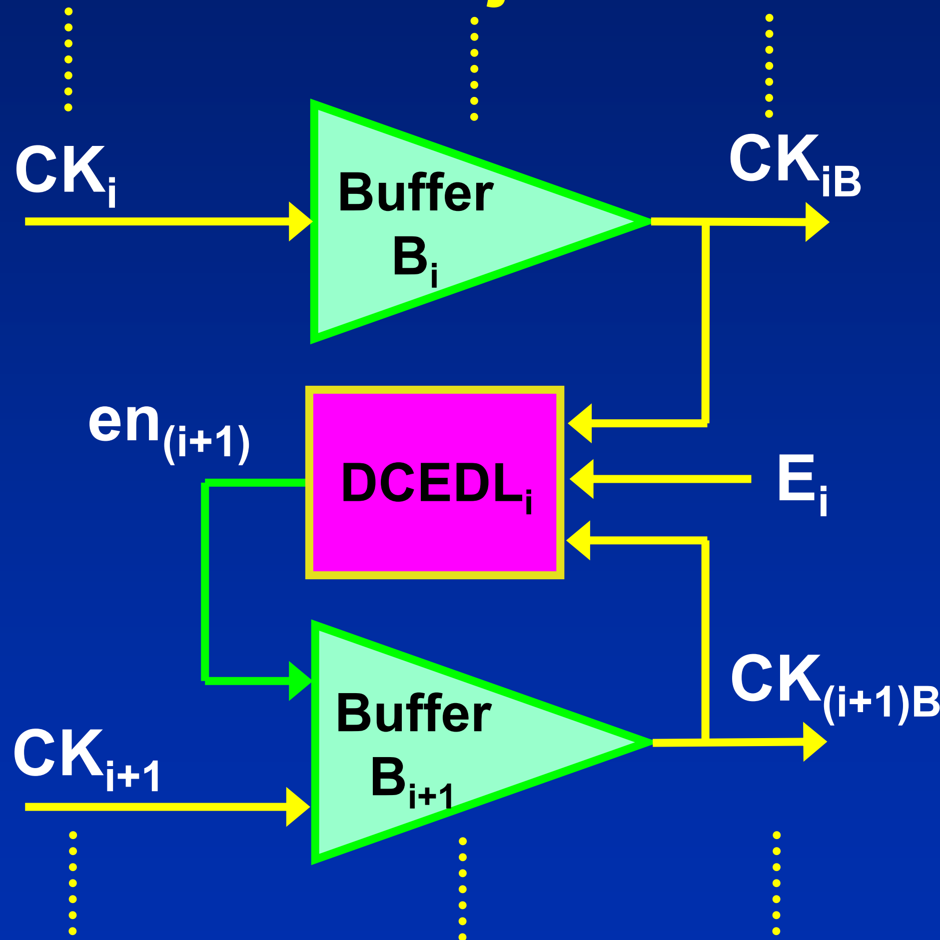


- Each $DCEDL_i$:
  - checks the outputs of 2 adjacent clock buffers;
  - gives the enable signal for one of such clock buffers.
- All $DCEDL_i$ disabled (E_i=0) during μP normal operation.

C. Metra, M. Omaña, TM. Mak, S. Tam, "Novel Approach to Clock Fault Testing for High Performance Microprocessors", in IEEE Proc. VLSI Test Symposium, 2007, pp. 441-446.

Possible Hardware Implementation (cnt'd)

- Duty-Cycle Error Detect and Latch blocks ($DCEDL_i$) between adjacent clock buffers.

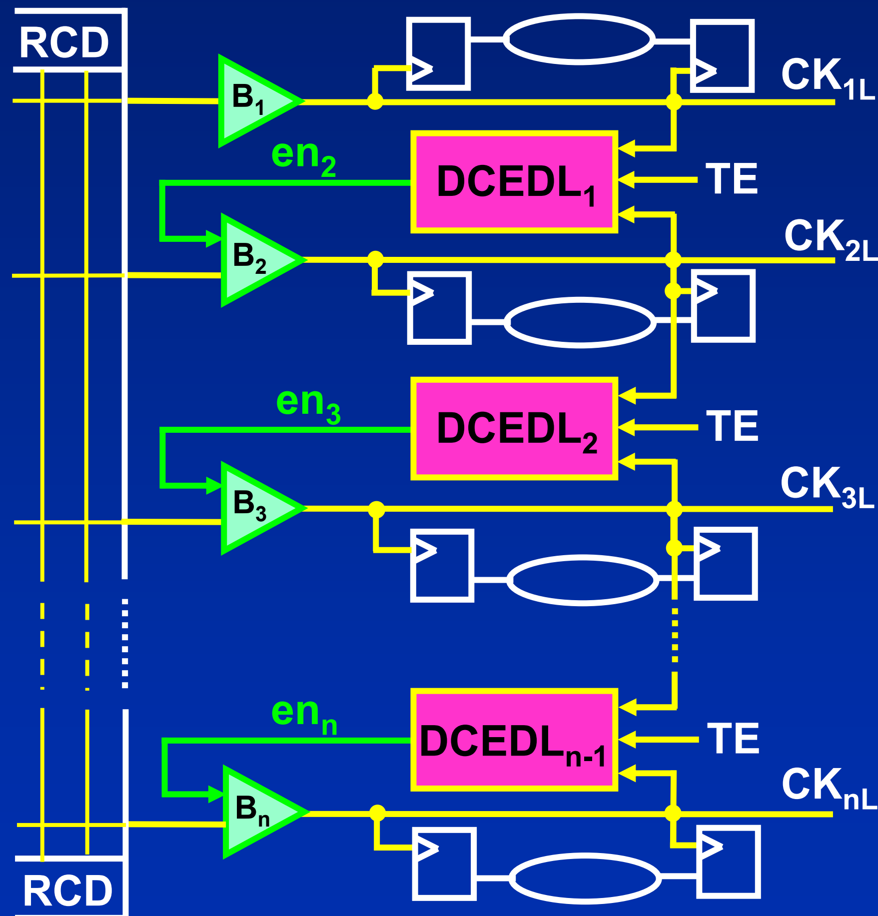


- $DCEDL_i$ enabled (E_i=1) during μP testing:
  - if $CK_{iB} \neq CK_{(i+1)B}$ → $en_{(i+1)}$=0 → buffer B_{i+1} disabled → $CK_{(i+1)B}$ S@0 → easy detection;
  - if $CK_{iB} = CK_{(i+1)B}$ $en_{(i+1)}$=1→ buffer B_{i+1} enabled → no effect.

C. Metra, M. Omaña, TM. Mak, S. Tam, "Novel Approach to Clock Fault Testing for High Performance Microprocessors", in IEEE Proc. VLSI Test Symposium, 2007, pp. 441-446.

Application to Local Buffers: Pentium®4 Example

- Approach **synergetic** with **local CK distribution** → **no routing problems.**



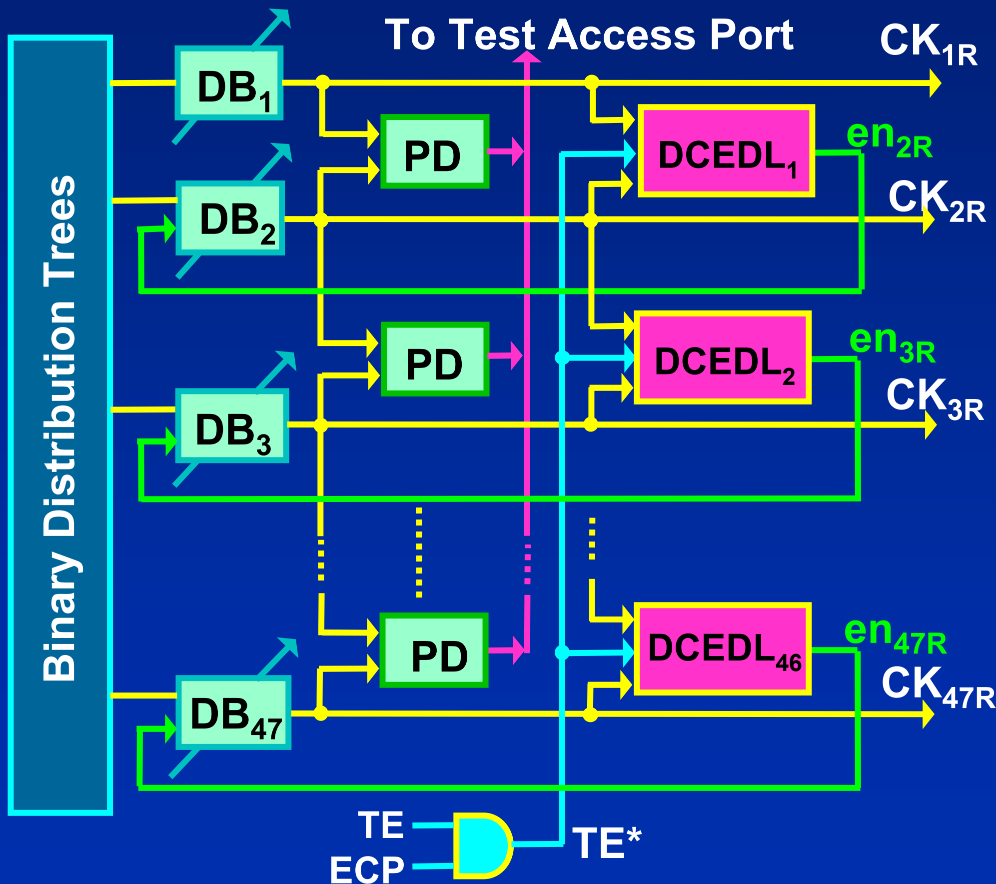
- **TE connected** to E_i of each $DCEDL_i$ →
- When **TE=1** → en_i generated in a **ripple fashion** → **S@0** on **all CKs** physically located **among** the **faulty** one and the **last** one.

***CF* easy detection through conventional manufacturing test.**

C. Metra, M. Omaña, TM. Mak, S. Tam, "Novel Approach to Clock Fault Testing for High Performance Microprocessors", in IEEE Proc. VLSI Test Symposium, 2007, pp. 441-446.

Application to Global Buffers: Pentium®4 Example

- Approach synergetic with global CK distribution → no routing problems.



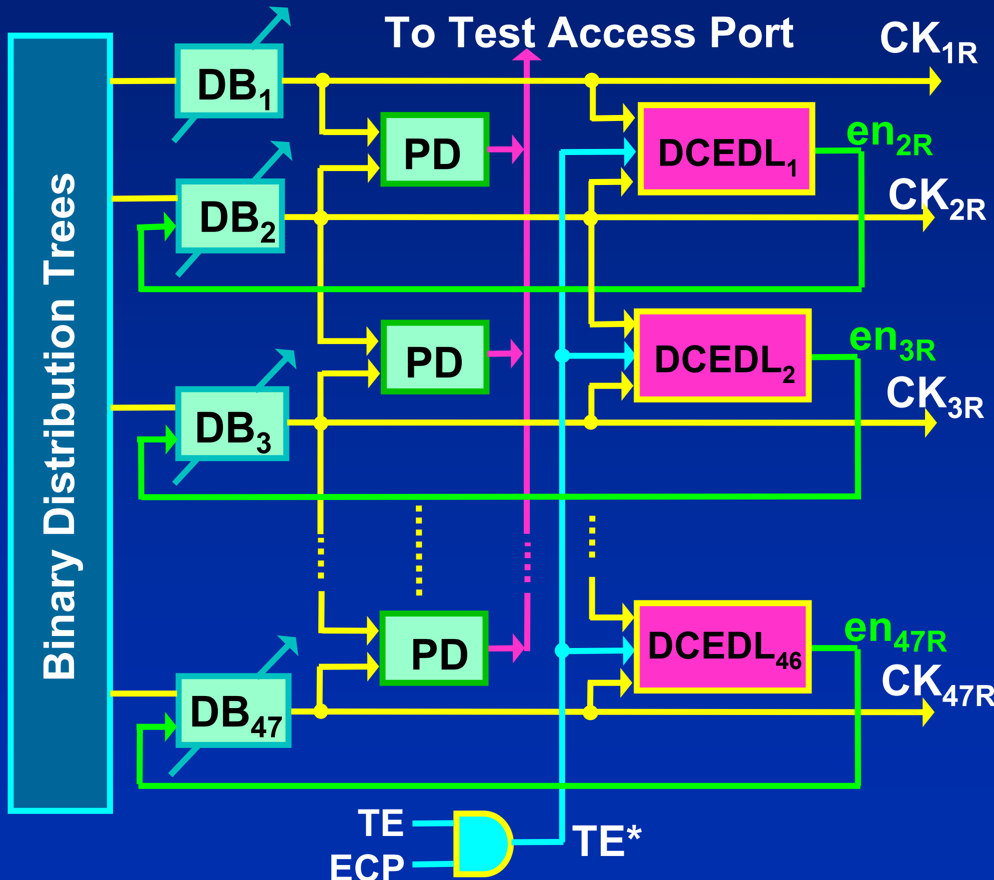
- Scheme activated after calibration (ECP=1) → detection of *CFs*, after parameter variation compensation.

- Signal TE* =AND(TE, ECP) connected to the enable terminals (E_i) of the DCEDLs.

C. Metra, M. Omaña, TM. Mak, S. Tam, "Novel Approach to Clock Fault Testing for High Performance Microprocessors", in IEEE Proc. VLSI Test Symposium, 2007, pp. 441-446.

Application to Global Buffers: Pentium®4 Example (cnt'd)

- Approach synergetic with global CK distribution → no routing problems.



- When TE*=1 → en_{iR} generated in a ripple fashion → S@0 on all CKs physically located among the faulty one and the last one.

CK fault easy detection through conventional manufacturing test

C. Metra, M. Omaña, TM. Mak, S. Tam, "Novel Approach to Clock Fault Testing for High Performance Microprocessors", in IEEE Proc. VLSI Test Symposium, 2007, pp. 441-446.

Example of Low Cost Correction Scheme for Clock Faults

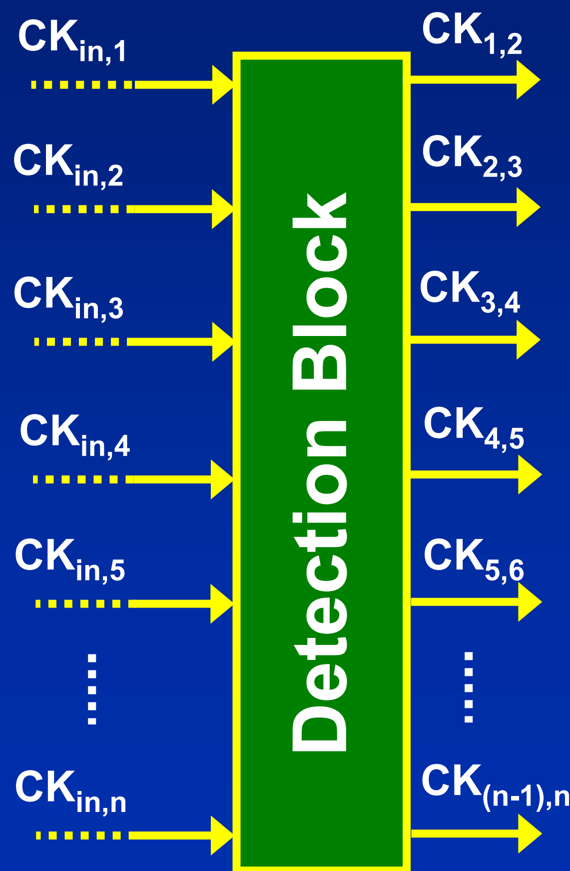
- Proposal of a scheme [5] capable of:
  - detecting mismatches between couples of physically adjacent local CKs and giving:
    i. a high impedance state output, in case of mismatch;
    ii. the logic value present on one of the two input clock signals, in case of matching.

[5] C. Metra, M. Omaña, TM. Mak, S. Tam, "Novel Compensation Scheme for Local Clocks of High Performance Microprocessors", in IEEE Proc. of the IEEE Int. Test Conference, 2007, pp. 1-9.

Correction Scheme: Component Blocks

- **Scheme composed of 3 blocks:**

1. Detection Block

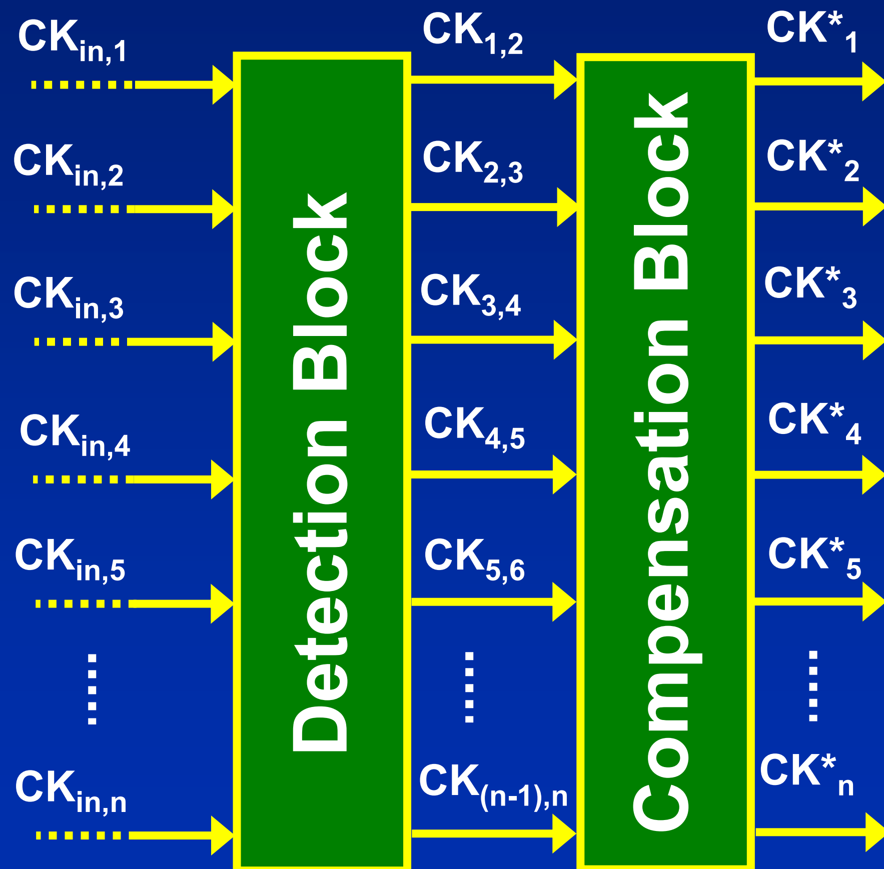


- It receives ***n* input local clocks** ($CK_{in,i}$, i=1,…, n) **to be compensated** in case of phase mismatch (i.e., duty cycle variation - ΔDC).
- It consist of ***(n-1)* sub-blocks**, each:
  - **detecting phase mismatches** between two **physical adjacent input clocks** ($CK_{in,I}$ - $CK_{in,(i+1)}$)
  - giving a **high impedance** state (Z) if the **input CKs present ΔDC.**

[5] C. Metra, M. Omaña, TM. Mak, S. Tam, "Novel Compensation Scheme for Local Clocks of High Performance Microprocessors", in IEEE Proc. of the IEEE Int. Test Conference, 2007, pp. 1-9.

Correction Scheme: Component Blocks (cnt'd)

- **Scheme composed of 3 blocks:**

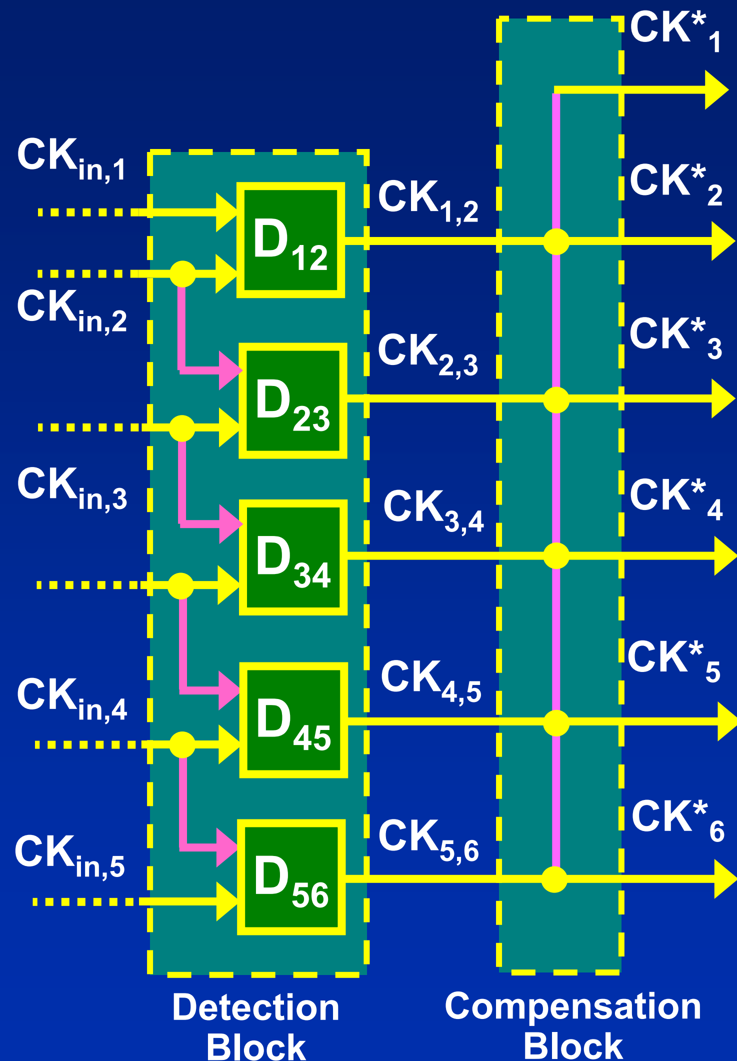


2. Compensation Block

- It **receives** the *(n-1)* **outputs** of the **Detection block** ($CK_{i,(i+1)}$, i=1,…, n-1) and **provides** n **compensated clock signals** (CK^*_i, i=1,…, n).

[5] C. Metra, M. Omaña, TM. Mak, S. Tam, "Novel Compensation Scheme for Local Clocks of High Performance Microprocessors", in IEEE Proc. of the IEEE Int. Test Conference, 2007, pp. 1-9.

Compensation Block: Possible Implementation

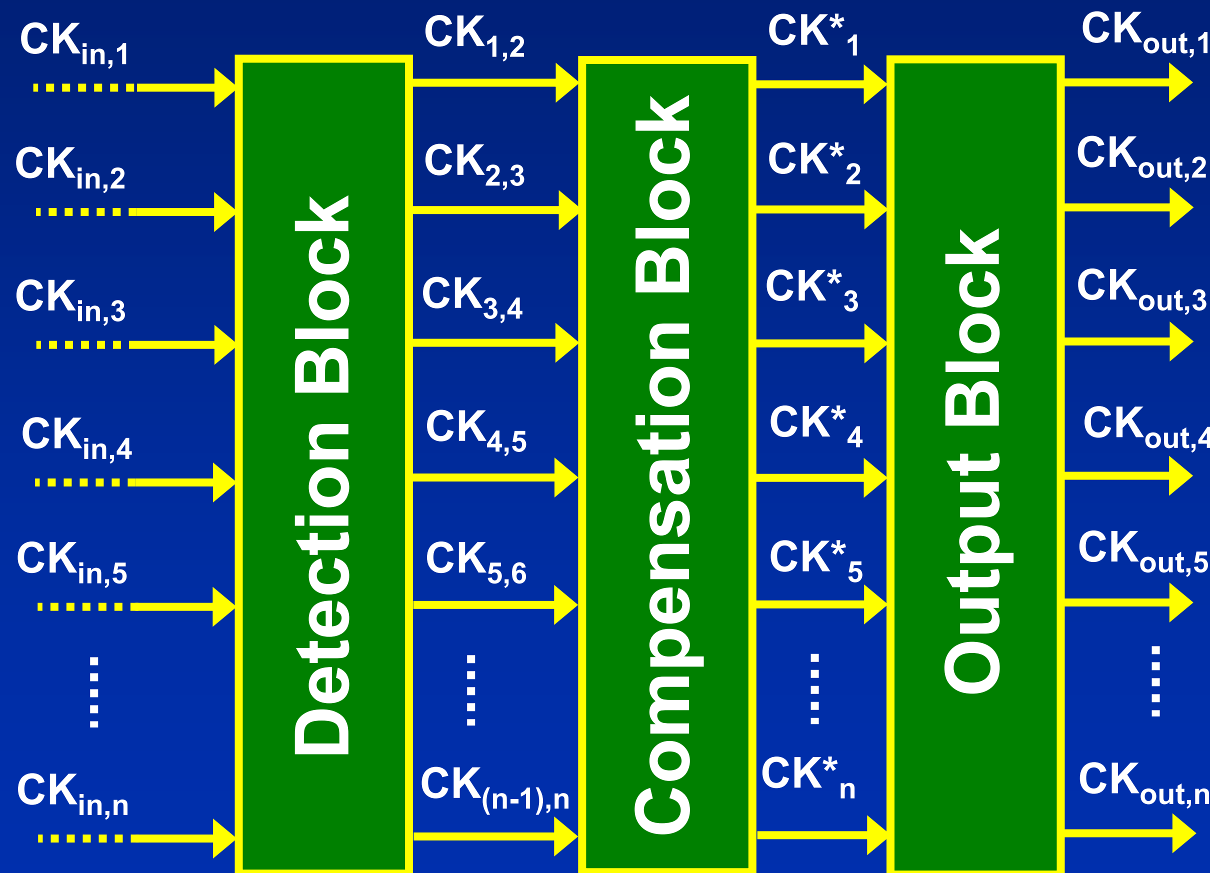


- We can simply **short together the *(n-1)* outputs** of the Detection Block.
- → the **high-Z state outputs** of the Detection Block are **forced to assume the correct logic value** imposed by the **non high-Z state outputs.**
- **No electrical conflict arises** → ***minimal power consumption and compensation time !***

[5] C. Metra, M. Omaña, TM. Mak, S. Tam, "Novel Compensation Scheme for Local Clocks of High Performance Microprocessors", in IEEE Proc. of the IEEE Int. Test Conference, 2007, pp. 1-9.

Correction Scheme: Component Blocks (cnt'd)

- Scheme composed of 3 blocks:



3. Output Block

- It **receives** the **outputs** of the **Compensation block** and **provides** properly **buffered, compensated output clocks** ($CK_{out,i}$, i=1,…, n).

[5] C. Metra, M. Omaña, TM. Mak, S. Tam, "Novel Compensation Scheme for Local Clocks of High Performance Microprocessors", in IEEE Proc. of the IEEE Int. Test Conference, 2007, pp. 1-9.

Cost Comparison

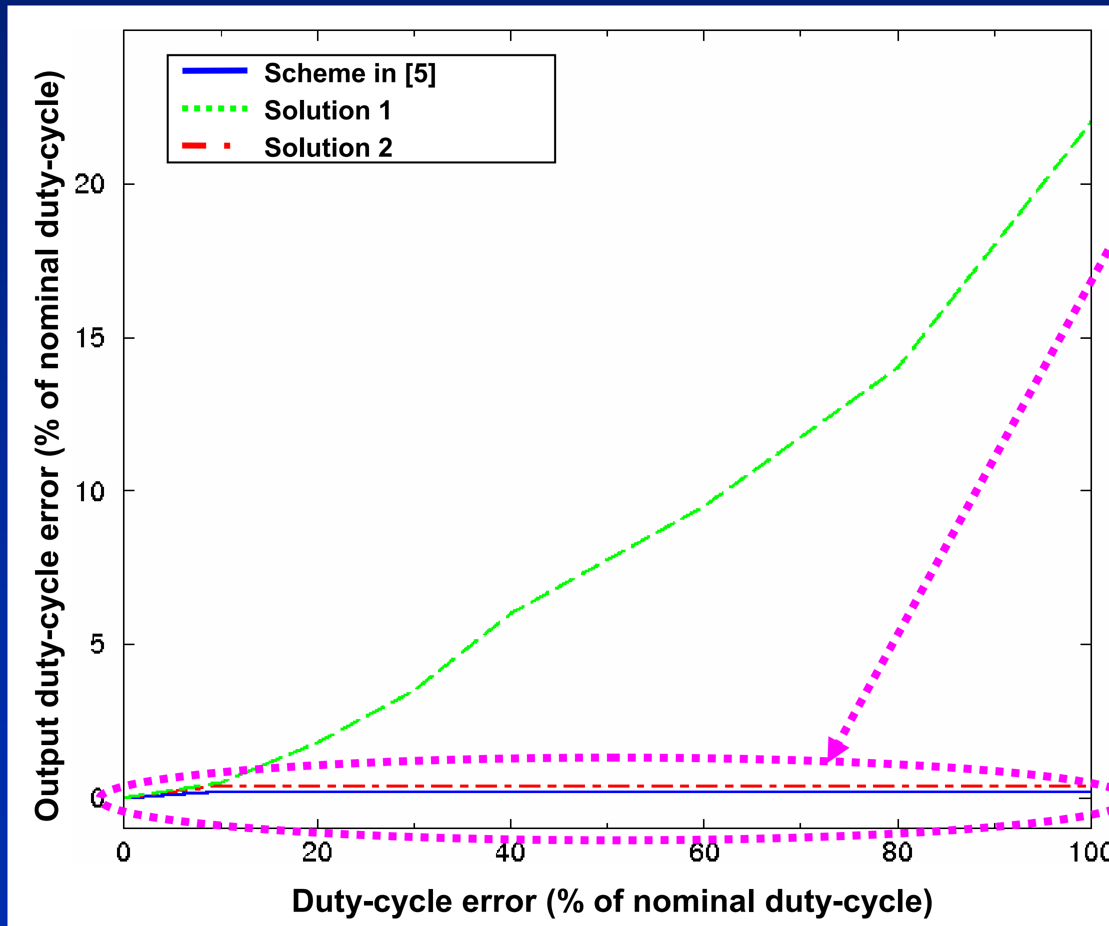
- Scheme in [5] compared with:
  - the clock compensation scheme in *[6]* *(Solution 1);*
  - the strategy that simply **shorts together** the outputs of the local clock buffers *(Solution 2).*
- Costs evaluated in terms of:
  - compensation error;
  - power consumption;
  - area overhead.

[5] C. Metra, M. Omaña, TM. Mak, S. Tam, "Novel Compensation Scheme for Local Clocks of High Performance Microprocessors", in IEEE Proc. of the IEEE Int. Test Conference, 2007, pp. 1-9.

[6] M. Omaña, D. Rossi, C. Metra, "Low Cost Scheme for On-Line Clock Skew Compensation", in Proc. of IEEE VLSI Test Symposium, pp. 90-95, 2005.

Cost Comparison: Compensation Error

- **Case 1:** for all schemes it has been considered that **1 out of 16 input CKs** presents a **ΔDC between 0% and 100%** of its nominal value (50% of T_{CK}).

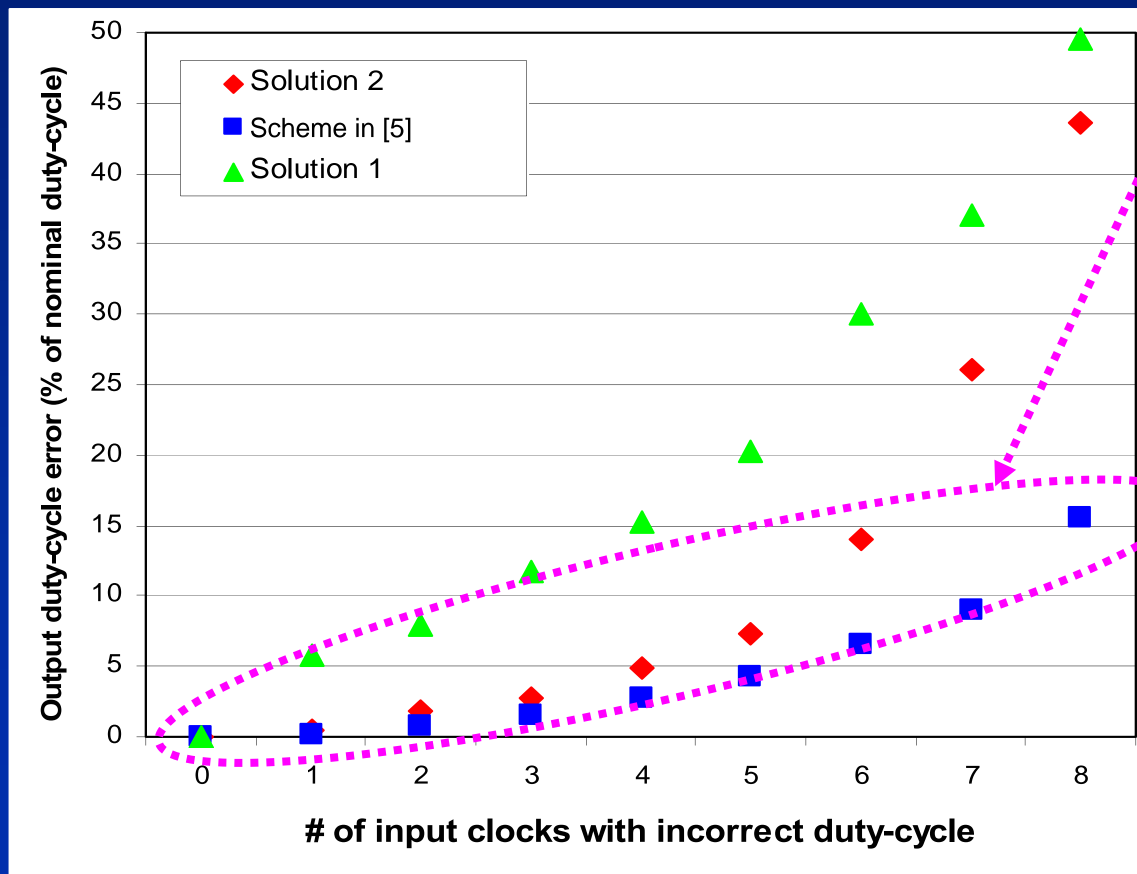


- **The scheme in [5]** & **solution 2** present a considerable **low compensation error** (0.2% and 0.4%, respectively) **that does not change** with the magnitude of **ΔDC.**

[5] C. Metra, M. Omaña, TM. Mak, S. Tam, "Novel Compensation Scheme for Local Clocks of High Performance Microprocessors", in IEEE Proc. of the IEEE Int. Test Conference, 2007, pp. 1-9.

Cost Comparison: Compensation Error (cntd)

- **Case 2: compensation error as a function of the # of incorrect input CKs (= among them and with a ΔDC of 40% of its nominal value).**

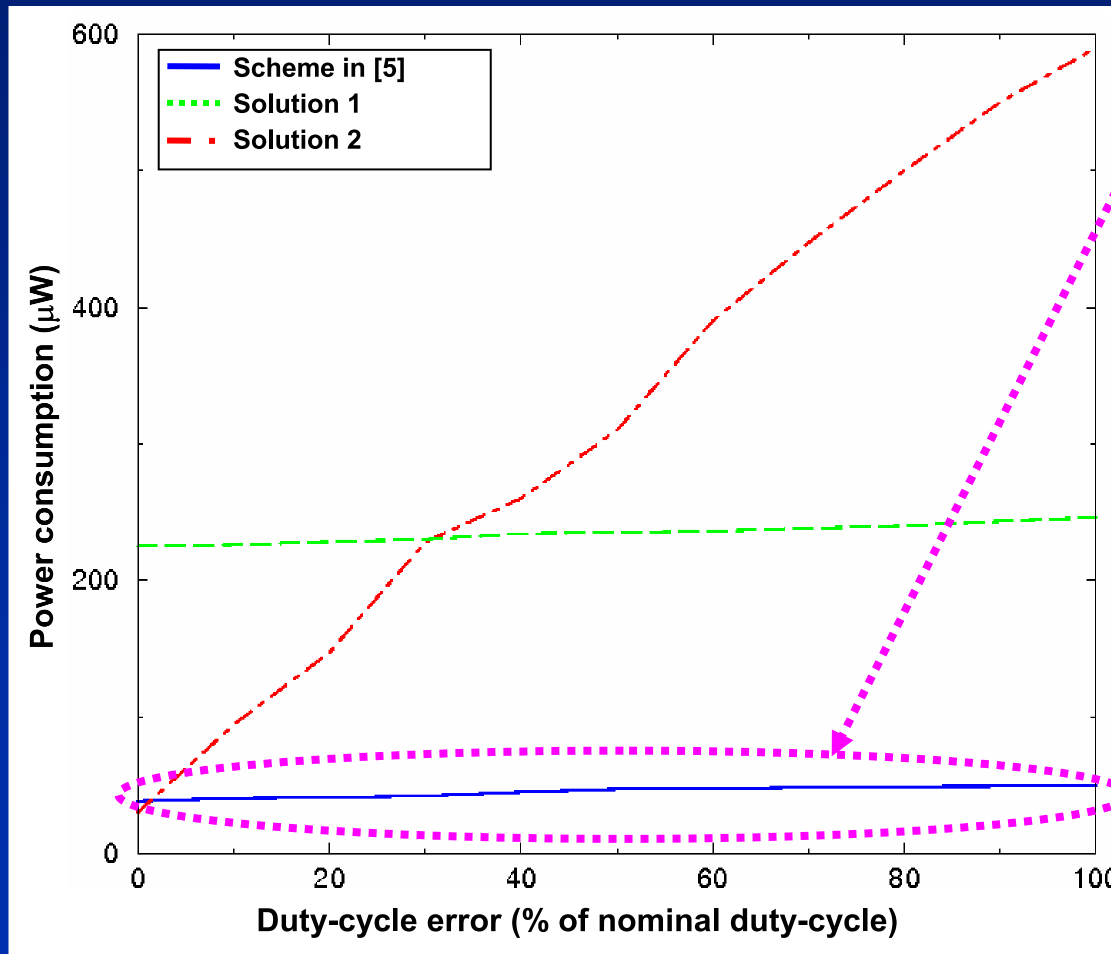


- **The scheme in [5] presents the lowest compensation error, with a reduction >69% compared to solution 1 and >40% compared to solution 2.**

[5] C. Metra, M. Omaña, TM. Mak, S. Tam, "Novel Compensation Scheme for Local Clocks of High Performance Microprocessors", in IEEE Proc. of the IEEE Int. Test Conference, 2007, pp. 1-9.

Cost Comparison: Power Consumption

- Power consumed by the 3 considered solutions as a function of ΔDC.

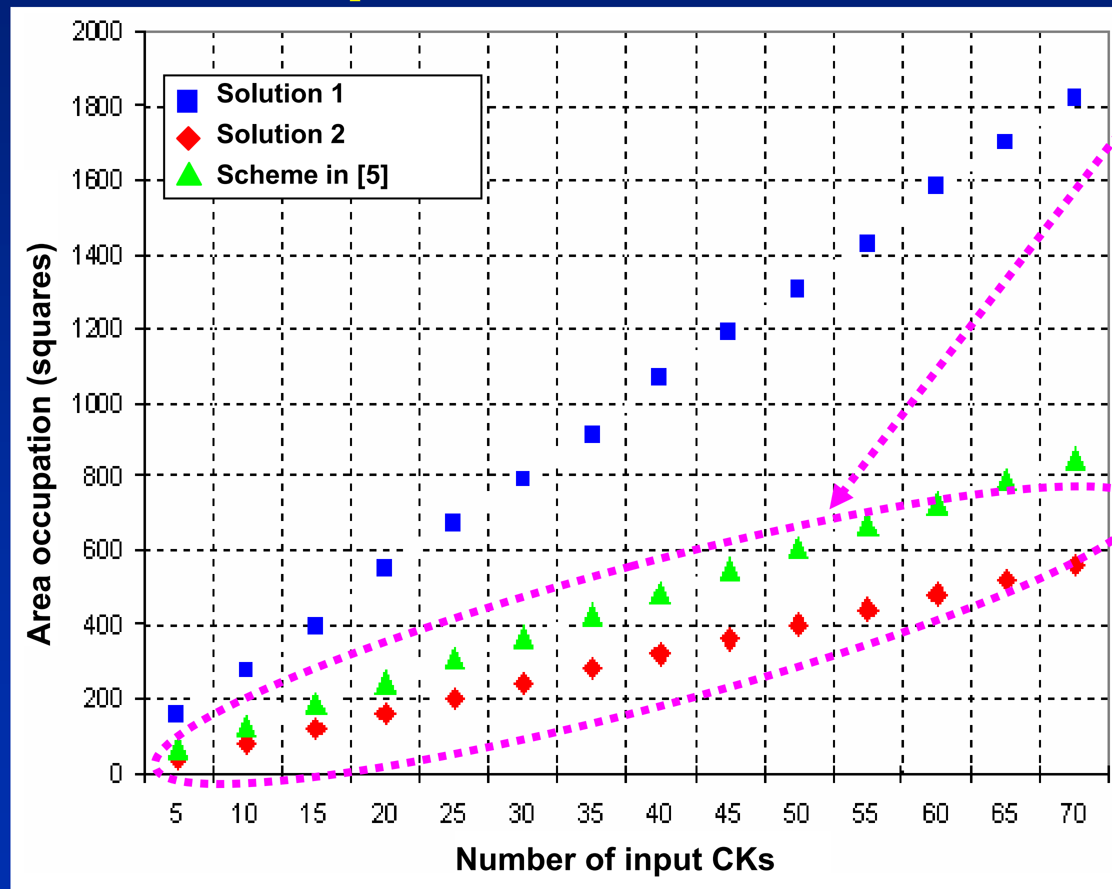


- Due to the avoidance of electrical conflicts during compensation, the power consumed by the scheme in [5] is approx. constant (~ 40µW) with ΔDC.

[5] C. Metra, M. Omaña, TM. Mak, S. Tam, "Novel Compensation Scheme for Local Clocks of High Performance Microprocessors", in IEEE Proc. of the IEEE Int. Test Conference, 2007, pp. 1-9.

Cost Comparison: Area Overhead

- **Area** (expressed in squares) of the 3 considered solutions **as a function of the # of input clocks to be compensated.**



- The **area of the scheme in [5] slightly increases** with respect to that of the **solution 2.** However, **such an increase** can be considered **negligible when** the **total chip area is accounted.**

[5] C. Metra, M. Omaña, TM. Mak, S. Tam, "Novel Compensation Scheme for Local Clocks of High Performance Microprocessors", in IEEE Proc. of the IEEE Int. Test Conference, 2007, pp. 1-9.

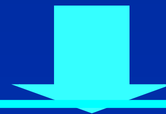
Conclusions

- Faults affecting **clock signals** are **likely** and their **likelihood will increase** with technology scaling

- They **may be not screened out during manufacturing testing**

- They **can not be compensated at low costs** by current schemes

- They **may compromise the microprocessor correct operation in the field,** with consequent **decrease in dependability**



New Testing Approaches and/or Correction Schemes are (should be) searched for increased Dependability at Affordable Costs

Trading Off Dependability and Cost for Nanoscale High Performance Microprocessors: The Clock Distribution Problem

Cecilia Metra

DEIS – University of Bologna

cecilia.metra@unibo.it