The 39th Annual IEEE/IFIP International Conference on Dependable Systems and Networks

June 29-July 2, 2009 — Estoril, Lisbon, Portugal

Third Workshop on Dependable and Secure Nanocomputing

Organizers:

- Jean Arlat, LAAS-CNRS
- Cristian Constantinescu, AMD
- Ravishankar K. Iyer, UIUC
- Johan Karlsson, Chalmers Univ.
- Michael Nicolaïdis, TIMA

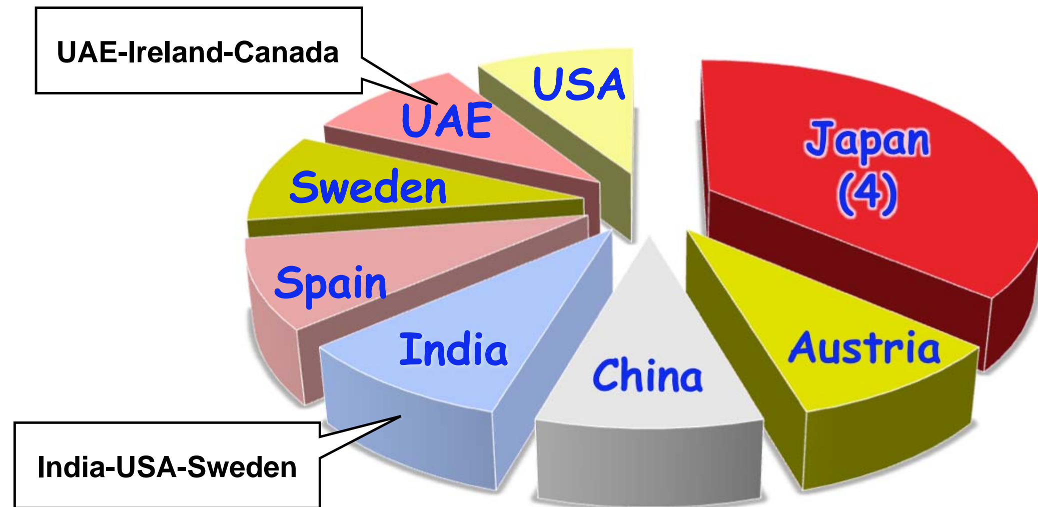
Monday June 29, 2009

Program Committee

Jacob A. Abraham	University of Texas, Austin, USA
Lorena Anghel	TIMA, Université de Grenoble, France
Davide Appello	STMicroelectronics, Agrate Brianza, Italy
Vikas Chandra	ARM R&D, San Jose, CA, USA
Yves Crouzet	LAAS-CNRS, Toulouse, France
Giorgio Di Natale	LIRMM, Montpellier, France
Babak Falsafi	EPFL, Lausanne, Switzerland
Richard E. Harper	IBM Research, Yorktown Heights, NY, USA
Shubhendu S. Mukherjee	Intel Corp., Hudson, MA, USA
Takashi Nanya	University of Tokyo, Japan
Jean-Jacques Quisquater	Univ. Cath. Louvain, Belgium
Juan Carlos Ruiz García	Univ. Politécnica de Valencia, Spain
Allan Silburt	Cisco Systems, Ottawa, ON, Canada
Arun Somani	Iowa State University, Ames, USA
Janusz Sosnowski	Warsaw University of Technology, Poland
Andreas Steininger	Vienna University of Technology, Austria
Alan Wood	Sun Microsystems, Santa Clara, CA, USA
Yervant Zorian	Virage Logic, Fremont, CA, USA

Program Set up

- 11 submissions



- Each submission reviewed by 4+ PC members
- Selection —> 8 presentations from submitted contributions
- 2 invited talks
- 1 panel

Program-at-a-Glance

Moderator

1- Opening and Invited Talks.. Jean Arlat

- **8:30-8:40** Workshop Introduction
- **8:40-10** *Vikas Chandra, Cecilia Metra*

10-10:30 Coffee break

2- Reliability Issues and Assessment..Johan Karlsson

- **10:30-11:50** *Eishi Ibe, Valeriu Beiu, David de Andres, Scott Bingham*
- **11:50-12** Additional Discussion

12-13:30 Lunch

3- Resilience Enhancement Techniques......................................Michael Nicolaïdis

- **13:30-14:50** *Tomohiro Yoneda, Daniel Skarin, Pramod Subramanyan, Andreas Steininger*
- **14:50-15** Additional Discussion

15-15:30 Coffee break

4- Panel and Closing...Cristian Constantinescu

Scaling Towards Nanometer Size Devices: Issues and Solutions

- **15:30-16:20** Presentations by the panelists
  Jacob Abraham, Valeriu Beiu, Helia Naeimi, Arun Somani, Seongmoon Wang
- **16:20-17** Panel discussion and Workshop Wrap up

17 Workshop Adjourn

About Nanocomputing

- Nanocomputing describes computing that uses extremely small — or nanoscale — devices (1 nm = 10^{-9} m).
  - Top Down: MOS device downscaling "More Moore"
  - Bottom Up: (Self-)assemblies of nanoelectronics devices "Beyond Moore"
- NanoComputing: The End — Not Here Yet, But Coming Soon, *Science*, Vol. 293. no. 5531, August 2001, p. 787
- The Future of Nanocomputing, George Bourianoff, Intel Corp., *Computer*, Aug. 2003, pp. 44-53
- Computer Architectures for Nanotechnology: Towards Nanocomputing, Christian Gamrat, CEA/LIST, in *Nanoscience*, (C. Dupas, P. Houdy, M. Lahmani, Eds), Springer, 2007
- Towards Achieving Reliable and High-performance Nanocomputing via Dynamic Redundancy Allocation, Shuo Wang, Lei Wang, Faquir Jain, *ACM J. on Emerging Technologies in Computing systems*, Vol.5, no.1, Jan. 2009

ITRS* Crosscutting Challenge 5: Reliability

Relaxing the requirement of 100% correctness for devices and interconnects may dramatically reduce costs of manufacturing, verification, and test.

Such a paradigm shift is likely forced in any case by technology scaling, which leads to more transient and permanent failures of signals, logic values, devices, and interconnects.

Several example issues are as follows. 1) Below 65nm, single-event upsets (soft errors) impact field-level product reliability, not only for embedded memories, but for logic and latches as well. 2) Methods for accelerated lifetime testing (burn-in) become infeasible as supply voltages decrease (resulting in exponentially longer burn-in times); even power demands of burn-in ovens become overwhelming. 3) Atomic-scale effects can demand new "soft" defect criteria, such as for non-catastrophic gate oxide breakdown. In general, automatic insertion of robustness into the design will become a priority as systems become too large to be functionally tested at manufacturing exit.

Potential solutions include automatic introduction of redundant logic and on-chip reconfigurability for fault tolerance, development of adaptive and self-correcting or self-healing circuits, and software-based fault-tolerance.

* International Technology Roadmap for Semiconductors — 2008 Update (www.itrs.net)