On the Evaluation of Reliability of NanoFabric-based architectures through Fault Simulation

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Abstract

Chemically Assembled Electronic Nanotechnology is a promising alternative to CMOS fabrication. In particular, the nanoFabric has proven to be a viable solution for implementing digital circuits. We propose an automated platform for fault simulation of combinational circuits mapped on the nanoFabric architecture, which is being used for the evaluation of reliability techniques applicable to this kind of devices.

As technology approaches the limits of CMOS fabrication, due to economic and technical factors, such as ultra thin gate oxides, short channel effects and doping fluctuations, a promising alternative to CMOS-based computing is *Chemically Assembled Electronic Nanotechnology* (*CAEN*). CAEN uses direct self-assembly and self-alignment to construct electronic circuits out of nanometer scale devices.

A CAEN-based device called *nanoFabric* [1] is an array of molecular electronic devices. It is composed of *nanoBlocks* and *switchBlocks*; the former include electrically programmable connections between orthogonal nanowires and implements the logic functions similarly to a *Programmable Logic Array* (*PLA*) device, while the latter are used for routing signals between nanoBlocks. It is estimated that nanoFabrics can include up to 10^{12} devices/cm^2, which is significantly higher than that of CMOS-based devices. However, defect densities in these devices are expected as high as 10% after fabrication.

Different approaches have been proposed in literature for dealing with such high defect rates, exploiting the intrinsic redundancy of the high-density structure for mapping the circuit avoiding the defective spots: some are based on the creation of a defect map for each manufactured chip [2][3], others on the integration of configuration and test [4][5]. These techniques allow avoiding the effects of production defects, but the systems are still susceptible to permanent and transient faults that arise during the product life cycle. Effects of transient faults have been studied probabilistically [6] and may be avoided through the use of proper redundancy techniques.

We propose an automated platform for the reliability evaluation of circuits implemented on the nanoFabric architecture based on fault-simulation. Since no standard tools are available for circuit mapping on nanoFabrics, we developed a flow for this initial task relying on traditional synthesis software and ad-hoc tools. Any combinational circuit can be implemented into a nanoFabric structure (possibly using defect map information to avoid defective spots); the structures are modeled using VHDL descriptions. Then, the fault-simulation platform allows injecting a user-defined list of permanent or transient faults (*stuck-at*, *stuck-open*, *forward and reverse-biased diode faults*, *bridging faults*, *single-event upsets and transients*) on the synthesized structure.

Preliminary experimental analysis has been performed on a set of benchmark circuits (ISCAS85). Stuck-at and diode faults have been injected and exhaustively simulated, showing that about 35% of the injected faults provoke an error on output; most faults can be detected simply comparing the circuit's direct and inverted output (the two outputs are provided since this kind of logic cannot perform inversions). Less than 1% of errors caused by diode faults on nanoBlocks is undetected and may be avoidable using different configurations of the logic array.

The platform is currently being exploited for the evaluation of different fault-tolerant configurations based on redundancy (such as Triple Modular Redundancy – TMR, etc.) on nanoFabric-based circuit implementations in different faulty scenarios.

References

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