Identifying Fault Mechanisms and Models of Emerging Nanoelectronic Devices

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As CMOS technology enters the nanoelectronic realm (tens of nanometers and below), where quantum mechanical effects start to prevail, conventional CMOS devices are meeting many technological challenges for further scaling. This situation has motivated the emergence of a variety of new nanoelectronic devices [1]. All these devices try to achieve a number of good characteristics such as extremely small dimensions, high switching speed, low power consumption, ease of fabrication and good scaling potential. Their main drawbacks include the need of low temperature operation, the low fanout and their poor reliability.

A confident use of these technologies relies on our capacity to better understand their fault mechanisms, and our ability to deduce related fault models.

We have conducted a prospective analysis of some relevant fault mechanisms of emerging nanoelectronic devices (resonant tunnelling devices, single-electron transistors, quantum cellular automata, spin devices, rapid flux quantum devices, molecular electronic devices, carbon nanotubes) which have been compared to those existing in deep-submicron CMOS technology.

New transient fault mechanisms, usually not considered in CMOS technologies, have been identified. Of particular importance are *thermal effects* and *background charges*, and *electromagnetic perturbations* of quantum dots and devices based on ferromagnetic materials. However, *cosmic radiation*, a major cause of concern in CMOS technologies, may not have such a great impact on new nanodevices due to the use of materials different than semiconductor silicon. An increasing incidence of manufacturing faults, manifested as permanent faults, can be precluded. Their main potential causes are *defects in tunnel layers*, *interconnect alignment*, and *doping level variations*. Defects related to the *self-assembly process* in molecular nanoelectronics can also be remarked. As in deep submicron CMOS technology, an increasing rate of intermittent faults is also expected, mainly due to manufacturing processes.

Table 1 compares the most harmful mechanisms of nanodevices and deep submicron CMOS [2].

Table 1. Fault mechanisms with greater impact on deep submicron CMOS and nanodevices

Faults	Deep submicron CMOS	Emerging nanodevices
Transient	Particles (package, cosmic radiation) Interconnections	Thermal effects Background charges Electromagnetic noise Cosmic radiation?
Intermittent	Manufacturing residuals Process variations	
Permanent	–	Manufacturing (tunnel layers, interconnect alignment, doping)

This study has allowed us to deduce fault models at transistor and logic abstraction levels according to transistor and simple circuit designs. Many are similar to classical CMOS fault models, since these circuits have a classical CMOS style or are hybrid designs with MOS transistors. Some other fault models are notably different and require a deeper analysis.

The definition of these fault models can be considered as a step forward towards the dependability assessment of emerging architectures for the definition of new and efficient fault mitigation techniques.

Well known mitigation techniques proposed in the architectures for nanodevices are grouped into Defect Tolerance (DT) and Fault Tolerance (FT) [3]. Improvements on these techniques should take into account the on-line defect mapping and reconfiguration in DT to deal with operational faults, hybrid solutions (DT/FT) and the design of robust nanodevices.

References

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[3] J. Han, "Fault-Tolerant Architectures for Nanoelectronic and Quantum Devices", Ph.D. dissertation, Delft University of Technology, 2004.