# NBTI-Resilient Memory Cells with NAND Gates for Highly-Ported Structures

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Work done in the Phoenix Project

# Motivation

One of the main **sources of failure** affecting transistors:

- **NBTI** (Negative Bias Temperature Instability)

NBTI issues

- Affects **PMOS transistors with “0” at their gates**
- Some molecules are broken and some atoms displaced

NBTI negative effects

- $V_{TH}$ increases, and hence, PMOS transistors **become slower**
- Minimum operating voltage (Vmin) of bit cells in a given block increases, so $\mathbf{V_{DD}}$ **cannot be decreased** as much for power savings (e.g. UL1 cache)

# Agenda

Motivation

**NBTI effects**

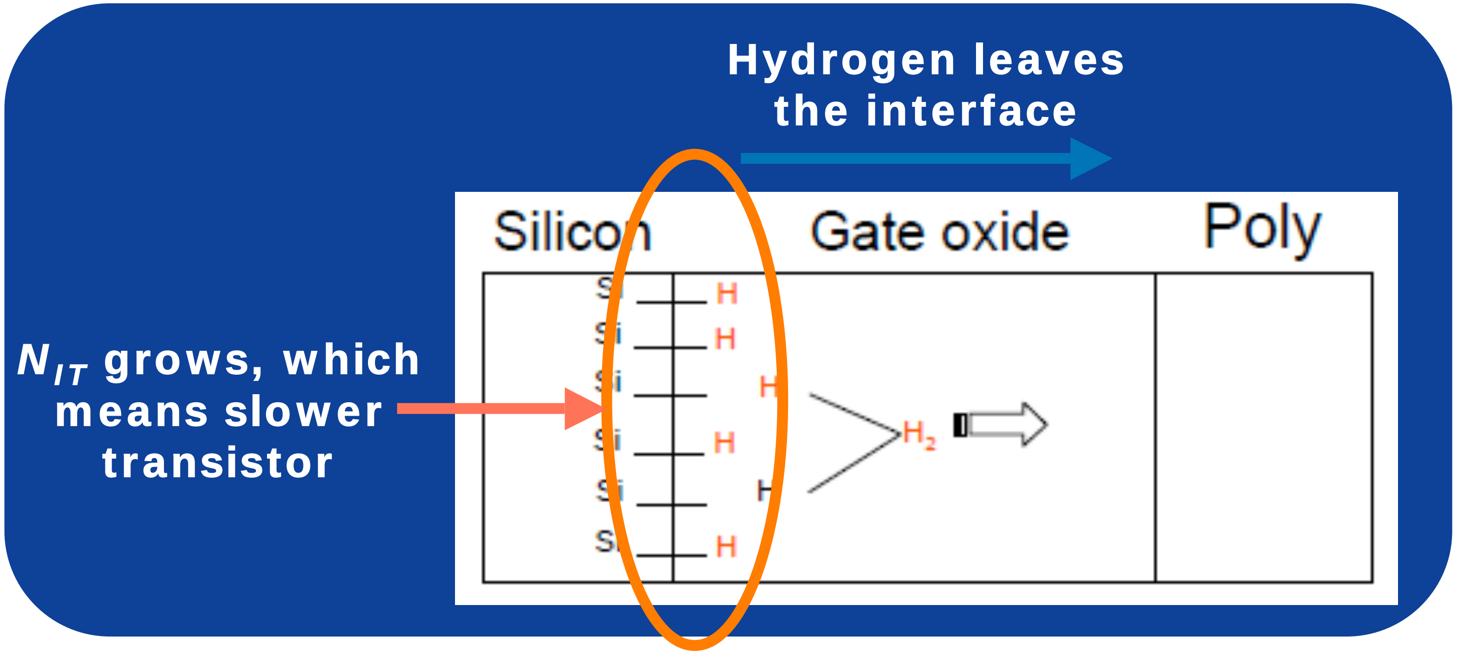
Memory cell design: conventional vs NAND-based

Results and final remarks

# NBTI Degradation

NBTI affects PMOS transistors when voltage at the gate is negative: Si-H bonds break

- More traps ($N_{IT}$) in the interface make the transistor slower

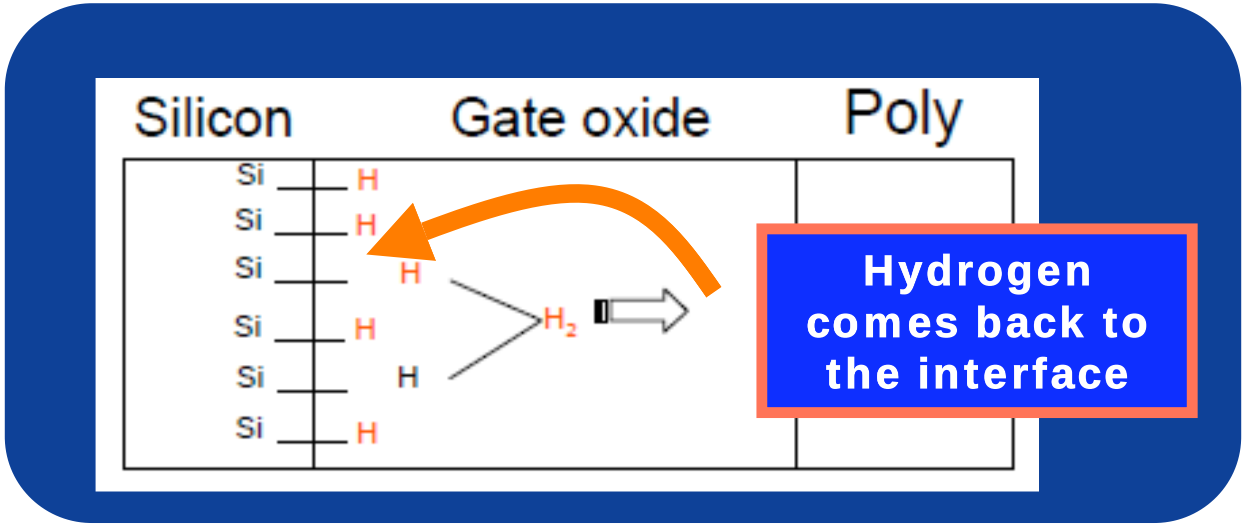



Source: M.A. Alam, “On Reliability of Microelectronic Devices: An Introductory Lecture on Negative Bias Temperature Instability”, Sept. 2005

# NBTI Self-Healing

Self-healing during non-negative voltage at gate

- H, $H^+$, $H_2^+$ close to the Si rebuild their bonds
- Self-healing is partial (not all bonds are rebuilt)

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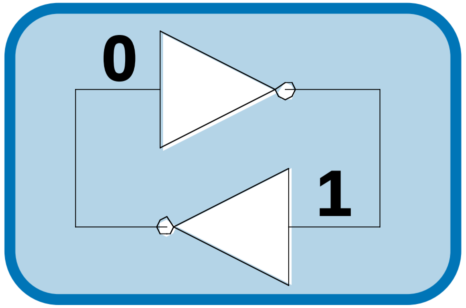
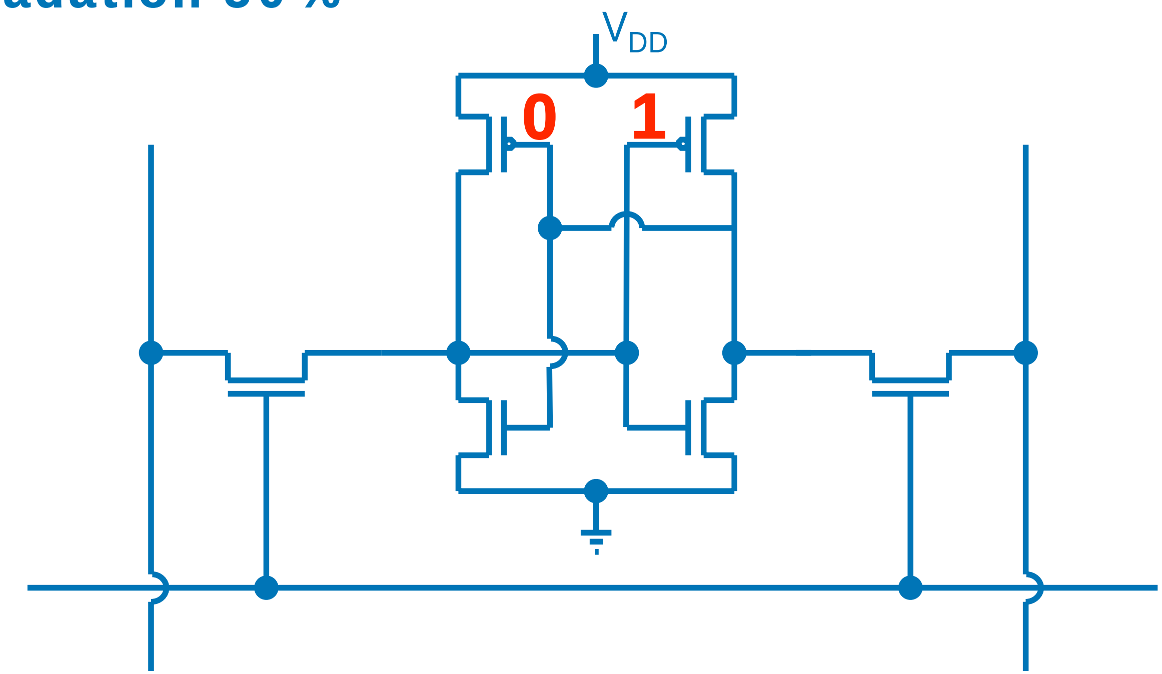
# Conventional Memory Cell Design

PMOS transistors degrade only when they have a “0” at their gates (what we call “duty cycle”)

- Two inverters. **One of them degrades at any time**
- Average **PMOS degradation 50%**

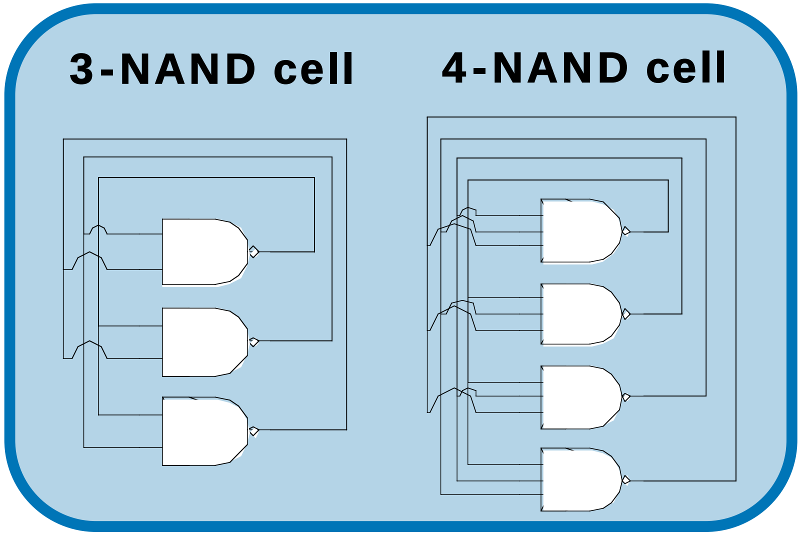


# New Memory Cell Design

NAND-based memory cells

- A given number (N) of NANDs. Only **one NAND outputs a “0”**
- Average PMOS **degradation 1/N** (e.g. **N=4, degradation 25%**)
- Area overhead pays off for highly ported structures (e.g. register files)




Example: 4-NAND cell

- Twice the number of bitlines than a conventional memory cell
- 4 different states, so **it encodes 2 bits**
- Thus, **same overhead per port** as a conventional memory cell

# Data Bias

Data **highly biased** towards “0”

- Conventional cells: **One PMOS degrades much more** than the other
- NAND-based cells: **Some PMOS degrade much more** that the others

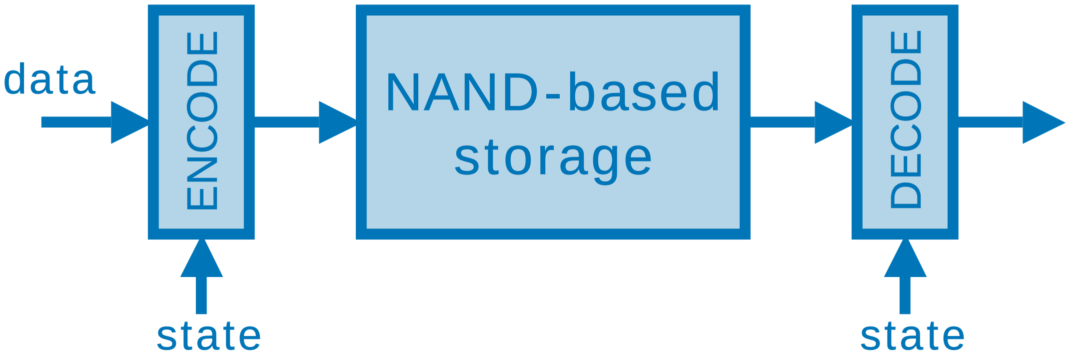
Solution

- Conventional cells: **store inverted contents 50% of the time**
- NAND-based cells: **periodically change codification** of data to balance degradation of PMOS

# Example: Conventional vs 4-NAND


Example “01”. Analogous for “00”, “10”, “11”

| state | write | encoded | read |
|---|---|---|---|
| 0 | 01 | **01** | 01 |
| 1 | 01 | **10** | 01 |




| state | write | encoded | read |
|---|---|---|---|
| 00 | 01 | **1011** | 01 |
| 01 | 01 | **1101** | 01 |
| 10 | 01 | **1110** | 01 |
| 11 | 01 | **0111** | 01 |

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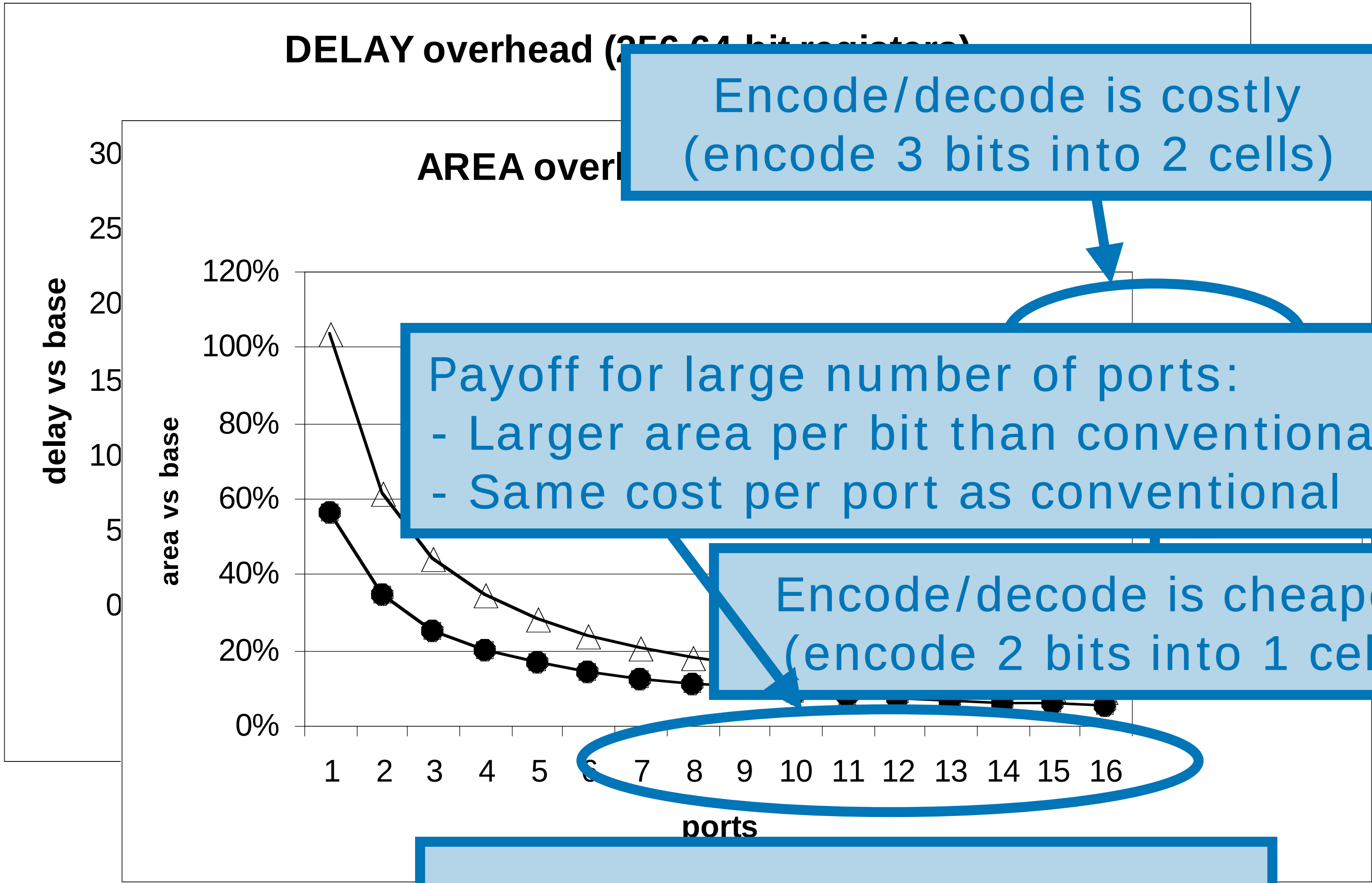
# Preliminary Results




Encode/decode is costly (encode 3 bits into 2 cells)

Payoff for large number of ports:
- Larger area per bit than conventional
- Same cost per port as conventional

Encode/decode is cheaper (encode 2 bits into 1 cell)

**Conventional: 50% duty cycle**
**3-NAND: 33% duty cycle**
**4-NAND: 25% duty cycle**

# Final Remarks

- NAND-based cells **reduce duty cycle** so lower guardbands are required for the **cycle time** and the **Vmin**
- Decreasing guardbands may **offset overheads** (partially or totally?)
- **Test chip data required**
  - Obtain accurate results of the overheads
  - Measure whether NAND-based cells payoff for current technologies
- NBTI degradation is still an open research topic
  - **How much does it cost** for current technologies? Different works show large discrepancies
  - **Will it worsen** for future technologies?

# Thank you !