Model-Based Fault Injection for Failure Effect Analysis – Evaluation of Dependable SRAM for Vehicle Control Units –

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Outline

• Background
• Proposed Fault-Injection System
• 7T/14T Dependable SRAM
• System-Level Evaluation
• Conclusion
Background (1/2)

Obstacles to VLSI reliability

Process variation, lithography, environmental fluctuation, NBTI, and soft error

To verify operating stability on a system LSI with a large number of vulnerable SRAMs, we must consider the device-level reliability of SRAM

We propose a novel fault-injection scheme using physical characteristics of the SRAM for the system-level verification
Background (2/2) (PILS and SRAM)

Processor-in-the-Loop Simulation (PILS)

Controller (Model) → Mechanical plant (Model)

Micro-controller LSI

Logic block

SRAM block

MC: Memory cell

Composed by small-sized transistors
(Channel size = 1–2.5F²)
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Proposed Fault-Injection System (FIS)

Can inject device-level SRAM failures into the system-level verification environment

The proposed fault-injection system can evaluate the impacts of SRAMs reliability on the operating stability of system
Failures in SRAM

Read/write margin failure

- Process variation
- Aging of transistor
- Environmental fluctuation

Soft error (temporarily failure)

- Neutron collision
- Alpha collision

<table>
<thead>
<tr>
<th>Write</th>
<th>Read</th>
<th>Failure period</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Normal read</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Flip 1</td>
</tr>
</tbody>
</table>

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<td>Flip 0</td>
</tr>
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<td>0</td>
<td>1</td>
<td>Normal write</td>
</tr>
</tbody>
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Soft error

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<th>Read</th>
<th>Failure period</th>
</tr>
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<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Data retention period</td>
</tr>
</tbody>
</table>

Flip 0

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</tr>
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Flip 1

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<td>0</td>
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</tbody>
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Data retention period

Read/write margin failure is datum-dependent ("0" failure or "1" failure)
Proposed Fault-Injection Flow

- Transistor-level SRAM netlist
- Device conditions (Supply volt., temp., aging etc.)

**Device level**
- SPICE Monte Carlo simulation
- SRAM BER library at each device condition
- Verification conditions of system LSI (Supply volt., temp., aging, SER etc.)

**Information of virtual chip**
- Fault Case Generator (FCG)
- System-level verification (PILS)
- SRAM failure data patterns

**System level**
- System-level verification (PILS)
Concept of Virtual Chip

Features

- Reproduce spatial randomness of SRAM failures
- Datum-dependencies are also determined randomly

Main advantages

- Reproduce the features on actual Si chips
- Repeatability of simulation
- Large-scale verification capability
Large-scale Verification using Virtual Chip

Proposed scheme w/ Virtual chip can perform an exhaustive large-scale verification
Fault Case Generator (FCG)

FCG can generate time-series SRAM failure data patterns corresponding to arbitrary waveforms for the power supply noise and operating temperature, and device parameters.
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7T/14T Dependable SRAM

Conventional 6T SRAM

7T/14T SRAM

Internal nodes are directly connected with additional transistors.

Can dynamically change its operating margin
### Proposed SRAM has three modes.

<table>
<thead>
<tr>
<th>Mode</th>
<th># of BCs stored 1bit</th>
<th># of WL drive</th>
<th>P0, P1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal</td>
<td>1 (7T/bit)</td>
<td>1</td>
<td>OFF</td>
</tr>
<tr>
<td>Dependable(write)</td>
<td>2 (14T/bit)</td>
<td>2</td>
<td>ON</td>
</tr>
<tr>
<td>Dependable(read)</td>
<td>2 (14T/bit)</td>
<td>1</td>
<td>ON</td>
</tr>
</tbody>
</table>

Reliability is trade-off for area.
Bit Error Rates (Read Operation)

65-nm process, FS corner, Temp. = 125 °C

- Conv. (6T) = 7T
- 14T (Dependable)

BER vs. VDD (V)

- Bit Error Rates (Read Operation)
- 1.9 x 10^{-5}
- 0.60V
- 0.21V
- 0.81V
Bit Error Rates (Write Operation)

65-nm process, SF corner, Temp. = −40 °C

Conv. (6T) = 7T
14T (Dependable)

BER

VDD (V)

5.5 x 10^{-4}

0.69V

0.26V

0.95V
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**Evaluation Methodology**

- Object system: vehicle ECU system
- The conventional 6T SRAM and 7T/14T dependable SRAM (14T dependable mode) are used as internal SRAM of ECU
- Abnormal termination of the vehicle ECU system is judged by a watchdog timer interruption and an access violation to an illegal address
- # of sample (virtual chip): 1050
- Evaluation method: Static supply voltage (DC) and operating temperature characteristics
- Aging: 10-year NBTI degradation

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<table>
<thead>
<tr>
<th>Controller model</th>
<th>Vehicle engine model</th>
</tr>
</thead>
<tbody>
<tr>
<td>Micro-controller</td>
<td>SH-2A CPU</td>
</tr>
<tr>
<td>CPU</td>
<td>DMAC</td>
</tr>
<tr>
<td>Peripheral</td>
<td>Bridge</td>
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Matlab®/Simulink® simulator
CoMET™ simulator
Verification conditions for system
Fault Case Generator

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System-level verification environment (PILS)
Fault-injection scheme
Fault-Injectable bus bridge
SRAM failure data pattern

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System-Level Evaluation Result

ECU System w/ 6T SRAM

ECU System w/ 7T/14T SRAM

ECU w/ 7T/14T SRAM improves the minimum op. voltatge by 0.05–0.15 V
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- **Proposed fault-injection system (FIS)**
  - Can inject well-device-conscious SRAM failures

- **Proposed fault-injection flow**
  - Can generate and inject SRAM failures from the device level to the system level

- **Dependability of vehicle ECU system using the 6T SRAM and the 7T/14T dependable SRAM are evaluated**
  - Proposed FIS can evaluate the relationships between the SRAM dependability and the system operating stability