Multi-Voltage Low-Power Design Technique with Built-in Voltage Measurement Mechanism for 3D-CIHIP

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Outline

• Motivation
• The Major Challenges of 3D IC
• The Proposed Low Power Technique for 3D IC
  • Power Switch Control Circuit
  • Retention Flip-Flop
  • Built-in Voltage Measurement
• Test Chip Design
• Chip Measurement Results
• Conclusion
Motivation

Area, Power, and Performance

2D Design

3D Stacking Design
The Major Challenges of 3D IC

- High power consumptions and *voltage drops*
- Heat dissipation lead to HOT design

Low Power and Power Management Techniques are required !!

- Testing techniques
- EDA design tools
Dynamic Voltage Frequency Scaling (DVFS)

IEEE Circuits and Systems Magazine, First Quarter, 2010
The Proposed Low-Power Techniques

- Power Switch Control Circuit (PSCC)
- Built-in Voltage Measurement (BIVM)
- Retention Flip-Flop (Ret FF)
Power Switch Control Circuit

<table>
<thead>
<tr>
<th>sel</th>
<th>sleep</th>
<th>sleep</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>0</td>
<td>sleep</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Low Voltage</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>High Voltage</td>
</tr>
<tr>
<td>1 CKVDD</td>
<td></td>
<td>Low power mode</td>
</tr>
</tbody>
</table>
Low-Power CKVdd Technique

\[ \text{Energy} \approx \frac{2RC_{SW}}{\Delta t} \left( \frac{1}{\Delta t} \frac{1}{2} C_{SW} V_{dd}^2 \right) \]

\[ V_{OUT} = V_{dd} \left( t - RC_{SW} \right) \frac{1}{\Delta t} \]

Built-in Voltage Measurement (BIVM)

BIDM (Built-in Delay Measurement)
Built-in Time Measurement (BIDM)
2D Test Chip Design

BIVM

BIDM
Chip Specification

<table>
<thead>
<tr>
<th>Technology</th>
<th>TSMC 0.18 CMOS 1P6M</th>
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<tbody>
<tr>
<td>Chip Size</td>
<td>1.08 x 1.08mm²</td>
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<tr>
<td>Power Supply</td>
<td>1.8v ~ 1.2v</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>0.98mW</td>
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<tr>
<td>Frequency</td>
<td>100MHz</td>
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<tr>
<td>Number of pin</td>
<td>40</td>
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</tbody>
</table>
Instrument Measurements (Retention FF)

Data Retention mode time

(a) Retention Mode

$V_{Vdd} = 1.24V$ Data recovery
Measurement Results

**Normal mode**

$\text{VVdd}=1.178V$

**Coarse-bit=7, fin-bit=3**

$\text{BIVM}=1.15V$
MorPack 3D Stack Technique

Developed by Chip Implementation Center, Taiwan
Our 3D Stacking Design

32 bits

Low Power (LP) Multiplier
Multi-Voltage
+PSCC
+BIVM
+RetFF

64 bits

32 bits

8 bits

LP-Multiplier

16 bits

8 bits

LP-Multiplier

16 bits

8 bits

LP-Multiplier

16 bits

8 bits

LP-Multiplier

16 bits

64 bits
Conclusion

The efficient low power multi-Vdd techniques are proposed
• (1) Power Switch Control Circuit
• (2) Retention Flip-Flop
• (3) Built-in Voltage Measurement

• The new high-performance with low-power 3D stacking design are evaluated by using MorPack technique
~Thanks to your attention~