Study the Effect of SET Induced Faults on Submicron Technologies

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Content

• Transient Faults
• Methodology
• Fault simulation
• Results
• Conclusion and Future Work
Transient Faults

- Origin of Transient Faults
  - Neutrons, protons, pions
  - Alpha particles
- Transient Induced Faults
  - SEU (Single Event Upset)
  - SET (Single Event Transient)
Transient Faults

- Importance of SEU and SET
  - Real Data from IROC Technologies (130nm)
    - 1 Error per 14 days for 148Mbyte memory
  - Increased complexity

- Higher density
  - Lower voltages
- Higher speeds
Methodology

• Physical Implemented Fault Injection
• Software Implemented Fault Injection
• Simulation-based Fault Injection

• Important issues
  • Accuracy of the processor model to conduct experiments
  • Pre-synthesized HDL model vs. post-synthesized timing netlist
  • The number of fault injection experiments
Fault Simulation

- **Xentium Processor (Recore Systems ©)**

The Xentium processor was fabricated in 90nm CMOS technology.
Fault Simulation

• Injection of SET

- Positive glitch
- Negative glitch

• Mibench benchmark suit
  • Quick Sort, BitCount and BasicMath program
Fault Simulation

- Timed and Untimed netlist
- Total failure rate of the datapath:

\[ P_{\text{total}} = (A/E) P_E + (A/S) P_S + (A/A) P_A + (A/C) P_C + (A/P) P_P + (A/M) P_M \]
Results

- Untimed netlist
Results

- Timed netlist
Results

- Different behaviour
  - Lower rate of injected faults has been propagated in untimed netlist
  - An independent convergence point in timed netlist
Results

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Conclusions and Future Works

• On simulated IP 10-26% chance of catastrophic failure
• Timing information
• Convergence point

• Propose faster simulation method
• Compare results with physical fault injection
• Propose method for EDAC
Questions?