Wrap-Up Discussion

- **Goal:**
  - To produce a list of Grand Challenges in Dependable Nanocomputing
  - Elaboration of Grand Challenges from ITRS-2009
  - Non-exhaustive list - Focus on problems brought up in the presentations

- **Areas of interest (examples):**
  - Circuit Design
  - Multi-core architectures
  - Testing
  - Fault Tolerance
  - Fault and failure models
  - Dependability prediction and assessment
List of Grand Challenges in Dependable Nanocomputing

- Testing of integrated circuits with massive process variations
  - Several problem areas highlighted in the special session
  - Testing of robust and FT circuits and systems is difficult
  - Identifying process parameters that has the most impact on dependability
  - Synergies between on-line and off-line testing
  - New definition of testing needed

- Building reliable systems from partially correct circuits
  - Confidence in test coverage
  - Reconfiguration, application deployment
List of Grand Challenges in Dependable Nanocomputing

Accurate modeling of faults, errors and failures
  - Understanding the impact of faults on the system service
  - Problem areas:
    - Linking models at different abstraction levels
    - Workload dependency
  - Fault types:
    - Soft errors (transient faults)
    - Intermittent faults
    - Aging faults
    - Delay faults
    - Design faults
    - Malicious faults
List of Grand Challenges in Dependable Nanocomputing

- Construction of dependable nanocomputing systems
  - Trade-off between Dependability, Energy consumption and Area Overhead
  - Cost-effective solutions
  - Trade-off between circuit, micro-architectural, software and system level techniques
  - Need for adaptive and configurable fault tolerance
  - Cost of design and design verification
  - Complexity (e.g., hubble radius)