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Soft Error Rate Trends

4th Workshop on Dependable and Secure Nanocomputing (WDSN-10)

Alan Wood

June 28, 2010

Shameless Advertisements

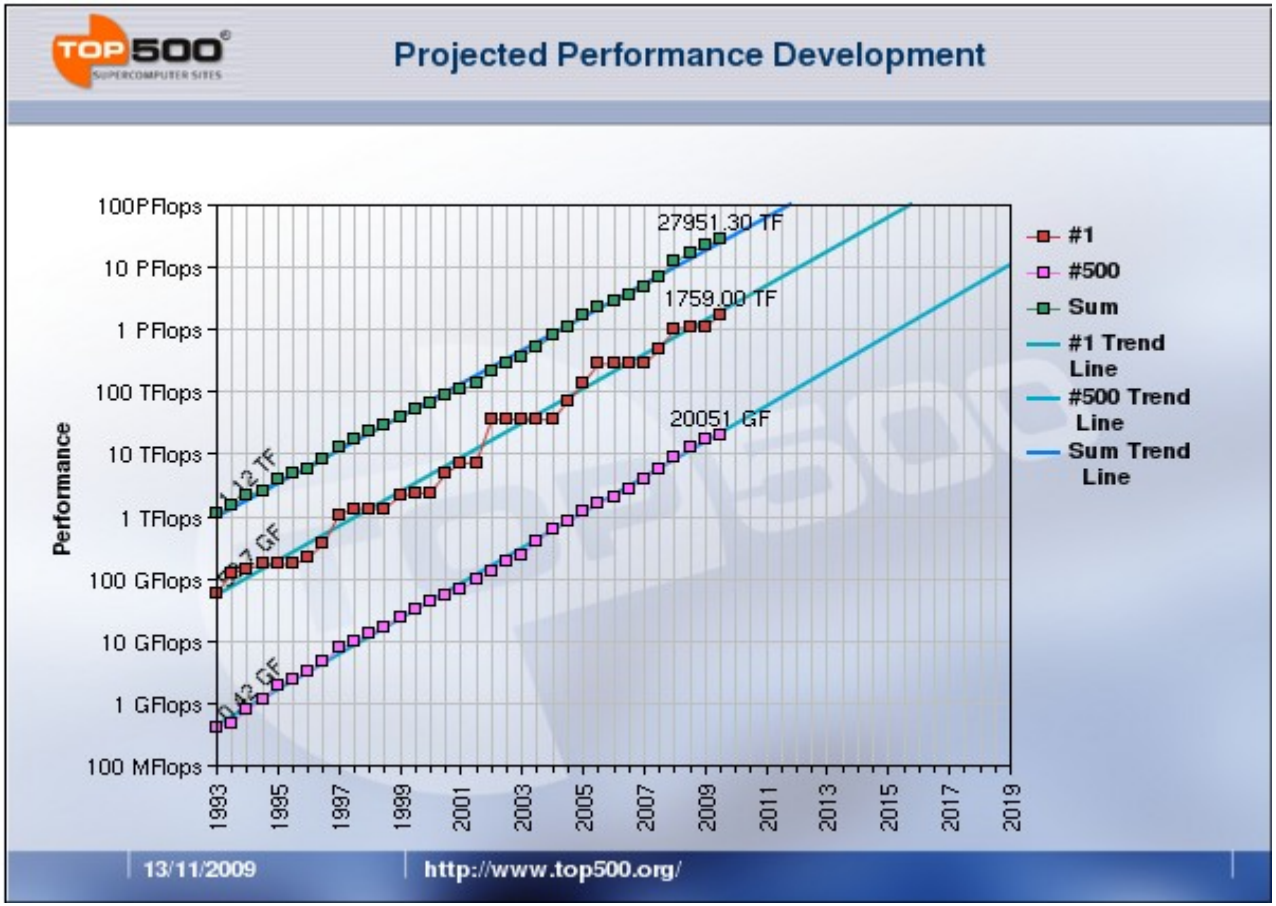
- Presentation data came from the 2010 Workshop on System Effects of Logic Soft Errors (SELSE-6)
  - www.selse.org
- Birds of a Feather session on The Future of Dependability Tuesday night, 18:00-19:30, State Room

Agenda

- Technology trends
- Soft error rate (SER) trends
  - DRAM
  - SRAM
  - Logic

The Largest Scale

- ExaFlops supercomputer (10^18) in 2020

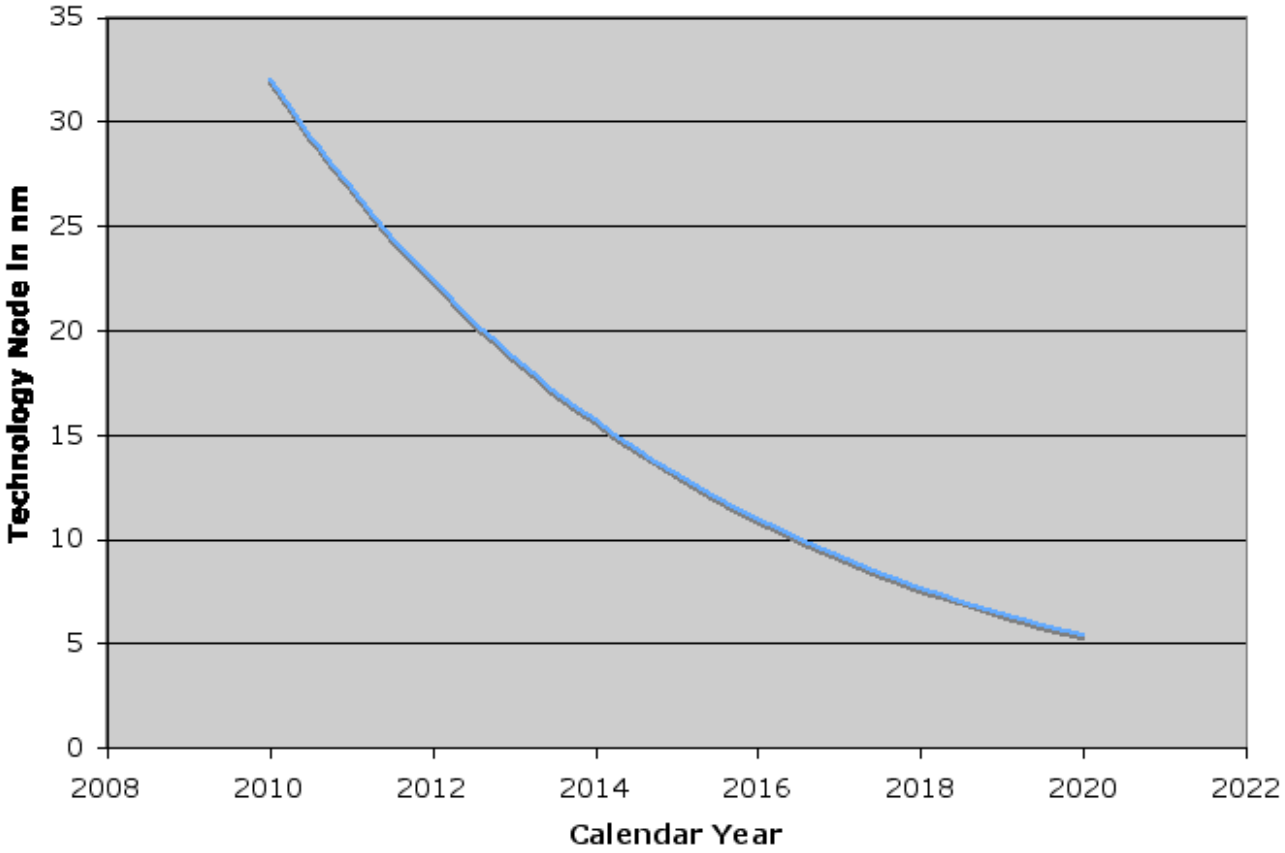


ExaScale Computing Challenges

- Energy – both for base computation and data transport
- Memory and Storage – bandwidth
- Concurrency and Locality – support for a billion parallel threads
- Resiliency - “the ability of a system to continue operation in the presence of either faults or performance fluctuations.”
  - Explosive growth in component count for large systems
  - Advanced technology
    - Lower voltage levels
    - New classes of aging effects

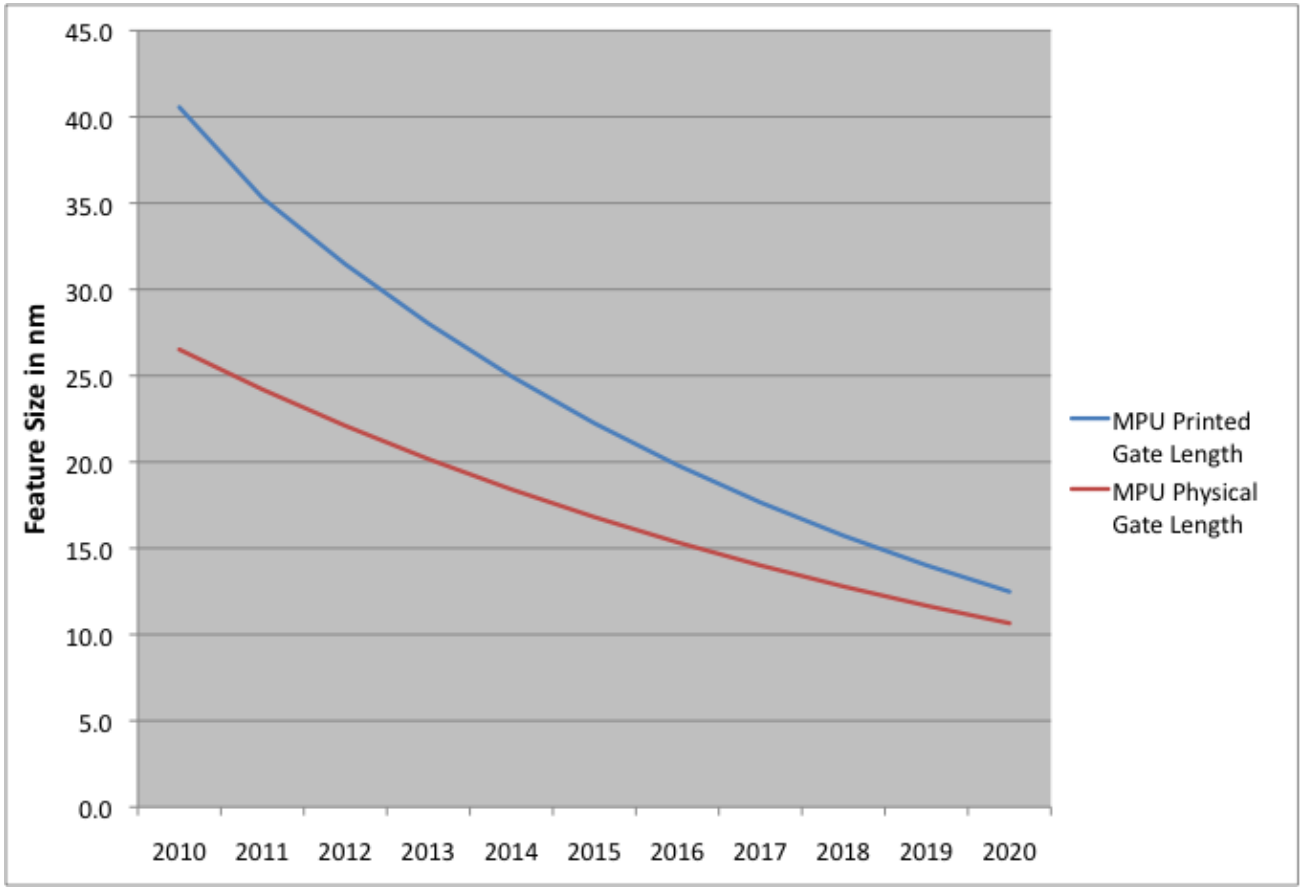
Source: DARPA ExaScale Computing Study

Equivalent Technology Scaling



"Equivalent" scaling means the number of functions doubles every 2 years (does not mean half pitch, gate length, feature size)

Feature Size Scaling



Feature size scaling not quite at Moore's law rate but still worrisome for SER trends

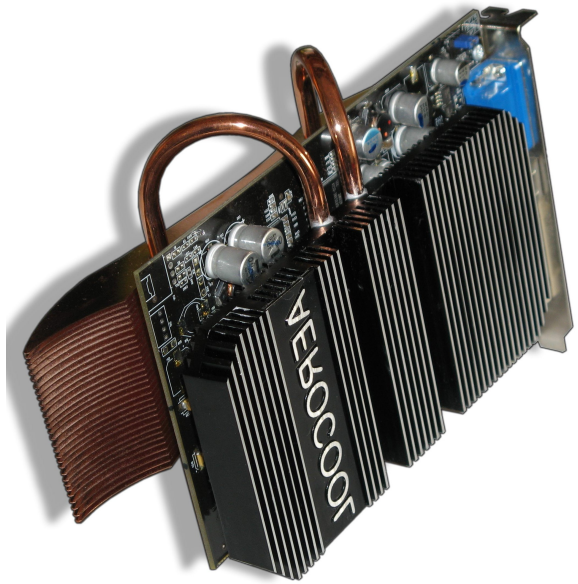
Source: 2009 ITRS

Servers in 2020

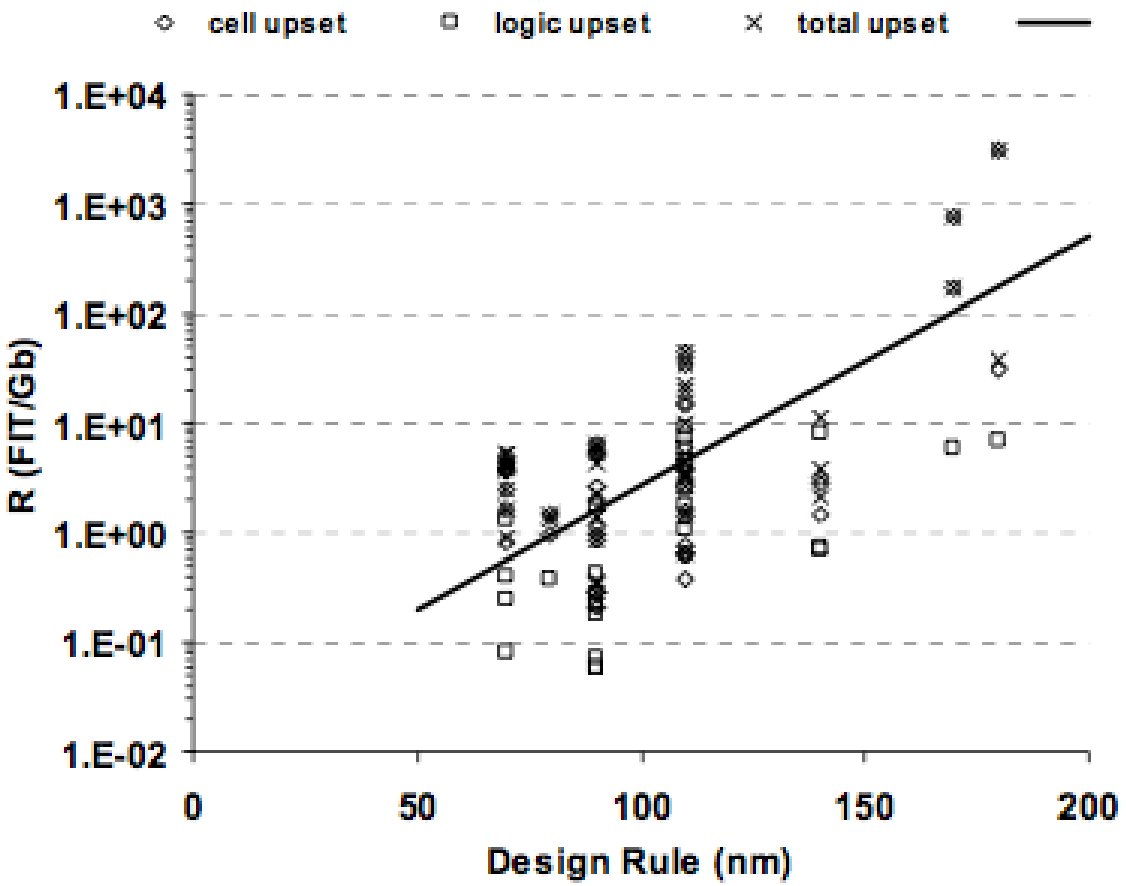
- Microprocessors
  - ~6-8nm technology (equivalent scaling)
  - ~128 cores per chip
  - ~16 Billion transistors per chip
  - Mostly SOCs?
  - CMOS replacement?
- Memory
  - Stacked or embedded (no DIMMs)
  - Flash part of memory hierarchy
  - New technologies (PRAM, NRAM, …)

Servers in 2020 - 2

- Storage
  - SSDs everywhere
  - New technology (holographic)?
- Packaging
  - 3D
  - Liquid cooling
    - Including on-chip, e.g., heat pipes
  - Free-space optics?



DRAM SER Trend

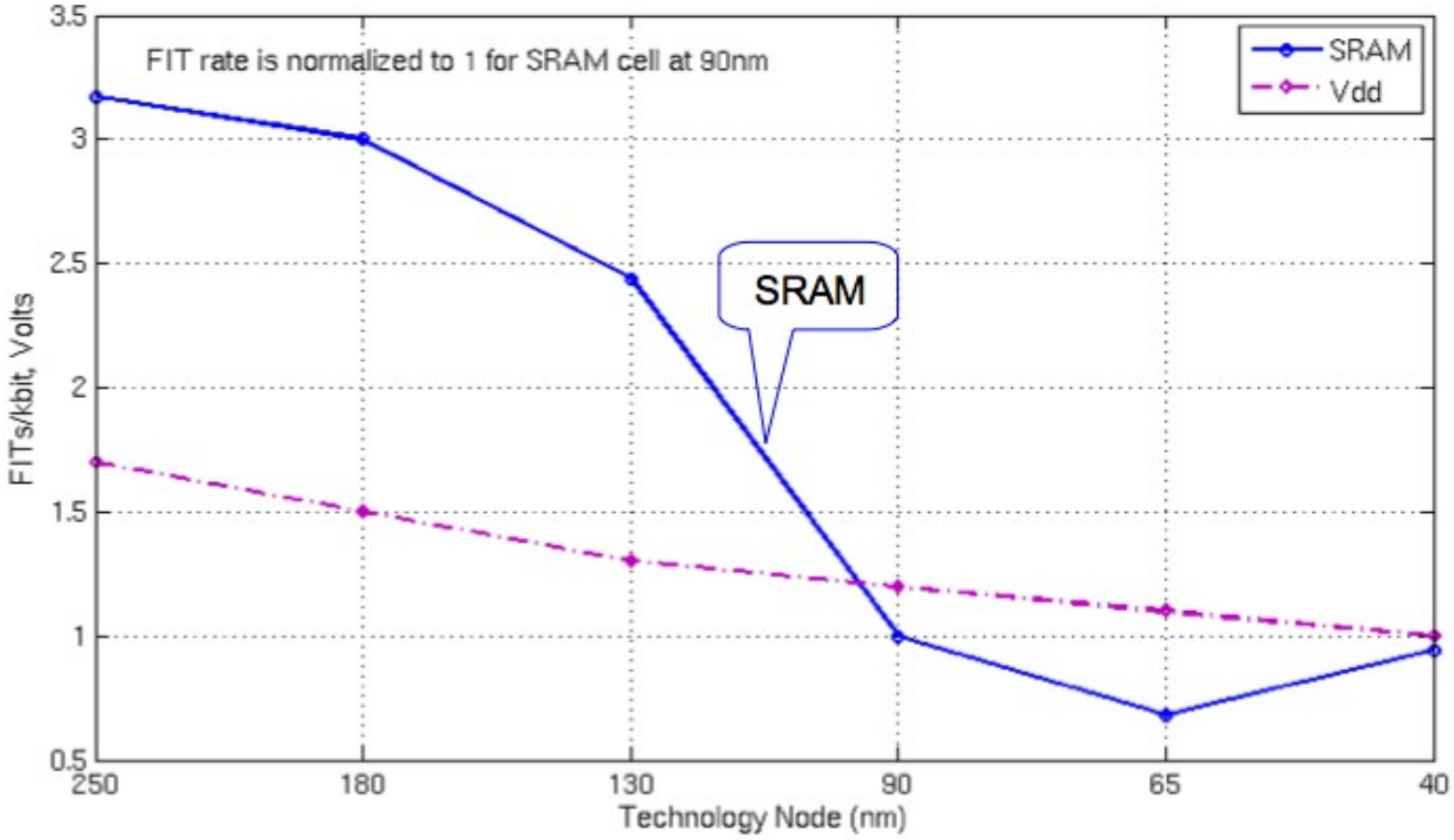


Source: L. Borucki, G. Schindlbeck and C. Slayman, “Comparison of Accelerated DRAM Soft Error Rates Measured at Component and System Level”, IRPS, Phoenix, 2008

DRAM SER Trend Explanation

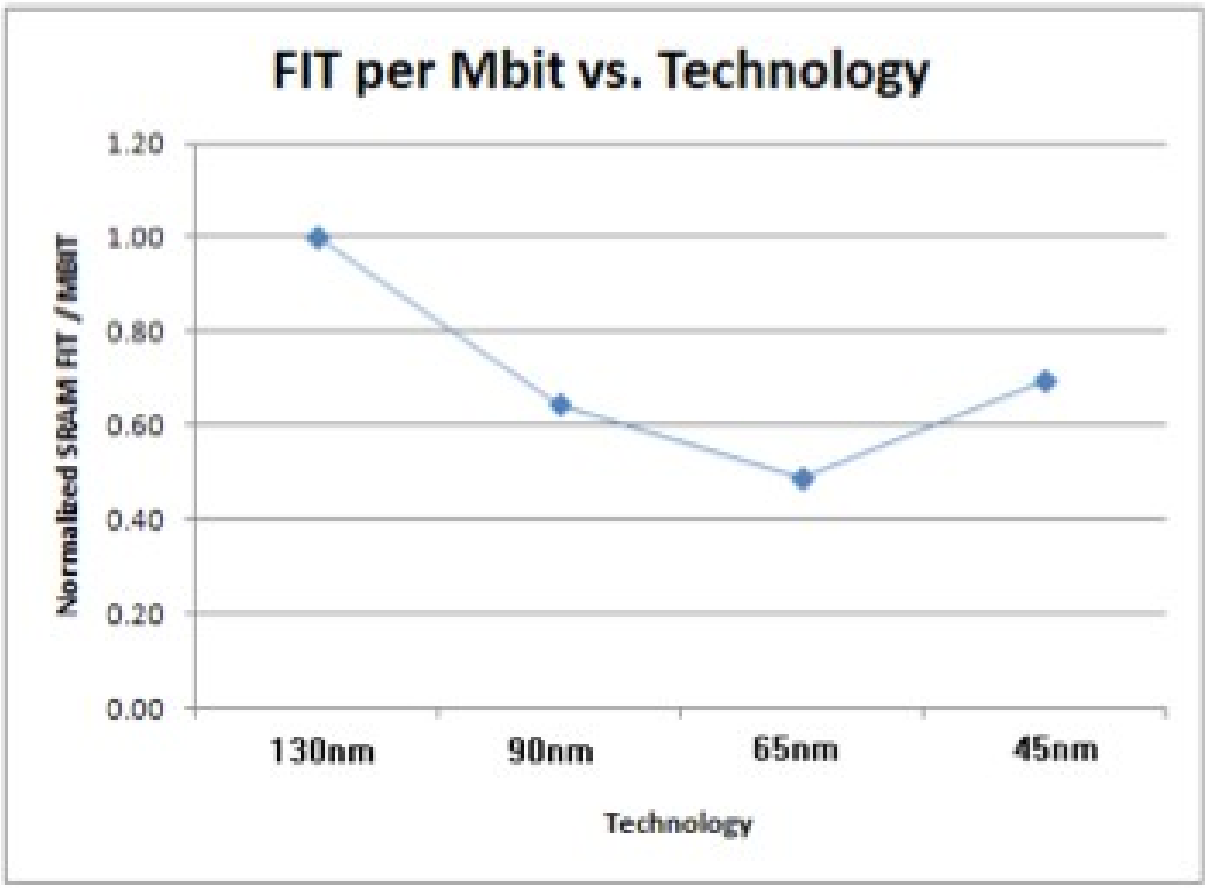
- DRAM memory cell SER has decreased by 2-3 orders of magnitude in the last 10 years
- Memory Cells
  - Basic DRAM cell has not changed much, so cell capacitance has not changed much, so Qcrit has not changed much
  - Charge collection area decreased by a factor of 2 with each generation
- DRAM Logic
  - Charge collection area has decreased, but decreases in voltage and different circuit designs has significantly decreased Qcrit

SRAM SER Trend- Sun



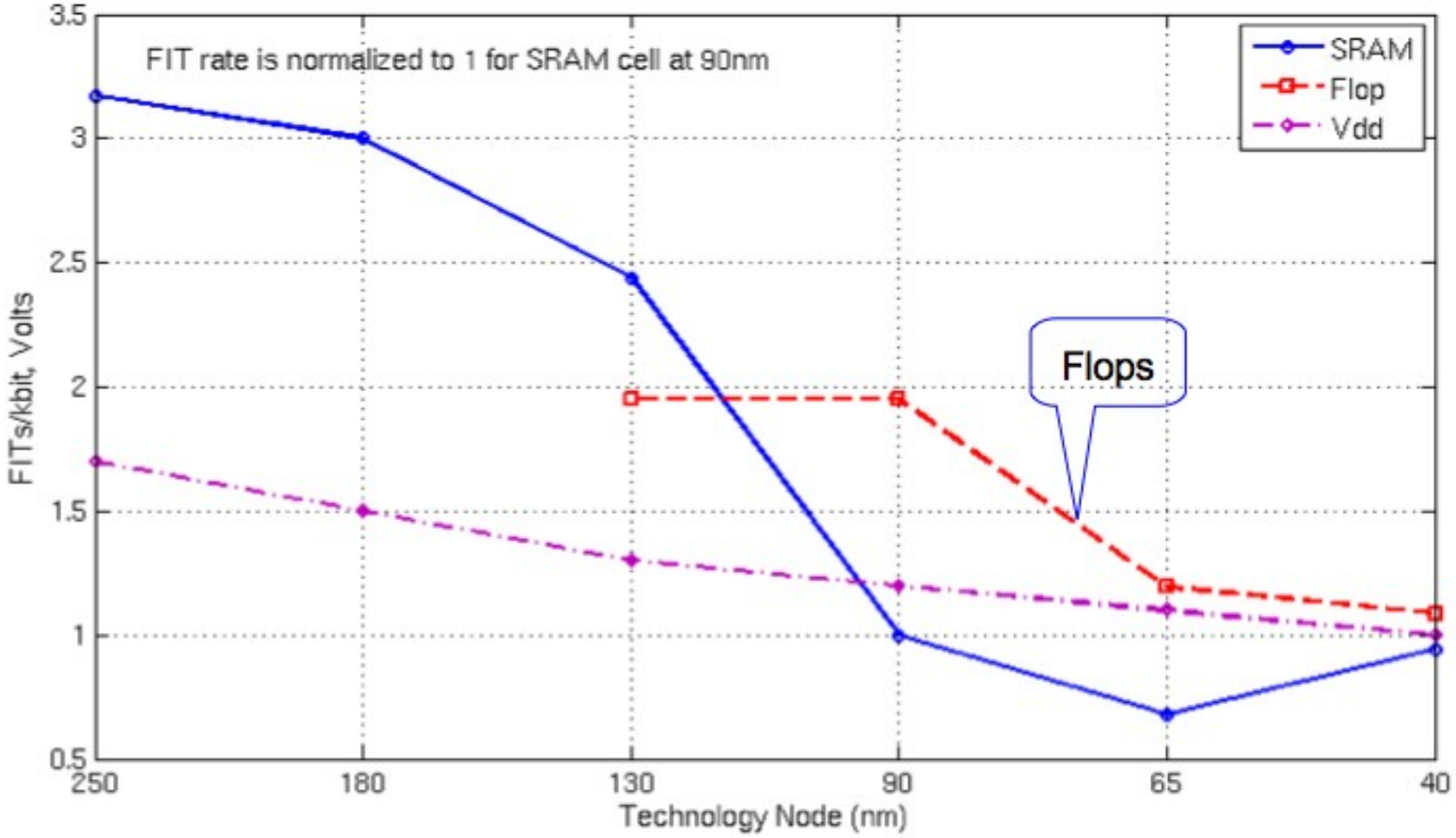
Source: Anand Dixit, Raymond Heald, and Alan Wood, “The Impact of New Technology on Soft Error Rates”, SELSE-6, Stanford, 2010

SRAM SER Trend- AMD



Source: Seth Prejean, “Accelerated Neutron Soft Error Rate Testing of AMD Microprocessors”, SELSE-6, Stanford, 2010

SRAM and Logic SER Trend- Sun



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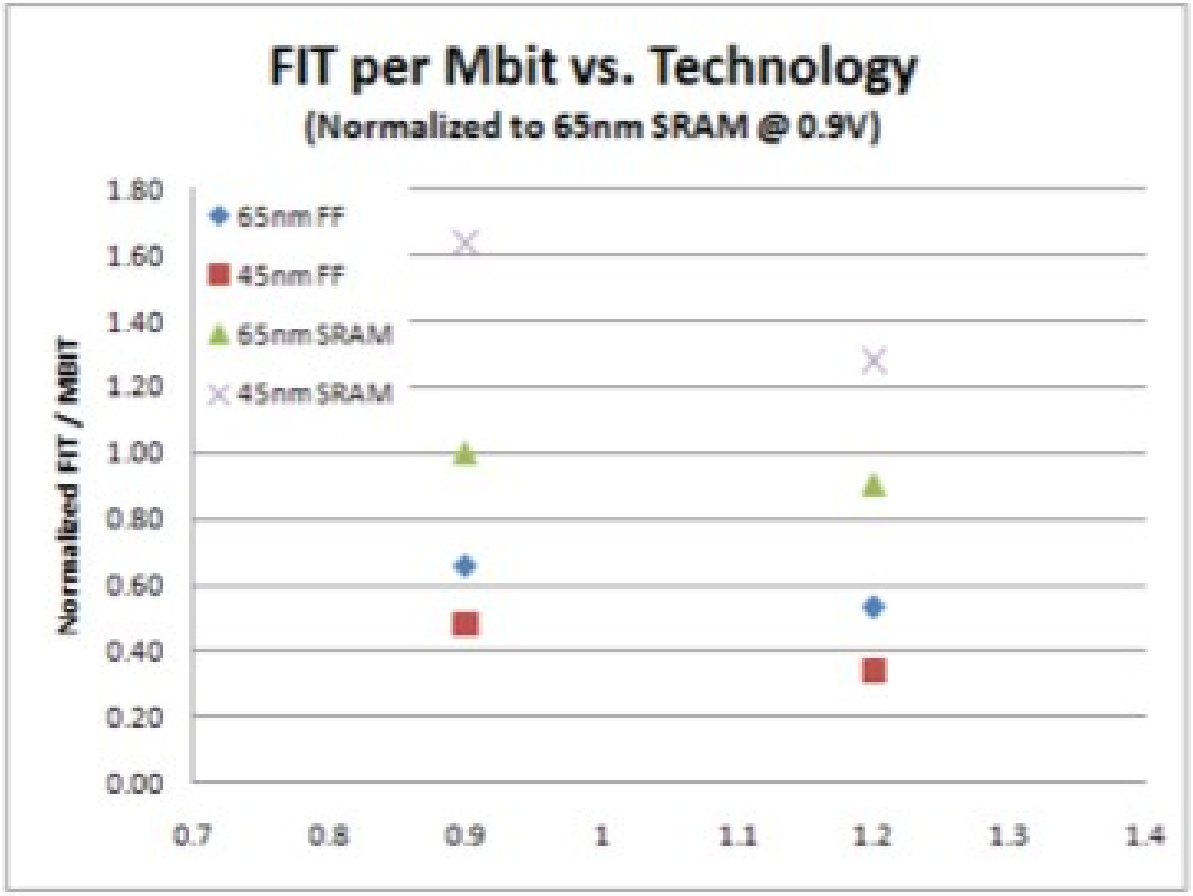
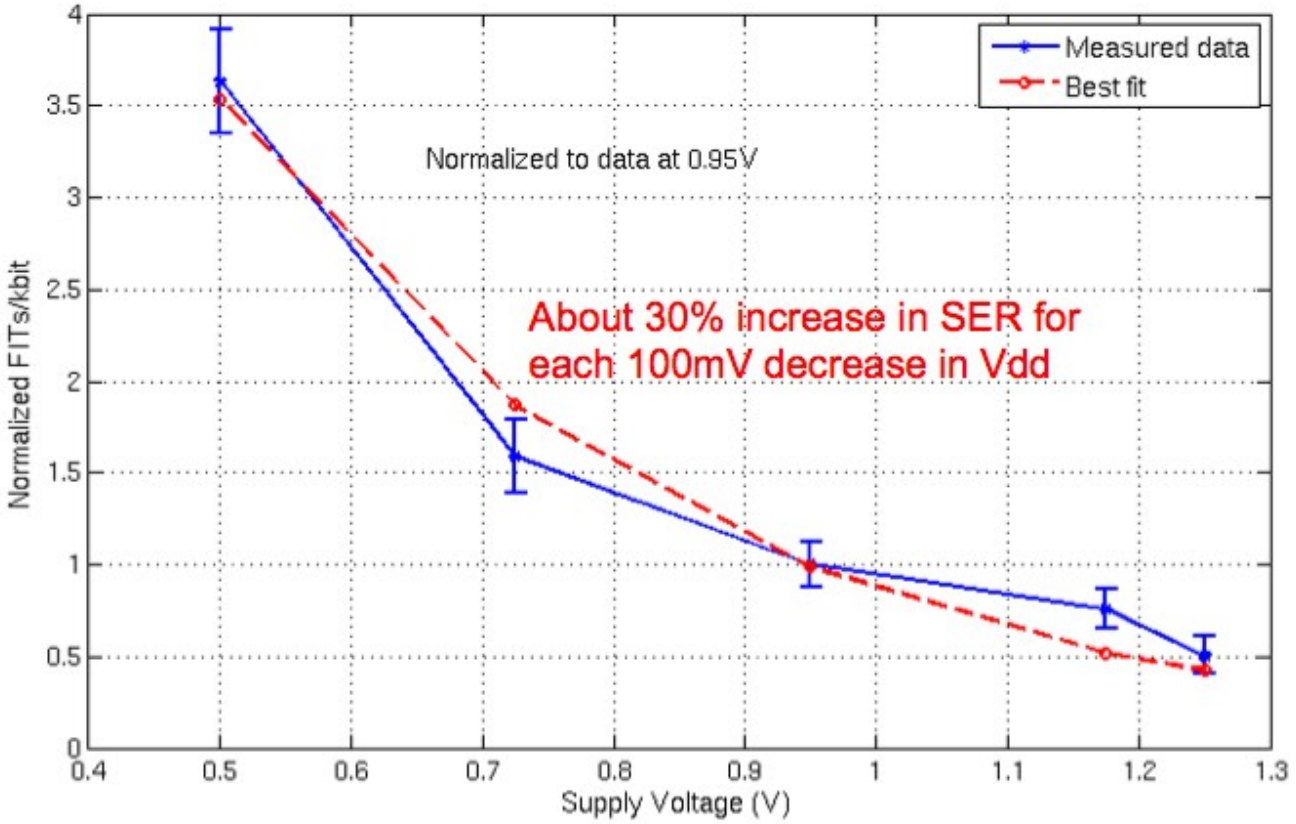
SRAM and Logic SER Trend- AMD



Source: Seth Prejean, "Accelerated Neutron Soft Error Rate Testing of AMD Microprocessors", SELSE-6, Stanford, 2010

Logic SER Trend as a Function of Voltage



Source: Anand Dixit, Raymond Heald, and Alan Wood, "The Impact of New Technology on Soft Error Rates", SELSE-6, Stanford, 2010

SER Trend Explanation

Vdd ↓ → Critical Charge ↓ → SER ↑

Area ↓ → Sensitive depletion region ↓ → SER ↓

SER α Area * exp(-Qcrit/Qcoll)

Linear with Area; Exponential with Vdd

Source: Anand Dixit, Raymond Heald, and Alan Wood, “The Impact of New Technology on Soft Error Rates”, SELSE-6, Stanford, 2010

Microprocessor SER Trend- Sun

Tech. (nm)	Relative SEU in FITs/kbit	Mbits/Processor	Relative uncorrected SEU/Processor
250	3.2	1.52	5.0
180	3.0	1.52	4.3
130	2.4	3.28	7.9
90	1.0	33.6	33.6
65	0.7	44.3	30.5
40	0.94	71	67.0

Reflects processor design over the years

Source: Anand Dixit, Raymond Heald, and Alan Wood, "The Impact of New Technology on Soft Error Rates", SELSE-6, Stanford, 2010