Fault Tolerant Communication in 3D Integrated Systems

Vladimir Pasca, **Lorena Anghel, Mounir Benabdenbi**

TIMA Laboratory

Outline

- 3D Integration
  - Opportunities
  - Challenges and Solutions
- Fault Tolerant Communication in 3D Systems
- Experimental results
- Conclusion and Future Work

Increasing Computational Demands for Future Multimedia Applications

Year	Number of Processing Engines
2007	32
2008	44
2009	58
2010	79
2011	101
2012	126
2013	161
2014	212
2015	268
2016	348
2017	424
2018	526
2019	669
2020	878
2021	1023
2022	1435

Logic, Memory Size (Normalized to 2007)

# of Processing Engines

GOPS: 0.01, 0.1, 1, 10, 100

Video: MPEG1, MP/ML, MPEG2, MP/HL, JPEG, MPEG4, H.264, DivX

Graphics: 3D rendering, 10Mpps, 100Mpps, 2D rendering, 3D image extraction

Audio Voice: AAC, Dolby-AC3, Sentence Translation, MPEG, WMA, Word Recog., Voice Recognition, Voice Translation

Recognition Comm.: VoIP modem, Face Recognition, Data modem, FAX, Voice-print Rec., Eye Recog., Video Recognition

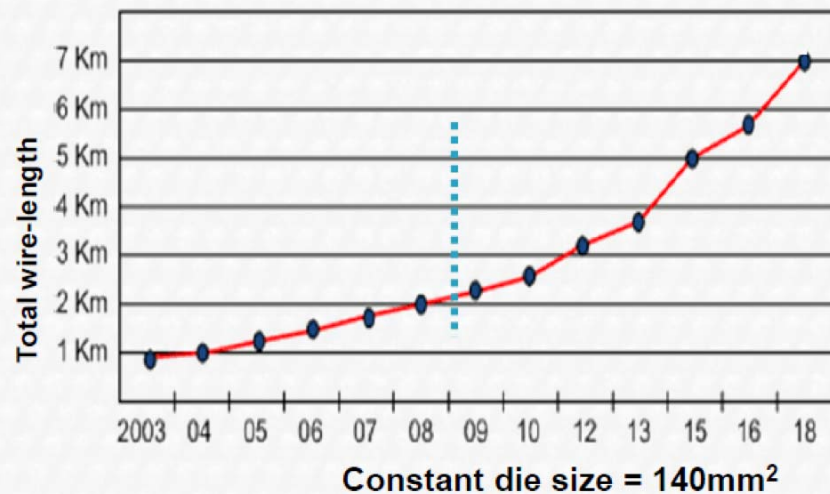
Number of Processing Engines (Right Y Axis)

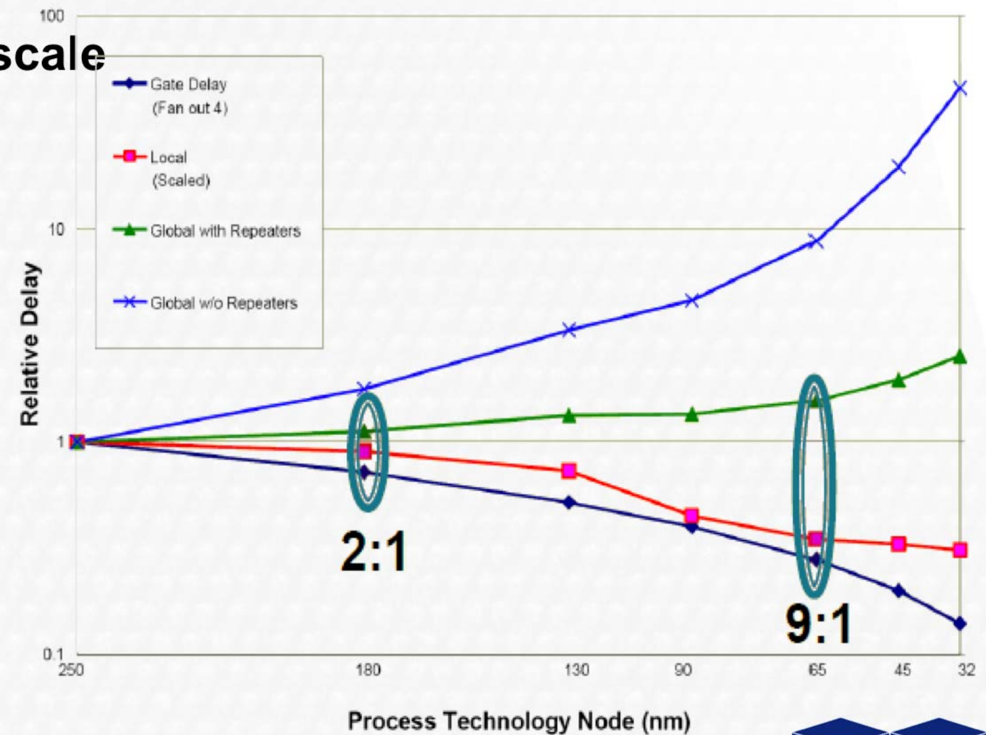
Total Logic Size (Normalized to 2007, Left Y Axis)

Total Memory Size (Normalized to 2007, Left Y Axis)

Global Interconnect Performance Bottleneck Problem

- **RC delay increases exponentially**
  - In 65nm technology, RC delay of 1mm wire at minimum pitch = 100X NMOSFET delay
- **Increasing dynamic power consumption on wires**
  - 51% of dissipated power on wires
- **Global interconnect length does not scale**
  - Chip size ~constant
  - Longer wires

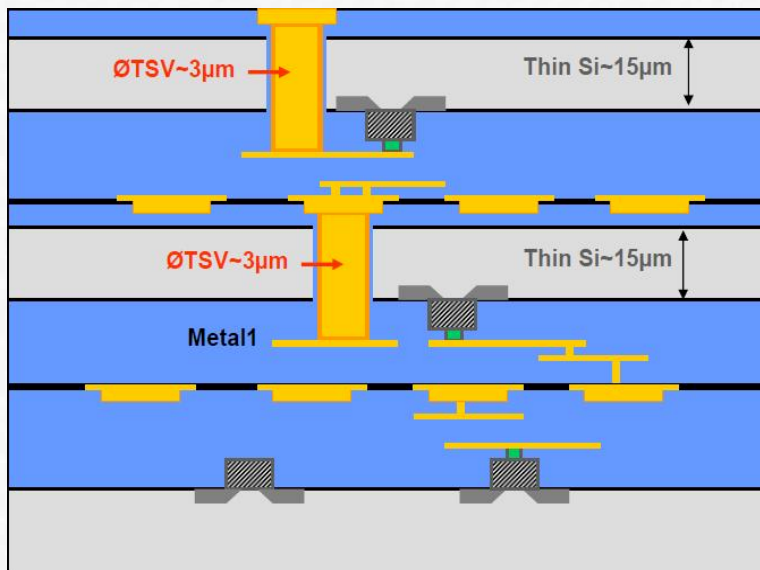


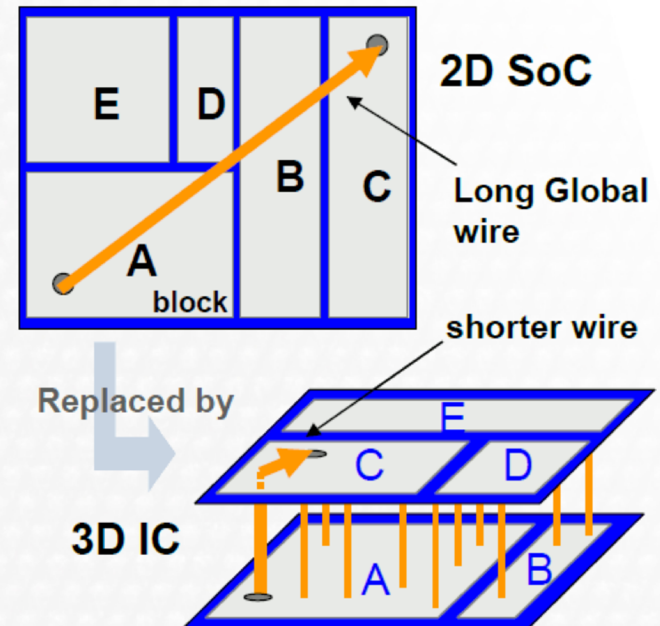


ITRS'07

3D TSV Integration

- **Stack active silicon layers (CMOS, CIS, RF, etc.)**
- **Connect layers with Thru-Silicon Vias (TSV)**
  - Replace long *(~mm)* global 2D interconnects with shorter *(~10s µm)* TSV
    - » Reduce RC delays
    - » Reduce power dissipation

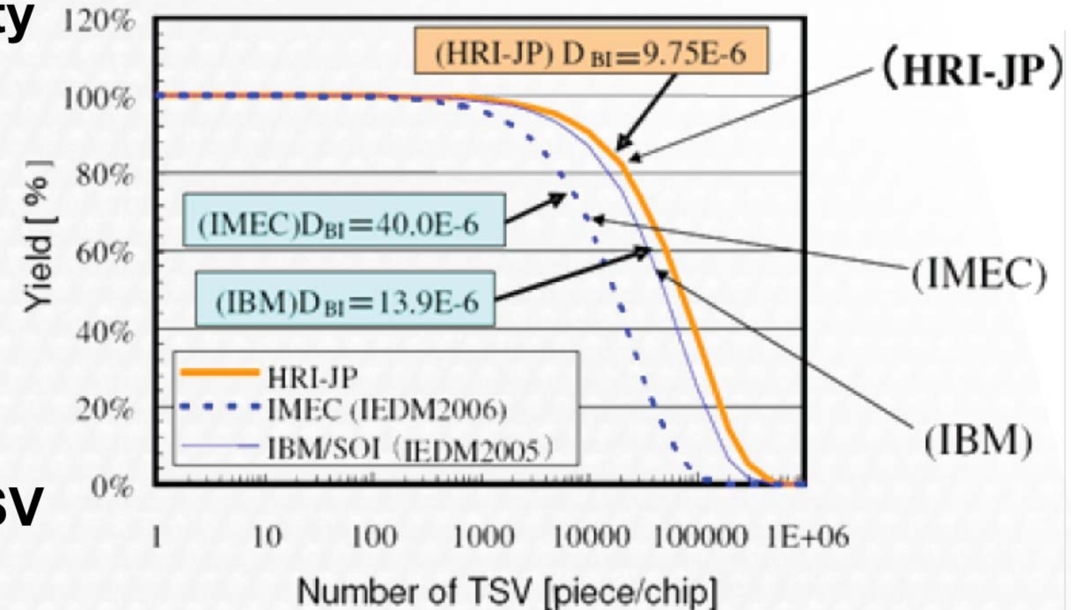




(Source: P. LEDUC - D43D 2009)

Challenges of 3D TSV Integration

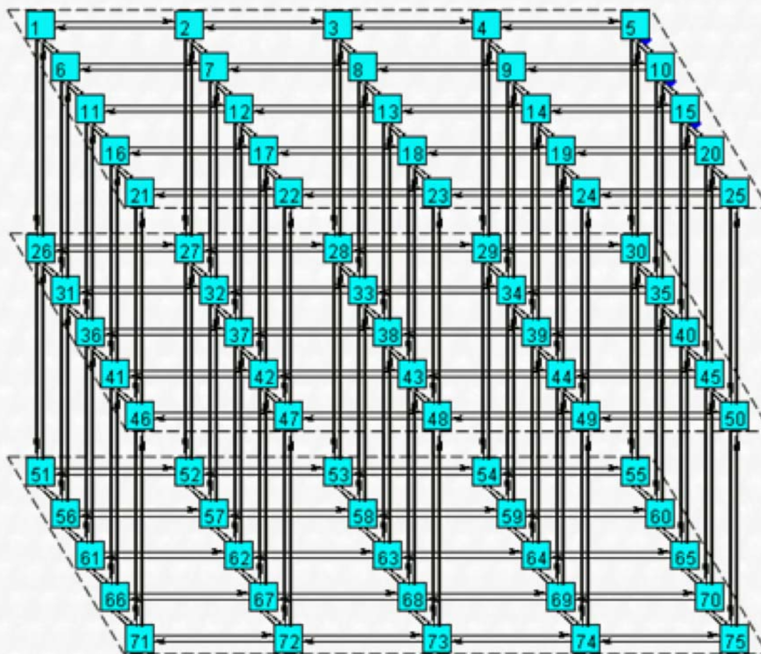
- **Poor TSV Yield and Reliability**
  - High TSV defect rates
    - » XY misalignment
    - » Tilted Z alignment
    - » Void formation
    - » Height variation, etc.
- **Sub-optimal High Density TSV process**
  - TSV pitch between 1 and ~tens µm
- **Heat Removal and Thermal Management**
- **Development and manufacturing cost**



(Source: I. LOI - ICCAD 2010)

3D Integration and Systems-on-Chip

- **SoC interconnect fabric**
  - Scalable
  - Good performance metrics
    - » Latency
    - » Bandwidth
    - » Throughput



- **3D SoC interconnect fabric**
  - Nodes connected by *LINKS*
  - Adaptable to the IP block and TSV distribution
  - Mix of interconnect technologies
    - » M_9-M_7 for horizontal (intra-die) links
    - » TSV for vertical (inter-die) links
  - Examples:
    - » 3D Network-on-Chip
    - » Vertical Bus
    - » Hybrid approaches

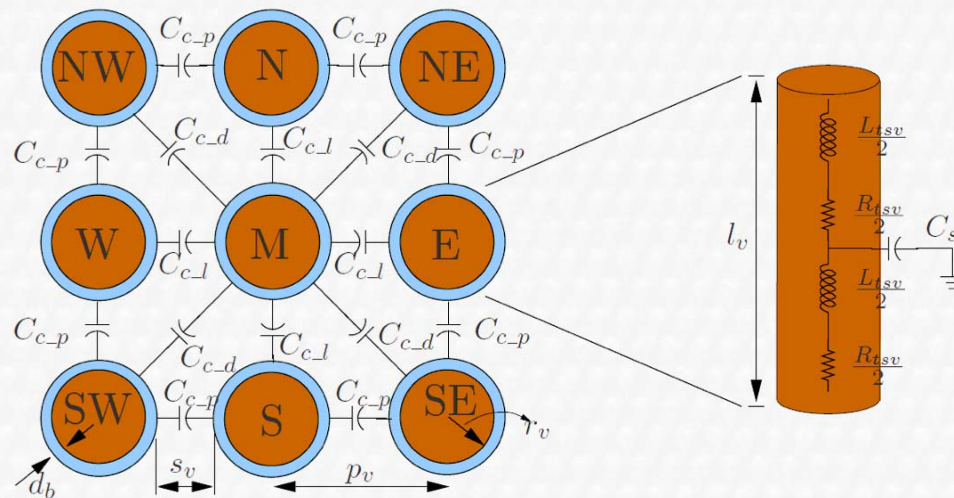
Vertical Communication Challenges and Solutions

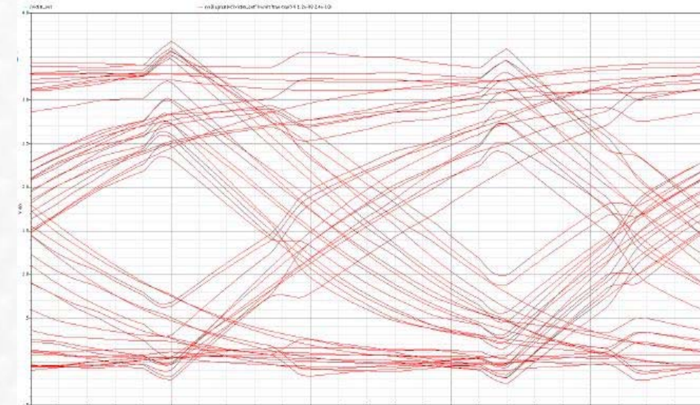
- **High TSV defect rates**
  - Dynamic Hardware Redundancy
    - » Loi ICCAD'08, Hu ISSCC'09: TSV repair
- **Noise**
  - Grange'08: TSV shielding
  - Coding (?)
- **3D clock distribution trees**
  - Inter-layer desynchronization
    - » Loi DATE'09: mesochronous communication
    - » Darve DATE'10: asynchronous serial link
- **Low TSV density**
  - Serial communication
    - » Pasricha DAC'09: high speed serial links
  - Partial vertical connectivity
    - » Bartzas WASP'07, Rusu NORCHIP'09

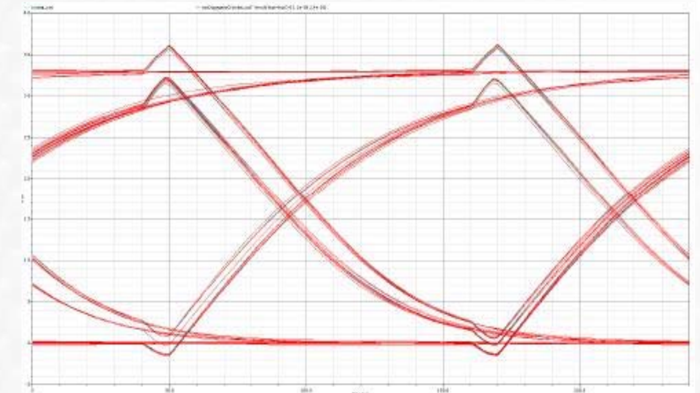
Noise in 3D Integrated Systems

- High Self- & Mutual Wire Coupling
  - Manufacturing defects
  - Process Variation

- Solution
  - TSV Shielding







(Source: M. Grange DATE'09)

TSV Manufacturing Defects

- **Fault Model**
  - Open
  - Short
  - High Capacitance (high delay)
- **Detect faulty TSV**
  - Interconnect Tests (e.g. Grecu VTS'06)
- **Replace faulty TSV with functional spare**
  - 2:1 repair – 1 repair TSV for every 2 functional (Kang ISSCC'09)
  - 4:2 repair – 2 repair TSVs for every 4 functional (Kang ISSCC'09)
  - TSV Doubling: 1 redundant TSV for every 1 functional
  - TSV Tripling: 2 redundant TSVs for every 1 functional
  - Loi: redundant TSV for every column in TSV bundle (ICCAD'08)

Yield improvement by TSV redundancy

Assumptions:
- 1000 functional TSVs
- Non-correlated TSV defects

Total TSV Chip Stack Yield

Legend:
- Base
- 2:1 Repair
- 4:2 Repair
- 1:1 Doubling
- 1:2 Tripling

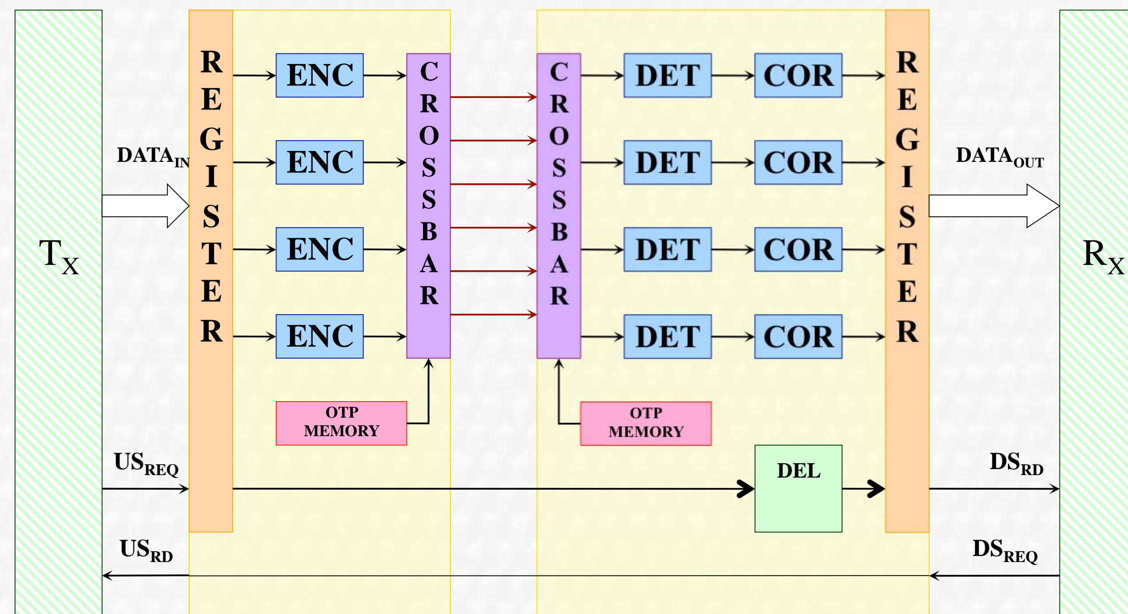
Total TSV Yield: 0%, 10%, 20%, 30%, 40%, 50%, 60%, 70%, 80%, 90%, 100%

Single TSV Yield: 90%, 91%, 92%, 93%, 94%, 95%, 96%, 97%, 98%, 99%, 100%

(Source: D. Velenis IMEC DATE'09)

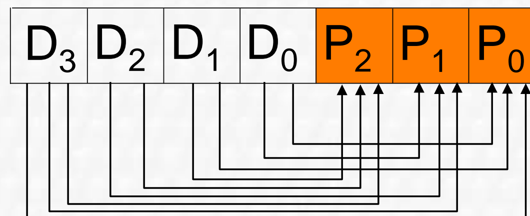
Fault Tolerant Vertical Link

- Encode data bits with error correction codes
- Map code bits on fault free TSV
  - Link configuration
    - After TSV interconnect tests
    - Use the test diagnosis vector to replace faulty TSV with spares



Single Error Correction Coding

- Information redundancy
  - Append error check bits
    - » P_2-P_0
  - Correct any single error
    - » D_3-D_0P_2-P_0



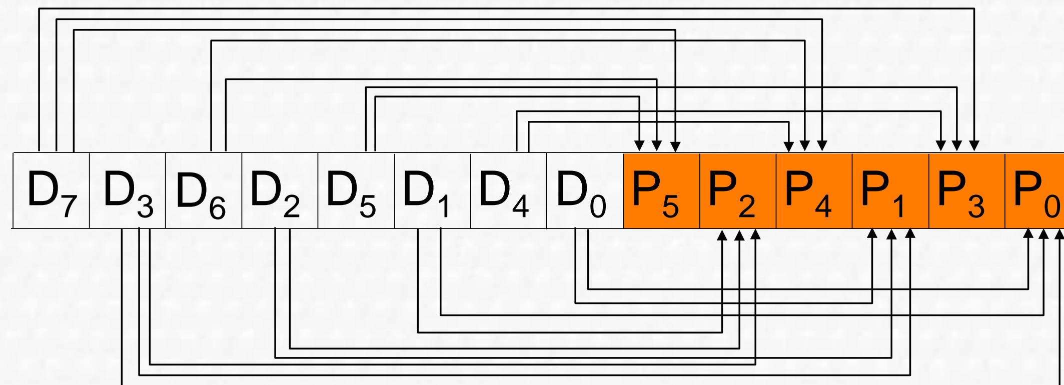
- Code Bits
  - Data Bits + Error Check Bits
  - Data Bits x Generator Matrix G

$$G_{(7,4)} = \begin{bmatrix} 1 & 0 & 0 & 0 & 1 & 1 & 1 \\ 0 & 1 & 0 & 0 & 1 & 1 & 0 \\ 0 & 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 1 & 0 & 1 & 1 \end{bmatrix}$$

- Examples
  - Hamming / Extended Hamming
    - » Detect multiple errors and correct single errors
    - » Data bit D_i checked by parity bit P_j iff i expressed using 2^j
  - Hsiao
    - » Detect multiple errors and correct single errors
    - » Optimized implementation for minimal area/power/delay

Block / Interleaved Single Error Correction Coding

- 3D integrated systems
  - High noise levels & high inter-wire coupling
    - » HIGH TRANSIENT ERROR RATE !
    - » BURST TRANSIENT ERRORS !
  - Multiple error correction capabilities
    - » Split transmitted data in smaller groups
    - » Interleave coded data bit groups

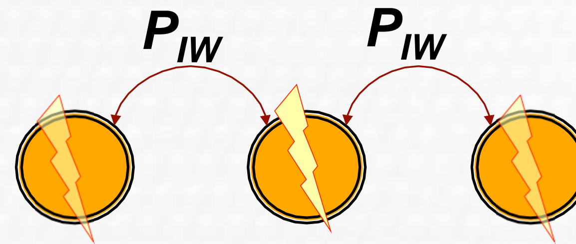


How many groups ?

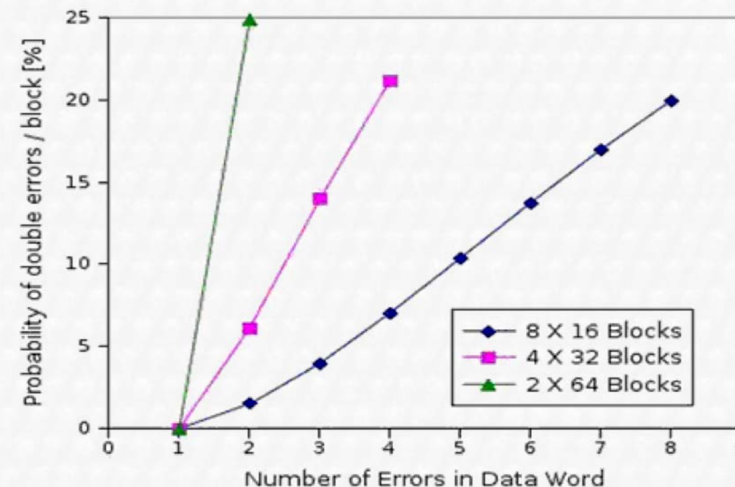
- **Noise**
  - Normal Gauss distribution: σ_{N}, μ_{N}
  - Error probability on a single wire ε
    - » V_{DD} voltage swing
  - Inter-wire coupling
    - » Burst error probability

$$\varepsilon = \int_{\frac{V_{dd}}{2\sigma_N}}^{\infty} \frac{1}{\sqrt{2\pi}} e^{-x^2/2} dx$$

(Hedge TVLSI'2000)

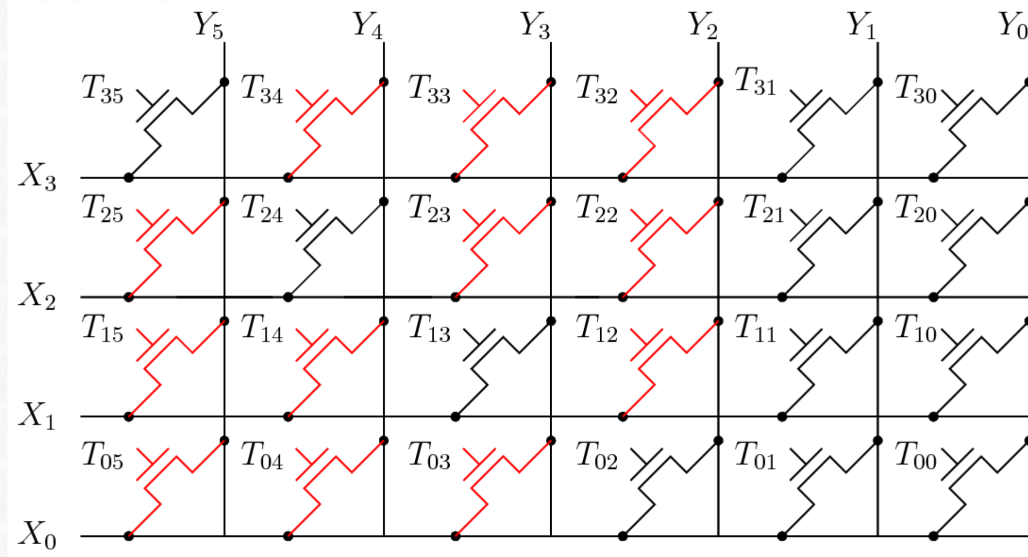


- **M-bit burst error probability**
  - Find M: P(M) < P_{TH} (e.g. 1e-8)
  - Split data in M groups
  - Correct up to M errors



TSV Spare and Replace

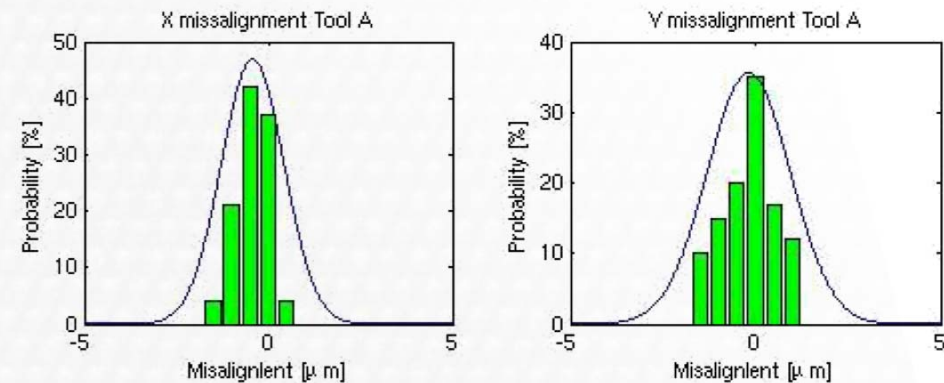
- **TSV Fault models**
  - Open: non-conducting
  - Short: leaking
  - Delay: high capacitance
- **TSV Repair**
  - Detect faulty TSV
    - » Interconnect Tests



  - Remap transmitted data bits on fault free TSVs
    - – Configuration logic
      - » MUX / DEMUX
      - » Crossbar (full or partial)
    - – One-time-programmable memory

How many spares ?

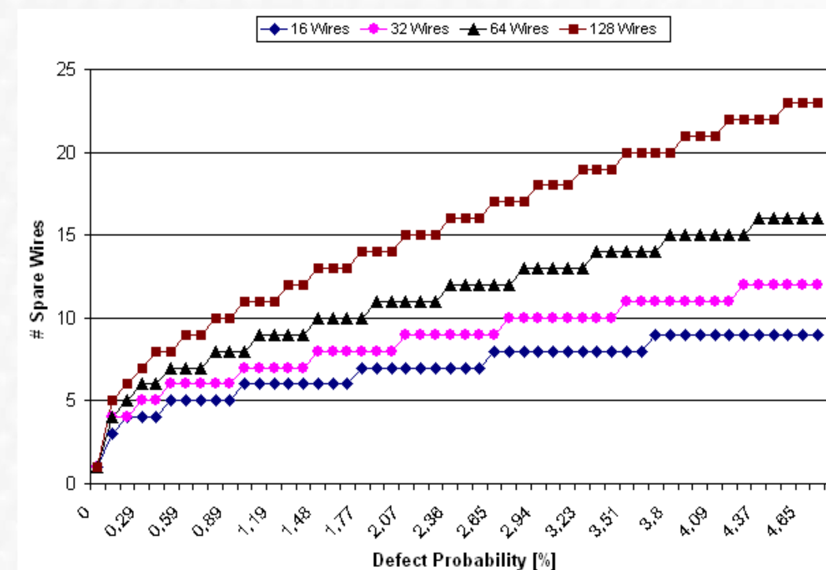
- **Misalignment defect**
  - Normal distribution with TSV pitch
- **Single TSV defect probability**
  - P_{WIRE}



(Source: P. Leduc IITC'07)

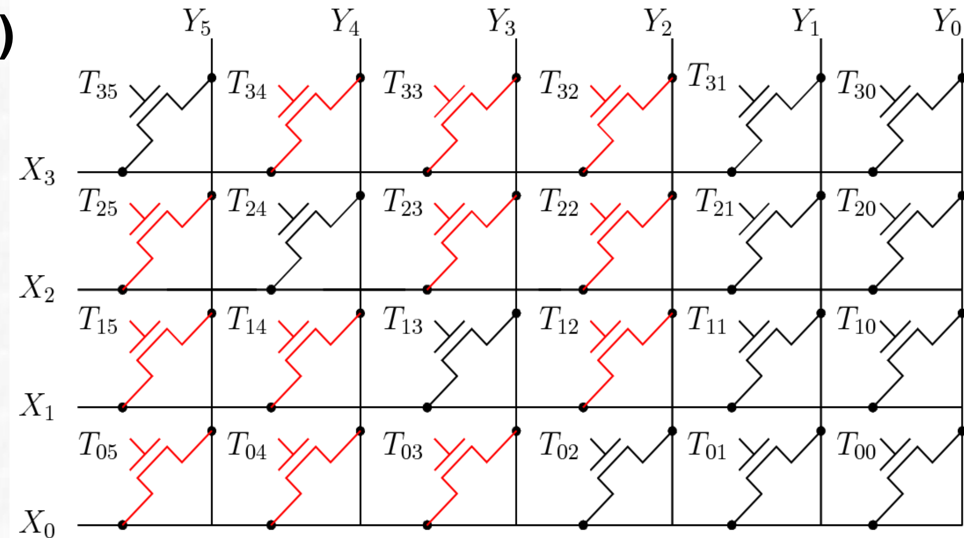
- **N wires with R spares**
  - At least N functional TSV
  - Target yield Y
  - Find R such that:

$$Y \leq \sum_{i=N}^{N+R} C_N^i (P_{WIRE})^i (1 - P_{WIRE})^{N+R-i}$$



Matrix control signal generation

- **Interconnect test diagnosis vector (DV)**
  - Identifies faulty TSVs
- **Control signal T_{IJ}**
  - Map data bit X_i on TSV Y_j
  - Iff functional TSV Y_j
  - Iff X_i is not mapped on other TSVs
  - Iff no other bit is mapped on Y_j



$$T_{ij} = \overline{DV_J} \bullet \overline{T_{i,N+R-1} + \ldots T_{i,j+1}} \bullet \overline{T_{N-1,j} + \ldots + T_{i+1,j}}$$

- For faulty TSV Y_4

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \end{bmatrix}$$

- For faulty TSV Y_2

$$\begin{bmatrix} 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$

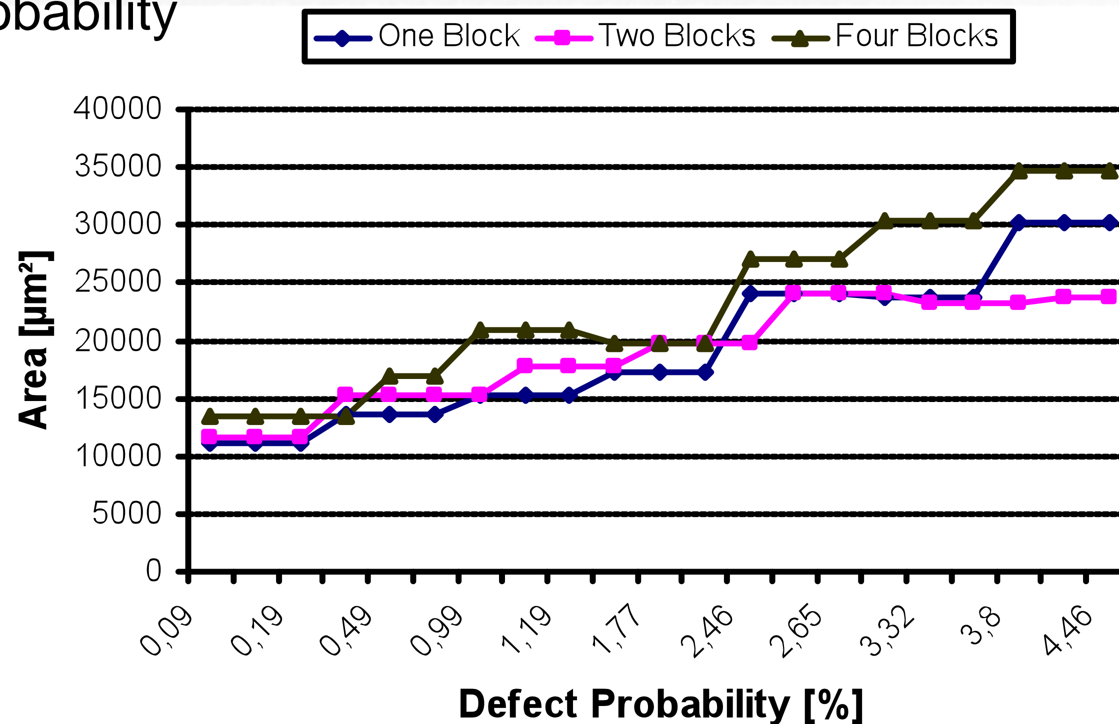
Experimental Results

- **Impact of fault tolerance on**
  - **Link area**
  - **Link dissipated power**

- **Experimental Setup**
  - 65nm technology
  - TSV fault rates up to 5%
  - 1-bit, 2-bit and 4-bit transient errors
    - » SEC code: Extended Hamming
    - » One / Two / Four SEC blocks
  - **Ignore area penalty of spare TSVs**

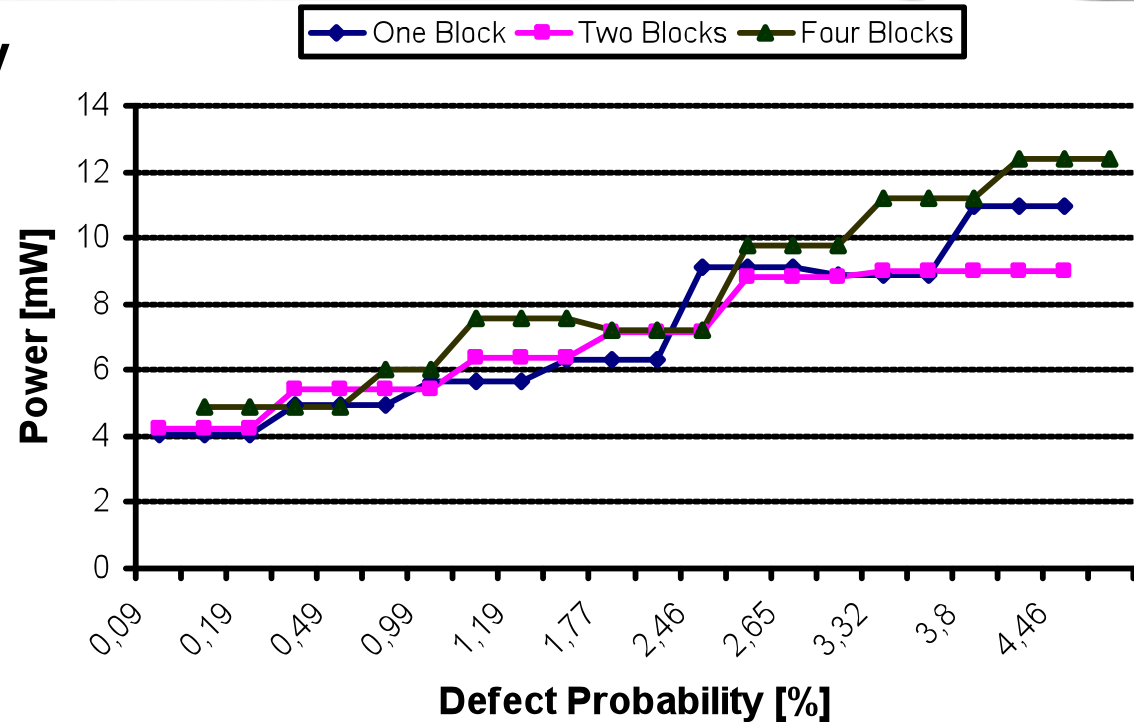
Link Area

- Increase burst error probability
  - Area overhead ~30%
    - » Extra coding / detection / correction modules
    - » More spares for targeted yield
- Increases defect probability
  - More spares
  - Area OH
    - » ~300%



Link Dissipated Power

- **Increases defect probability**
  - Larger crossbars
    - » More TSV spares
  - Power OH
    - » Up to ~300%



- **Increase burst error probability**
  - Power overhead up to ~30%
    - » Extra coding / detection / correction modules
    - » Larger crossbars (more spares for targeted yield)

Conclusion and Future Work

- **TSV interconnects**
  - Joint transient and permanent faults mitigation
    - » Interleaved SEC coding
    - » TSV spare & replace

- **High TSV fault rates ➔ high overheads (up to ~300%)**

- **Future work**
  - Unavailable spare TSV ➔ Serial transmission
    - » Avoid high spare TSV area penalty

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Additional Slides: TSV Pitch