The 40th Annual IEEE/IFIP International Conference on Dependable Systems and Networks

June 28-July 1, 2010 — Chicago, IL, USA

Fourth Workshop on Dependable and Secure Nanocomputing

Organizers:

- **Jean Arlat**, LAAS-CNRS
- **Cristian Constantinescu**, AMD
- **Ravishankar K. Iyer**, UIUC
- **Johan Karlsson**, Chalmers Univ.
- **Michael Nicolaïdis**, TIMA

Monday June 28, 2010

Where Do We Stand?

The "More Moore" (Top-Down) Trend

- Process variations ↗
- Manufacturing (lithography, testing) costs ↗
- Yield ↘
- Prob. defects get undetected ↗
- Impact of defects ↗

- Frequency ↗, Power dissipation ↗
- Parameter variation ↗
- Power supply voltage ↘
- Soft Error Rate ↗

Some Further Rationale

- **ITRS (International Technology Roadmap for Semiconductors)**
  - 2008 Edition: Crosscutting Challenge 5: Reliability
  - 2009 Edition: Crosscutting Challenge 5: Reliability & Resilience
- **Quoting the Design Section [http://www.itrs.net]**
  - *Relaxing the requirement of 100% correctness for devices and interconnects may dramatically reduce costs of manufacturing, verification, and test.*
  - *Such a paradigm shift will likely be forced in any case by technology scaling, which leads to more transient and permanent failures of signals, logic values, devices, and interconnects.*
  - *In general, automatic insertion of robustness into the design will become a priority as systems become too large to be functionally tested at manufacturing exit.*
  - *Potential solutions include automatic introduction of redundant logic and on-chip reconfigurability for fault tolerance, development of adaptive and self-correcting or self-healing circuits, and software-based fault-tolerance.*

About Previous Events

- 1st Edition at DSN-2007: Raising up the Awareness
- 2nd Edition at DSN-2008: Bringing up a Community
- 3rd Edition at DSN-2009: Link with IOLTS Community
  -> 42 attendees (academia and industry) from 18 countries
- 4th Edition at DSN-2010: Link with European Test Symp. Community
  -> Special focus session on testing of statistical and variation-tolerant design
  -> Papers to be available via IEEE Xplore

www.laas.fr/WDSNxx, xx ∈ {07,08,09,10}

WDSN-10 Special Focus

Massive Statistical Process Variations:
A Grand Challenge for Robustness in Nanoelectronics

Four presentations focusing on testing of statistical and variation-tolerant design.

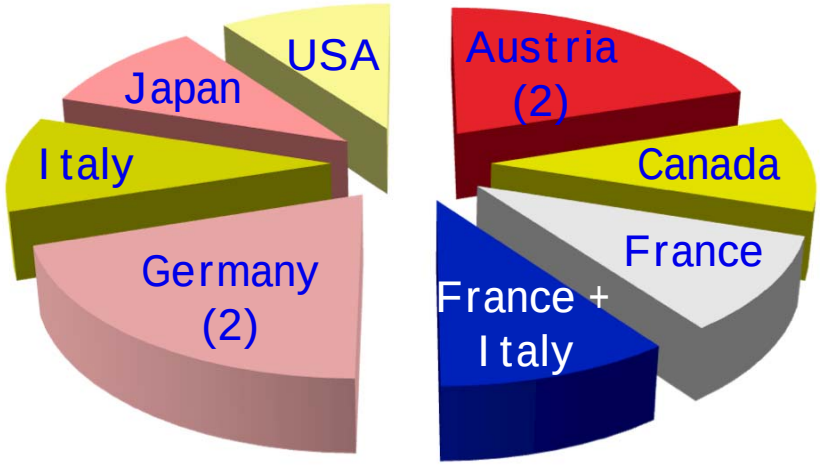
- Statistical Process Variations: Models and Algorithms
- Statistical Test Methods
- Algorithmic Foundations
- Quality Binning – how to maximize yield under robustness constraints.

Program Committee

Davide Appello	STMicroelectronics, Agrate Brianza, Italy
Vikas Chandra	ARM R&D, San Jose, CA, USA
Abhijit Chatterjee	GeorgiaTech, Atlanta, USA
Yves Crouzet	LAAS-CNRS, Toulouse, France
Babak Falsafi	EPFL, Lausanne, Switzerland
Eishi Ibe	Hitachi Ltd, Yokohama, Japan
Régis Leveugle	TIMA, Grenoble, France
Cecilia Metra	University of Bologna, Italy
Helia Naeimi	Intel Corporation, Santa Clara, CA, USA
Takashi Nanya	University of Tokyo, Japan
Jean-Jacques Quisquater	Univ. Cath. Louvain, Belgium
Juan Carlos Ruiz García	Univ. Politécnica de Valencia, Spain
Andreas Steininger	Vienna University of Technology, Austria
Arnaud Virazel	LIRMM, Montpellier, France
Alan Wood	Sun Microsystems, Santa Clara, CA, USA
Hans-Joaquim Wunderlich	University of Stuttgart, Germany
Tomohiro Yoneda	National Institute of Informatics, Tokyo, Japan

Program Set up

- **10 submissions**
  - **9 regular submission**
  - **1 special session proposal**



- **Regular submissions reviewed by 3+ PC members**
- **Selection —> 8 presentations from regular submission**
- **1 Special focus session**

Program-at-a-Glance

Moderator

1 - Opening.....**Cristian Constantinescu**

8:30 - 8:40 Workshop Introduction, *Jean Arlat and Johan Karlsson*

8:45 - 10:00 Special Focus Session, *B. Becker, S Hellebrand, I. Polian, B. Straube, W. Vermeiren, H.-J. Wunderlich*

10:00 - 10:30 Coffee break

2 - Soft Errors and Intermittent Faults.....**Alan Wood**

10:30 - 11:45 *Layali Rashid, Warin Sootkaneung, (Oscar Ballan)*

11:45 - 12:00 Additional Discussion

12:00 - 13:30 Lunch

3 - Fault Tolerant Architectures..... **Helia Naeimi**

13:30 - 14:50 *Masahshi Imai, Tomas Panhofer, Vladimir Pasca*

14:50 - 15:00 Additional Discussion

15:00 - 15:30 Coffee break

4 - Robustness Enhancement & Trust Management .....**Takashi Nanya**

15:30 - 16:20 *Marcus Ferringer, Thilo Piontek*

Workshop Wrap-Up .....**Jean Arlat, Cristian Constantinescu, Johan Karlsson**

16:20 – 17:15 Discussion on Grand Challenges in Dependable Nanocomputing

All **17:15** Workshop Adjourn

Wrap-Up Discussion

- **Goal:**

  To produce a list of Grand Challenges in Dependable Nanocomputing
  - Elaboration of Grand Challenges from ITRS-2009
  - Non-exhaustive list – Focus on problems brought in the presentations

- **Areas of interest (examples):**
  - Circuit Design
  - Multi-core architectures
  - Testing
  - Fault Tolerance
  - Fault and failure models
  - Dependability prediction and assessment