4th Workshop on Dependable and Secure Nanocomputing

Call for Contributions — Deadline extended until March 15, 2010

Monday June 28, 2010 — Chicago, IL, USA

in conjunction with the 40th Annual IEEE/IFIP International Conference on Dependable Systems and Networks — DSN-2010

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Important Dates

NEW!

- **Papers due:** March 15, 2010
- **Acceptance notification:** April 12, 2010
- **Final version due:** May 3, 2010

Further Information

- About DSN-2010 and the venue: **www.dsn.org**
- About the Workshop: **www.laas.fr/WDSN10** or contact the organizers via: **dsn2010-nanocomputing[at]laas.fr**
- About the previous editions of the Workshop: **www.laas.fr/WDSN##** [with ## ∈ {07,08,09}]

Motivation and Objectives

Nanocomputing technologies hold the promise of higher performance, lower power consumption as well as increased functionality. However, the dependability of these unprecedentedly small devices remains uncertain. The main sources of concern are:

- Nanometer devices are expected to be highly sensitive to process variations. The guard-bands used today for avoiding the impact of such variations will not represent a feasible solution in the future. As a consequence timing errors may occur more frequently.
- New failure modes, specific to new materials, are expected to raise serious challenges to the design and test engineers.
- Environment induced errors, like single event upsets (SEU), are likely to occur more frequently than in the case of conventional semiconductor devices
- New hardware redundancy techniques are needed to enable development of highly energy efficient systems.
- The increased complexity of the systems based on nanotechnology will require improved computer aided design (CAD) tools, as well as better validation techniques.
- Security of nanocomputing systems may be threatened by malicious attacks targeting new vulnerable areas in the hardware.

Hardware implemented fault tolerance features are becoming employed widely for dealing with these dependability issues. The use of error correcting codes, as well as space and time redundancy, is expected to significantly increase. Providing high dependability to the end users also requires improved error reporting, recovery, and system manageability. As a consequence the role of software solutions will increase. Software will also play the leading role in the improvement of design and validation tools. Furthermore, improved parallel processing programming paradigms are needed due to the advent of multicore processors. We believe DSN is the appropriate venue for discussing these challenges and potential solutions.

Scope and Topics

For this year's edition, we would like to focus the Workshop on **Architecting, Designing, Manufacturing, and Assessing Dependable Nanocomputing Systems**, with a special attention being paid to the following topical areas:

- Nanocomputing architectures for high dependability;
- Design and validation techniques for coping with increased complexity;
- Manufacturing nanodevices;
- Failure mode analysis and testing issues specific to nanoscale computers.

Contributions related to these main topics will allow the Workshop to continue the debate on the issues posed by nanocomputing, as well as the best solutions for providing highly dependable systems and networks to the end users. In addition to the diverse set of problems addressed in the previous editions, including issues related to process variations, aging, particle radiation and security vulnerabilities, this year we would like to encourage contributions on new CAD tools and validation techniques, and the mitigation of impairments related to power dissipation and reduced energy consumption.

Participation, Submission and Selection Process

The Workshop is open to all researchers, system developers and users who are involved with or have an interest in dependability and security of hardware technologies. Both invited and submitted contributions will be included in the Workshop program. We are interested in contributions from both industry and academia on all topics related to dependable and secure nanocomputing. Potential topics of interest include, but are not limited to: failure modes and risk assessment, yield and mitigation techniques in nanoscale technologies, on-line adaptive and reconfigurable nanoarchitectures, design techniques for developing resilient nanosystems, fault-tolerant architectures specific to nanoscale circuits, scalable verification and testing methodologies, network on chip and communication protocols, etc. All prospective contributors should submit an extended abstract, work-in-progress report or position paper, in PDF format, via the Workshop Webpage at: **www.laas.fr/WDSN10**.

Submissions must be original work with no substantial overlap with previously published papers or simultaneous submissions to a journal or conference with proceedings. The submissions should conform to the proceedings publication format (IEEE double-column conference style) and should not exceed six pages (including all text, references, appendices, and figures). They should explain the contribution to the field and the novelty of the work, making clear the current status of the work. Each submission should start with a title, a short abstract, and names and contact information of the authors. Submissions will be fully refereed by three PC members. Authors of accepted papers must guarantee that their paper will be presented at the Workshop. Accepted papers will be published in a supplement volume of the DSN 2010 proceedings. Outstanding contributions will be offered the opportunity of submitting extended versions to appear into an edited book.

Update: February 27, 2010