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Third Workshop on Dependable and Secure Nanocomputing
Monday June 29, 2009, Estoril, Lisbon, Portugal **www.laas.fr/WDSN09**

Invited Talk Session (8h30-10h)

Dependable Design in Nanoscale CMOS Technologies: Challenges and Solutions

Vikas Chandra
ARM R&D, San Jose CA, USA
vikas.chandra@arm.com

Abstract. With nearly three decades of continued CMOS scaling, the devices have now been pushed to their physical and reliability limits. Imperfections in manufacturing are unavoidable due to atomistic scale of nanoscale devices. With technology scaling, early life failures are becoming increasingly common due to random manufacturing defects and SEUs are of great concern during the normal lifetime of the design. Designs manufactured correctly will wearout and become unreliable over time because of mechanisms like NBTI and gate oxide breakdown. The impact of unreliability results in time-dependent variability, where the electrical characteristics of the devices will vary statistically in a temporal manner, directly translating into design uncertainty in manufactured chips. Further, dynamic variations in voltage and temperature will induce variability in the performance of the design. Design techniques which can adapt to these variations can make the design more resilient by mitigating errors on the fly. The three components of adaptive design techniques are failure prediction, failure detection and failure recovery. Adaptive design techniques with particular emphasis on error-tolerant techniques will be reviewed.

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Vikas Chandra is a Staff Researcher in the Corporate R&D group at ARM. He received his Ph.D. and M.S. degrees in Electrical and Computer Engineering from Carnegie Mellon University (CMU). He has worked at Intel's Strategic CAD Labs, IBM Austin Research Lab and the Central R&D group at STMicroelectronics. Dr. Chandra has presented a tutorial at the VLSI Design Conference 2009 and has published papers at prestigious international conferences like ICCAD, DATE, ISFPGA, ICCD, etc. He has two approved US patents and three patents pending. Dr. Chandra serves as a vice-chair of the ACM/SIGDA Technical Committee on FPGA & Configurable Computing and is the co-organizer of the SIGDA Design Automation Summer School (co-located with DAC). He has served or is serving as a Technical Program Committee member for CICC, ICCD, IOLTS, SELSE, DRV workshop, DSN Workshop, VLSI Design conference and also serves as a reviewer for IEEE Trans. on VLSI, IEEE Computer and ACM TODAES. His research interests are in high performance & low-power custom circuit design, memory architecture, DFM and reliability aware design.

Trading Off Dependability and Cost for Nanoscale High Performance Microprocessors: The Clock Distribution Problem

Cecilia Metra
Università di Bologna, Italy
cecilia.metra@unibo.it

Abstract. The continuous scaling of microelectronics technology allows for keeping on increasing IC performance and complexity, but simultaneously poses serious challenges to design, test and dependability. Manufacturing defects are becoming more likely, and parameter variations occurring during fabrication even more severe. Together with the increased ICs' complexity and operating frequency, this is making ever more challenging to guarantee that clock signals are distributed throughout the die with correct skew, duty-cycle, limited jitter and sharp edges. On the other hand, providing correct clock distribution is mandatory for synchronous ICs, to guarantee their dependable operation. The talk will discuss data on clock fault likelihood for high performance microprocessors, and their expected increase for next generation microprocessors. Their testing difficulties, and resulting impact on system dependability will then be analyzed. Possible approaches to allow their concurrent detection and correction in the field to improve system dependability will be described. The issues discussed will encompass industry wide techniques, as well as alternate, currently under development approaches.

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Cecilia Metra is an Associate Professor in Electronics at the University of Bologna. She is also affiliated with the Advanced Research Center on Electronic Systems for Information and Communication Technologies E. De Castro (ARCES) at the Univ. of Bologna. Her research interests encompass Design and Test of Integrated Digital Systems, Reliable and Error Resilient Systems, Fault Tolerance, On-Line Testing, Fault Modelling, Diagnosis and Debug, Emergent Technologies. She has been/is responsible of Research Projects in collaboration with several Companies, including Intel Corporation, STMicroelectronics, Philips Research Labs, Alstom Transport and Becar-Gruppo Beghelli. She is Associate Editor in Chief of the IEEE Transactions on Computers, and Member of the Editorial Board of the Journal of Electronic Testing: Theory and Applications and the Int. Journal of Highly Reliable Electronic System Design. She is the Vice General Chair of IEEE VTS 2010, and recently, was Program Chair of VTS 2009, Program Co-Chair of VTS 2008, the IEEE Int'l Workshop on Design & Test of Nano Devices, Circuits and Systems 2008. She is a Golden Core member of the IEEE Computer Society.