Trading Off Dependability and Cost for Nanoscale High Performance Microprocessors: The Clock Distribution Problem

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Abstract

The continuous scaling of microelectronics technology allows for keeping on increasing IC performance and complexity, but simultaneously poses serious challenges to design, test and dependability. For high performance microprocessors, guaranteeing that clock signals are distributed throughout the die with correct skew, duty-cycle, limited jitter and sharp edges is becoming ever more challenging, and is expected to get even worse for next generation microprocessors. On the other hand, the availability of correct clock signals throughout the die is mandatory for their dependable operation. This problem will be described and possible approaches for dependable clock signal distribution will be discussed.

Extended Summary

The continuous scaling of microelectronics technology allows for keeping on increasing IC performance and complexity, but simultaneously poses serious challenges to design, test and dependability. Manufacturing defects are becoming more likely, and parameter variations occurring during fabrication even more severe. Together with the increased ICs' complexity and operating frequency, this is making ever more challenging to guarantee that clock signals are distributed throughout the die with correct skew, duty-cycle, limited jitter and sharp edges, although providing correct clock distribution is mandatory for synchronous ICs' dependable operation.

Particularly, this is the case for high performance microprocessors and their clock distribution network (Fig. 1), whose signals are increasingly likely to get affected by faults, either directly involving clock nets [1], or their buffers [2].

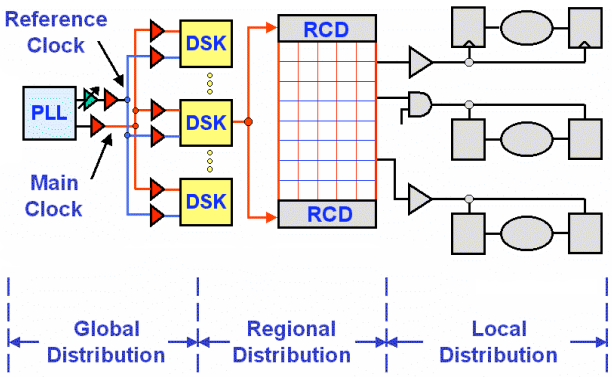

Fig. 1. Example of clock distribution network [3].

As an example, starting from the analysis of real process data and considering, as a reference, the Intel® Itanium® microprocessor [3], by means of Inductive Fault Analysis [4], it has been shown that the probability of resistive bridging faults directly involving clock nets is two orders of magnitude higher than that of other most likely microprocessor bridging faults [1]. Moreover, by means of electrical simulations, it has been verified that only a small percentage of these faults result in a catastrophic failure of the microprocessor, while the majority result in a local delay failure which, although not likely to be revealed during manufacturing test [5], could compromise the microprocessor dependability in the field [1]. Additionally, these undetected clock faults may also invalidate the testing procedure itself [6].

Similar problems may occur due to faults affecting clock buffers. Particularly, considering the Intel® Pentium® 4 microprocessor as an example, it has been shown that this may be the case for permanent and transient faults affecting the global clock signal adjustable delay clock buffers [2]. At the end of fabrication, these buffers are intended to correct systematic clock skews, for instance due to within-die variations of device channel length, threshold, width, etc, while in the field they are intended to compensate for skews due to operation environmental variations, such as Vcc, temperature, etc.

The adoption of such on-chip clock calibration features has been proven successful commercially. However, with the increasing likelihood of faults (due to technology scaling in the nanometer range), and with the wider need of deskew schemes in all segments of clock distribution (due to the increasing likelihood of skew occurrence, for instance due to the increase of process variations), the likelihood of faults, both permanent (due to defects and process variations) and transient (e.g., due to Alpha particles and neutrons), will increasingly affect the clock deskew schemes [2].

Permanent faults affecting clock compensation schemes may cause the generation of output clocks with incorrect duty-cycle, an effect that may not be detectable through manufacturing testing [5], despite the incorrect behavior of the microprocessor due to such faults. Considering the case of the Pentium® 4 deskew calibration features as an example [7], it has been shown that the severity of the derived duty cycle error is so much (Fig. 2), that it is not even easily compensated by modifying the deskew buffers [2]. Similarly, transient faults possibly affecting

the deskew calibration circuits can also result in the generation of output clocks with temporarily incorrect duty cycle, possibly compromising the microprocessor operation in the field and dependability [2].

This kind of problems should not be ignored and specific strategies should be developed to guarantee the microprocessor dependable operation in the field. This is especially true for process shrink of successive generations of microprocessors, that will: 1) present a higher probability to be affected by permanent faults during fabrication and by transient faults in the field; 2) be increasingly dependent upon the use of calibration schemes, in order to cope with the higher performance levels and increase in statistical variations of electrical parameters.

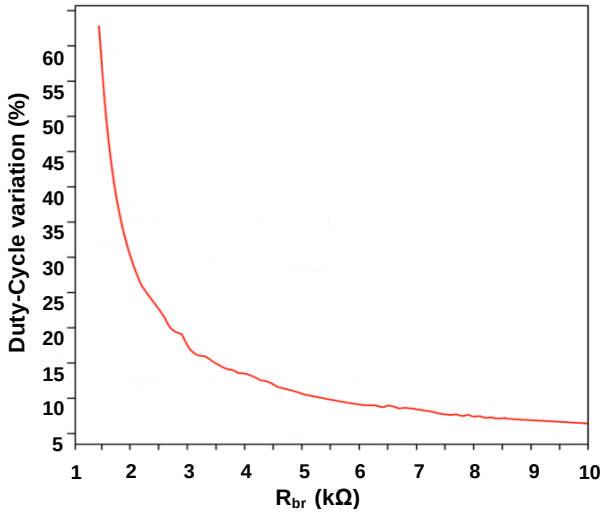

Figure 2. Example of duty-cycle variations due to a resistive bridging fault affecting global clock deskew buffers [2].

Several compensation/correction schemes for clock signals have been proposed in the literature in the past years. They are generally conceived to compensate clock skew, but not duty-cycle variations, which instead have been proven to be likely for today's high performance microprocessors [1, 2] and are expected to become even more likely for next generation ones. Moreover, they generally require some level of area overhead and power consumption, thus being not suitable for massive deployment for the numerous local clocks.

Most recently, some correction/compensation schemes have been proposed to deal also with clock duty-cycle variations and local clocks. As an example, this is the case of the compensation scheme for local clocks of high performance microprocessors and high end ASIC in [8]. Similar to the widely adopted approach of shorting the local clock buffers' outputs, such a scheme does not require any reference clock. It performs compensation continuously, during the chip operation, thus allowing compensation for dynamic faults occurring in the field and achieving dependability increase. Compared to the strategy of shorting the local clock buffers' outputs and to the correction scheme previously proposed in [9], the approach in [8] features lower compensation error (varying from the 42% to the 65%, or from the 69% to the 91%, depending on the considered solution), significantly lower power consumption (up to 91% and 83%, depending on the considered solution and duty-cycle variation) and a lower or comparable area overhead. Therefore it is suitable to local (as well as global) clock compensation of next generation high performance microprocessors, thus allowing their dependability increase.

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