Trading Off Dependability and Cost for Nanoscale High Performance Microprocessors: The Clock Distribution Problem

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Scaling of Microelectronic Technology

Scaling of microelectronic technology:

- ↑ IC complexity and ↑ IC performance.

Courtesy of Intel Corporation


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Scaling and Clock Due Dependability Risks

- But scaling comes together with:
  - \( \uparrow \) IC complexity \( \rightarrow \) \( \uparrow \) # of switching elements \( \rightarrow \) \( \uparrow \) power supply noise
  - \( \uparrow \) operation frequency \( \rightarrow \) time margins \( \downarrow \)
  - \( \uparrow \) likelihood of fabrication defects
  - \( \uparrow \) entity of on-die process variations

\( \uparrow \) difficulties in ensuring limited skew, jitter and correct duty cycle for all clock signals of a synchronous system

\( \downarrow \) System Dependability
Clock Distribution

- Complex network, spreading out throughout the whole chip (horizontally and vertically).

Clock Compensation

- ODCS (On Die Clock Shrink):
  - intended to compensate duty cycle variations (mainly due to parameter variations) at the PLL output

- DSK (DeSKew buffers):
  - intended to compensate skew (mainly due to parameter variations) at the global clock level
Intel™ Pentium®4 example:

- **PD**: Phase Detectors
- **DB**: programmable Delay Buffers, whose programming bits can be fixed permanently

DSK Example: Pentium®4 (cnt’d)

Programmable Delay Buffer:

3-bit Control Register

3 to 8 decoder

s<7:0>

d0
d1
d2

TapClock

iScanDataIn

Early Clock

s0
s1
s2
s7

domain_clk_disable#

Output Clk

DSK Example: Itanium® - 1st gen

- DSK architecture:
  - Local Controller
  - Delay Circuit
  - Deskew Buffer
  - Ref. Clock
  - Global Clock
  - TAP I/F
  - Regional Clock Grid
  - RCD

- DSK local controller:
  - 16-to-1 Counter
  - Phase Detector
  - Digital Low-Pass Filter
  - Enable
  - Reference Clock
  - Feedback Clock
  - Lead / Lag
  - To Deskew Buffer Register

Variable Delay Circuit:

Input

20-bit Delay Control Register

Enable

Output

DSK Example: Itanium® - 2nd gen

Variable Delay Circuit:

Variable Delay Circuit (for fine delay adjustment):


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Attempts at Clock Correctness

- DeSKew strategies intended to compensate skew (mainly due to parameter variations) at the global clock level

But are parameter variations the only attempt at clock signal correctness?

Or can clock signals get also (directly/indirectly) involved by faults occurring during fabrication, or in the field?

And how this will change with technology scaling?
Can Clock Signals Get Directly Involved by Faults?

- Inductive Fault Analysis (IFA) performed on the Intel® Itanium® microprocessor proved [1] that:

  - after the most likely Vcc-Vss bridging fault (BF),

  BF$s directly involving a CK signal and Vcc (or Vss) are the most likely!

Can Clock Signals Get Directly Involved by Faults? (cnt’d)

Clock is the #1 net in terms of probability

These are scan clocks and scan control signals

TOP WCA signal nets

Can Clock Signals Get Directly Involved by Faults? (cnt’d)

- Electrical level simulations of the *Itanium®* clock distribution network, with BFs emulated by resistances in the \([0-10\, k\Omega]\) range, proved [1] that:
  
  - the most likely effects of clock faults are the occurrence of *duty cycle variations* which can occur also at the *local clock level*


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Can Clock Signals Get Directly Involved by Faults? (cnt’d)

Voltages at a leaf of the clock tree with a 50 Ω BF to Vcc
duty cycle variation at the local clock level!


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Can Clock Signals Get Directly Involved by Faults? (cnt’d)

- Clock signals can also get directly involved by faults [1]
- Such clock faults:
  - are orders of magnitude more likely than other faults [1]
  - may produce effects observable only at a local level [1]
  - are likely to result in duty-cycle variations [1]
  - will be increasingly more likely with technology scaling

- If not screened out or compensated, such faults might compromise the correct operation of the microprocessor in the field

**Dependability Risks!**


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Can Clock Signals Get Indirectly Involved by Faults?

- Electrical level simulations of the Pentium 4® microprocessor adjustable delay clock buffers [2] with injected:
  - transistor stuck-ons (SONs),
  - transistor stuck-opens (SOPs),
  - node stuck-ats (SAs),
  - BF s (R in the [0-6kΩ] range)

proved that:
  - such faults are very likely to result in output clocks with incorrect duty-cycle [2].

Effects of Faults Affecting Clock Buffers

SA Effect Probability

- No Effect: 29%
- Detectable Effect: 71%

SON Effect Probability

- No Effect: 29%
- Duty Cycle Variation: 42%
- Detectable Effect: 29%

SOP Effect Probability

- No Effect: 29%
- Duty Cycle Variation: 35%
- Detectable Effect: 36%


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Effects of Faults Affecting Clock Buffers (cnt’d)

% BF affecting the CKout duty-cycle


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Produced Duty-Cycle Variations Can be Significant

- Example of a BF between Vcc and the buffer output.

- High duty-cycle variations for values of connecting resistance ≤ 4kΩ!


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Clock signals can also get indirectly involved by faults (which directly affect clock buffers) [2]

Such clock faults:
- are likely to result in duty-cycle variations, which can be very significant [2]
- will be increasingly more likely with technology scaling

If not screened out or compensated, such faults might compromise the correct operation of the microprocessor in the field

Clock Faults’ Due Dependability Risks: Solutions?

Can clock faults be screened out through manufacturing (structural or functional) testing?

Or can their effect be compensated?
Can Clock Faults Be Tested Out?

- Generally, no specific testing procedure is adopted for clock faults.

- However, can clock faults be indirectly detected during manufacturing testing (e.g., structural or functional testing)?

  - It has been verified that clock fault indirect detection through

    - structural testing is not likely [1]
    - functional testing is not likely [3]


Can Clock Faults Be Tested Out? (cnt’d)

- Detecting clock faults through **structural testing** is not likely [1]:

  - depending on the structural test technique, anywhere **between 59% and up to 88% of possible clock faulty conditions may be not detected.**

Inability of Structural Testing to Guarantee Clock Faults’ Detection


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Can Clock Faults Be Tested Out? (cnt’d)

- Detecting clock faults through functional testing is not likely [3]:

* Results for all long/short paths of 10 considered ISCAS’85 benchmarks

$$\text{AvP}_{\text{det}} = \sum \frac{P_{\text{det}}(i)}{n} \quad i = 1, 2, \ldots, n = 10$$

<table>
<thead>
<tr>
<th>Mod($\Delta_{DC}$ %)</th>
<th>10%</th>
<th>20%</th>
<th>30%</th>
<th>40%</th>
<th>50%</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\text{AvP}_{\text{det-sp}}$</td>
<td>23%</td>
<td>33%</td>
<td>43%</td>
<td>44%</td>
<td>44%</td>
</tr>
<tr>
<td>$\text{AvP}_{\text{det-lp}}$</td>
<td>24%</td>
<td>27%</td>
<td>33%</td>
<td>34%</td>
<td>35%</td>
</tr>
</tbody>
</table>

Inability of Functional Testing to Guarantee Clock Faults’ Detection


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Clock Faults’ Due Dependability Risks: Solutions?

Can clock faults be screened out through manufacturing (structural or functional) testing?

No guarantee

Or can their effect be compensated?
Can CKF Effect Be Compensated?

- Compensation schemes are intended to compensate skew mainly due to parameter variations at the global clock level.

- CKFs’ most likely effect is to produce duty cycle variations, which:
  - can be very significant
  - can occur also at the local level only

- Compensation schemes could be modified to deal with CK faults, but their cost would be very high.
Clock Faults’ Due Dependability Risks: Solutions?

Can clock faults be screened out through manufacturing (structural or functional) testing?

No guarantee

Or can their effect be compensated?

NO (unless high cost)

Need for Testing Approaches and/or Correction Schemes to Increase Dependability at Affordable Costs

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Example of Low Cost Testing Approach for Clock Faults

It has been proposed [4]:

- to make CFs’ most likely effects (i.e., duty-cycle variations) result in clock stuck-at faults (S@)
- catastrophic effects
- easy detection through conventional manufacturing test

Possible Hardware Implementation

- Insertion of Duty-Cycle Error Detect and Latch blocks (DCEDL\(_i\)) among physically adjacent (local and global) CK buffers.

- Each DCEDL\(_i\):
  - checks the outputs of 2 adjacent clock buffers;
  - gives the enable signal for one of such clock buffers.

- All DCEDL\(_i\) disabled (E\(_i\)=0) during µP normal operation.


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Possible Hardware Implementation (cnt’d)

- Duty-Cycle Error Detect and Latch blocks (DCEDL_i) between adjacent clock buffers.

- DCEDL_i enabled (E_i=1) during μP testing:
  - if CK_{iB}≠CK_{(i+1)B} → en_{(i+1)}=0 → buffer B_{i+1} disabled → CK_{(i+1)B} S@0 → easy detection;
  - if CK_{iB}=CK_{(i+1)B} en_{(i+1)}=1 → buffer B_{i+1} enabled → no effect.


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Approach synergetic with local CK distribution → no routing problems.

- TE connected to E_i of each DCEDL_i →
- When TE=1 → en_i
- generated in a ripple fashion → S@0 on all CKs physically located among the faulty one and the last one.

CF easy detection through conventional manufacturing test.

Application to Global Buffers: Pentium®4 Example

- Approach synergetic with global CK distribution → no routing problems.

- Scheme activated after calibration (ECP=1) → detection of CFs, after parameter variation compensation.

- Signal TE* =AND(TE, ECP) connected to the enable terminals (E_i) of the DCEDLs.


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Application to Global Buffers:
Pentium®4 Example (cnt’d)

- Approach synergetic with global CK distribution → no routing problems.

- When $TE^* = 1 \rightarrow en_{iR}$ generated in a ripple fashion → $S@0$ on all CKs physically located among the faulty one and the last one.

CK fault easy detection through conventional manufacturing test

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Example of Low Cost Correction Scheme for Clock Faults

Proposal of a scheme [5] capable of:

- detecting mismatches between couples of physically adjacent local CKs and giving:
  
  i. a high impedance state output, in case of mismatch;

  ii. the logic value present on one of the two input clock signals, in case of matching.

Correction Scheme: Component Blocks

Scheme composed of 3 blocks:

1. Detection Block
   - It receives \( n \) input local clocks \( (CK_{in,i}, i=1,\ldots, n) \) to be compensated in case of phase mismatch (i.e., duty cycle variation - \( \Delta DC \)).
   - It consists of \((n-1)\) sub-blocks, each:
     - detecting phase mismatches between two physical adjacent input clocks \( (CK_{in,i} - CK_{in,(i+1)}) \)
     - giving a high impedance state (Z) if the input CKs present \( \Delta DC \).

Correction Scheme: Component Blocks (cnt’d)

- Scheme composed of 3 blocks:

1. Detection Block
2. Compensation Block

- It receives the \((n-1)\) outputs of the Detection block \((CK_{i,(i+1)}, i=1,\ldots, n-1)\) and provides \(n\) compensated clock signals \((CK^*_i, i=1,\ldots, n)\).


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Compensation Block: Possible Implementation

- We can simply **short together the $(n-1)$ outputs of the Detection Block.**

- The **high-Z state outputs** of the Detection Block are forced to assume the correct logic value imposed by the non high-Z state outputs.

- **No electrical conflict arises → minimal power consumption and compensation time !**

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Scheme composed of 3 blocks:

- It receives the outputs of the Compensation block and provides properly buffered, compensated output clocks ($CK_{out,i}$, $i=1,\ldots, n$).

Cost Comparison

- Scheme in [5] compared with:
  - the clock compensation scheme in [6] (Solution 1);
  - the strategy that simply shorts together the outputs of the local clock buffers (Solution 2).

- Costs evaluated in terms of:
  - compensation error;
  - power consumption;
  - area overhead.


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Case 1: for all schemes it has been considered that 1 out of 16 input CKs presents a \( \Delta DC \) between 0\% and 100\% of its nominal value (50\% of \( T_{CK} \)).

The scheme in [5] & solution 2 present a considerable low compensation error (0.2\% and 0.4\%, respectively) that does not change with the magnitude of \( \Delta DC \).

**Cost Comparison: Compensation Error (cntd)**

- **Case 2:** compensation error as a function of the # of incorrect input CKs (= among them and with a ΔDC of 40% of its nominal value).

  - The scheme in [5] presents the lowest compensation error, with a reduction >69% compared to solution 1 and >40% compared to solution 2.

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Cost Comparison: Power Consumption

- Power consumed by the 3 considered solutions as a function of ΔDC.

Due to the avoidance of electrical conflicts during compensation, the power consumed by the scheme in [5] is approx. constant (∼40μW) with ΔDC.


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Cost Comparison: Area Overhead

- Area (expressed in squares) of the 3 considered solutions as a function of the # of input clocks to be compensated.

- The area of the scheme in [5] slightly increases with respect to that of the solution 2. However, such an increase can be considered negligible when the total chip area is accounted.

Conclusions

- Faults affecting clock signals are likely and their likelihood will increase with technology scaling.
- They may be not screened out during manufacturing testing.
- They cannot be compensated at low costs by current schemes.
- They may compromise the microprocessor correct operation in the field, with consequent decrease in dependability.

New Testing Approaches and/or Correction Schemes are (should be) searched for increased Dependability at Affordable Costs.
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