Invited Talk

Sustaining Error Resilience: Case Study of the IBM POWER6™ Microprocessor

Pia Sanda

IBM Systems & Technology Group
Poughkeepsie, NY, USA
sanda@us.ibm.com

Abstract

As circuit density continues to increase, hard and soft errors also increase. As such, it is becoming ever more important for systems to be resilient to circuit level errors. This is the case for today's systems in CMOS technology, and this learning will prepare us for devising resilient architectures for post-silicon technology. This talk will describe the error resilient design of the IBM POWER6™ microprocessor. POWER6 extends the reliability, availability, and serviceability (RAS) capabilities of the POWER5™ microprocessor, dramatically increasing the ability to recover from hard and soft errors without increasing system down time. The POWER6 microprocessor adds new mainframe-like features for enhanced RAS including instruction retry and processor failover. POWER6, optimized for performance and power, implements these RAS enhancements without compromising ultra-high frequency operation. Error resilience was validated using accelerated testing with high energy proton and neutron beam sources. Statistical fault injection (SFI) provides a means to verify the hardware-emulated gate-level model for soft error resilience. SFI was validated against particle beam experiments for the POWER6 microprocessor core built in IBM 65nm SOI technology.