Second Workshop on Dependable and Secure Nanocomputing

Preface

Jean Arlat
LAAS-CNRS, Université de Toulouse
7, Avenue du Colonel Roche
31077 Toulouse Cedex 04 – France
jean.arlat@laas.fr

Cristian Constantinescu
AMD
2950 E Harmony Rd.
Fort Collins, CO 80528 – USA
cristian.constantinescu@amd.com

Ravishankar K. Iyer
Coordinated Science Lab. - UIUC
1308 West Main Street
Urbana, IL 61801 – USA
iyer@crhc.uiuc.edu

Michael Nicolaïdis
TIMA
46, Avenue Felix Viallet
38031 Grenoble – France
michael.nicolaidis@imag.fr

The Workshop is aimed at focusing on the emerging dependability and security issues that are attached to the evolution of hardware designs and semiconductor technologies. Two main tracks are being considered in order to incorporate an increasingly large number of devices and processing elements into a chip:

- pushing further the long standing Moore's Law-based trend that aims at reducing the size of silicon microelectronics (the *More Moore* track*)*;
- featuring atomic assemblies of nanoscale technologies (nanowires, carbon nanotubes, organic molecules, etc.,) as weel as highly advanced (e.g., quantum or optical) computing devices (the *Beyond Moore* track).

This Workshop was established last year in the frame of DSN-2007 (see www.laas.fr/WDSN07). It was quite successful: it gathered about 50 participants and resulted in many lively discussions among the contributors and the attendees. Moreover, not all issues at stake could be addressed with sufficient level of details then. Accordingly, we are pleased to welcome you to the second edition.

The overall aim is twofold: i) better characterizing the hardware-related impairments and threats; ii) identifying possible design techniques and operation paradigms for sustaining dependable and secure computing. The Workshop slightly extends the three main objectives that we had put forward last year:

1) *Review* the state-of-knowledge about main threats in nanocomputing technologies: manufacturing defects, operational faults, and malicious attacks.
2) *Identify* existing solutions and *propose* new solutions attached to various design options for mitigating faults and implementing resilient computing devices and systems.
3) *Forecast* the risks associated to emerging technologies and *foster* new trends for cooperative work, possibly combining various alternatives to help increase the pace of advances and solutions.

The feedback received from the community was, once again, excellent: 14 papers were submitted, involving eleven different countries. Each of these submissions has been reviewed by at least three members the Program Committee. We are thankful to them for their support in the evaluation process and especially for their dedication in providing insightful feedback to the authors.

This evaluation has shown the richness and large scope of the submitted contributions, spanning many issues relevant for nanoscale technologies: fault models, soft error characterization and analysis, fault tolerance techniques, reconfigurable chips, synchronous *vs.* asynchronous designs, intrusion detection mechanisms, testing, etc.

Accordingly, this year the program heavily relies on these submitted contributions. Thirteen of these contributions are included in the program of the Workshop. Paper authorship is distributed as follows: USA (3), Spain (2), France, Japan, Taiwan (1 each), and we have also 5 dual-country papers — Estonia-Germany, France-Canada, France-Poland, Germany-USA, USA-Israel.

Based on the specific feedback received during the evaluation process, presentations will include both regular (20mn) and short (10mn) slots. They are grouped into three main sessions as follows: i) characterization of defects and failure modes in nanoscale technologies, ii) performance and security issues in hardware design, iii) mitigation and resilience techniques for nanocomputing. Moreover, an invited talk by Pia Sanda (IBM Systems & Technology Group, Poughkeepsie, NY, USA) will kick off the Workshop by addressing error resilience issues on the IBM POWER6™ microprocessor.

You will find hereafter the written material that accompanies each of the presentations given at the Workshop. For your convenience, the papers are listed according to the session schedules.

We sincerely hope that you will enjoy the Workshop and actively participate by interacting with the various contributors. We also very much welcome your comments and hints for future plans of this event.

Further information is available from this year Workshop website (www.laas.fr/WDSN08). In particular, the site will be updated after the Workshop to include the slides presented by the contributors.