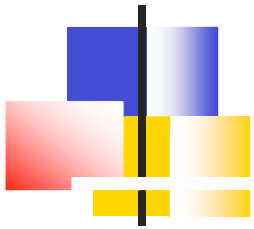

Combined Defect and Fault Tolerance for Reconfigurable Nanofabrics

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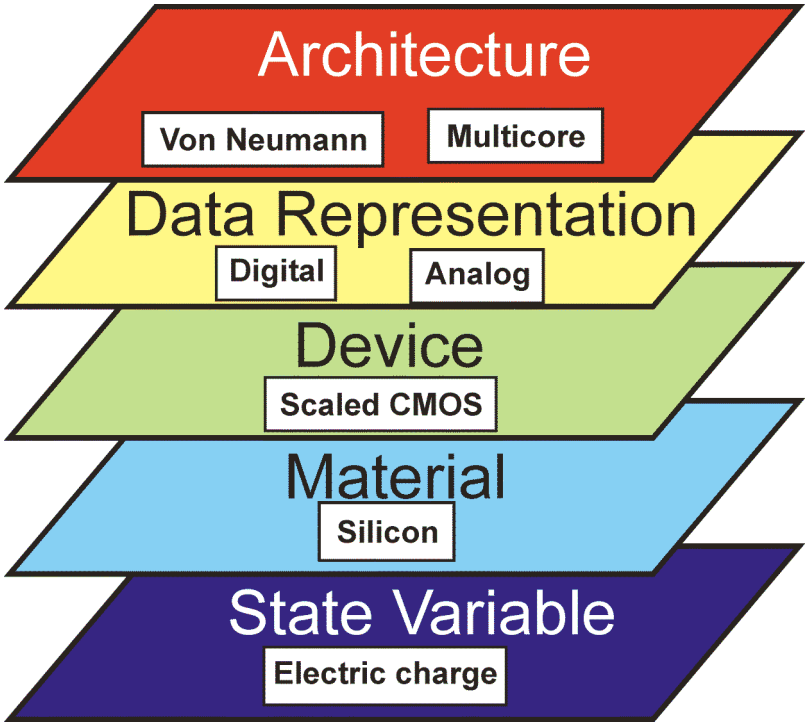
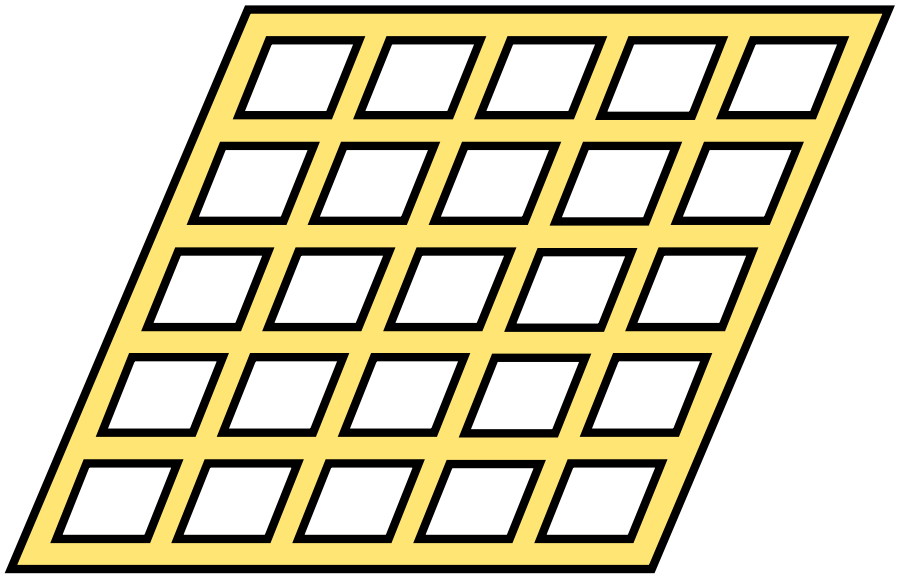
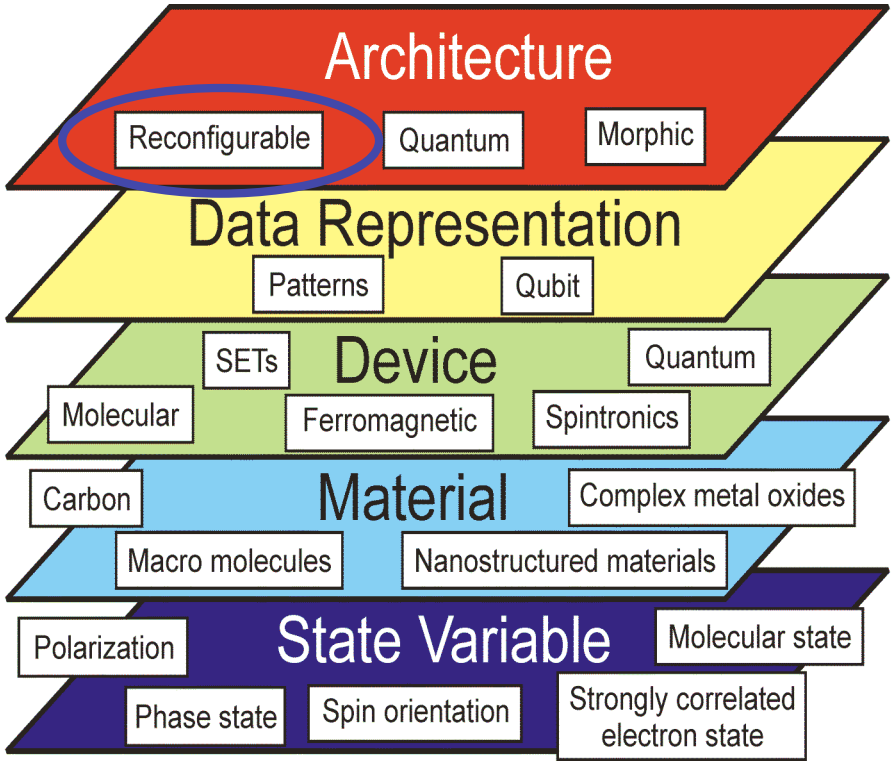
Conventional scaled CMOS

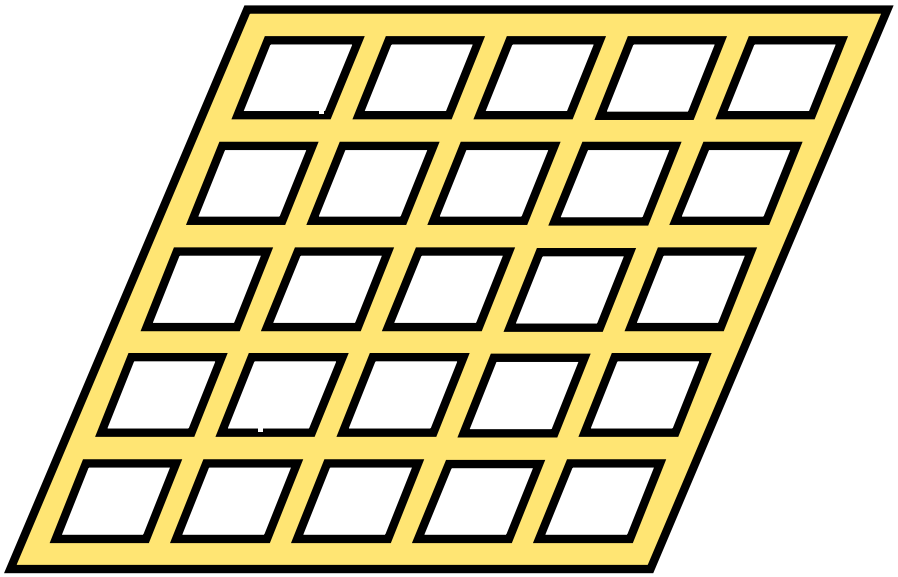




10%-40% defective cores

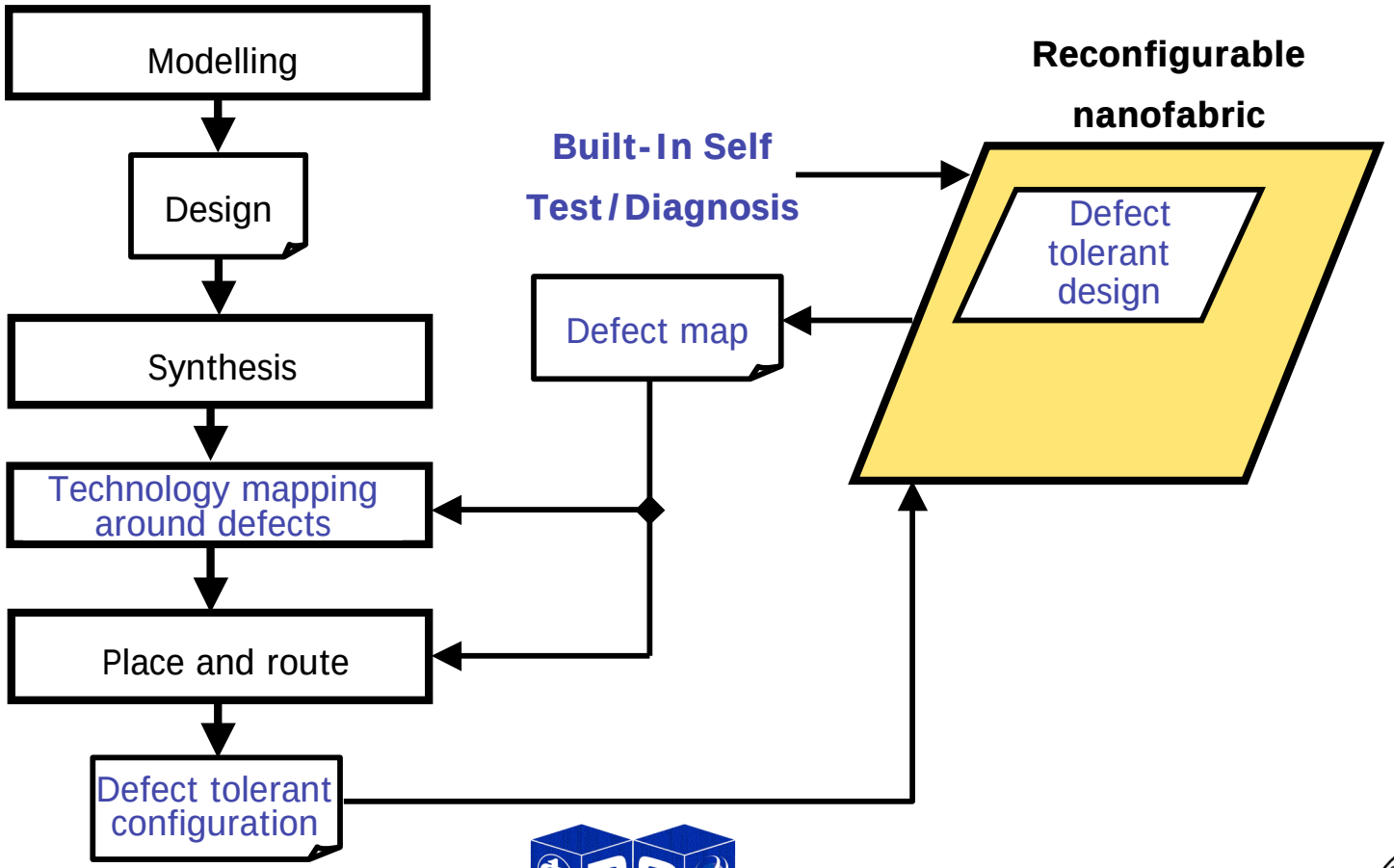
New information process technologies



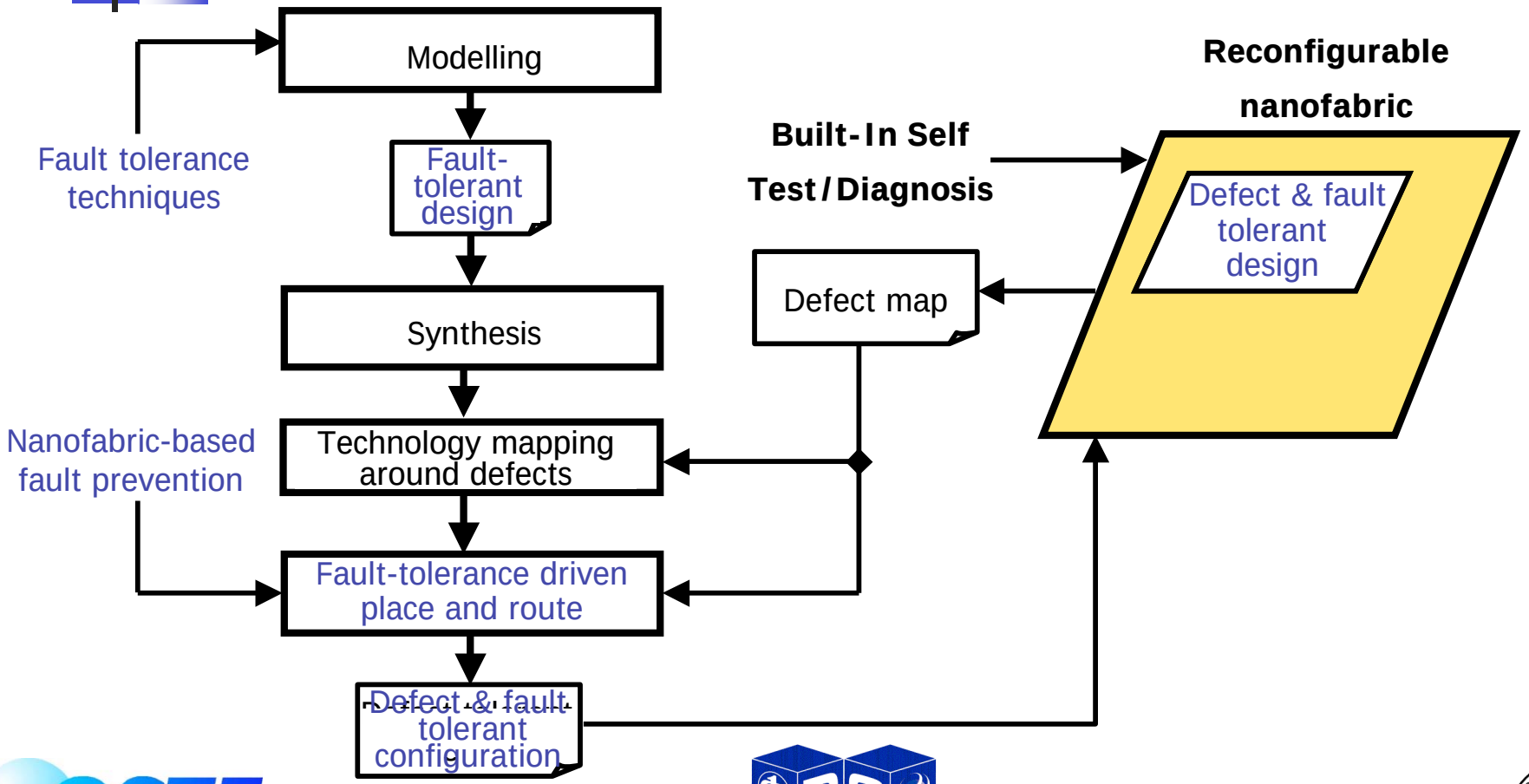


~10% defective *devices*

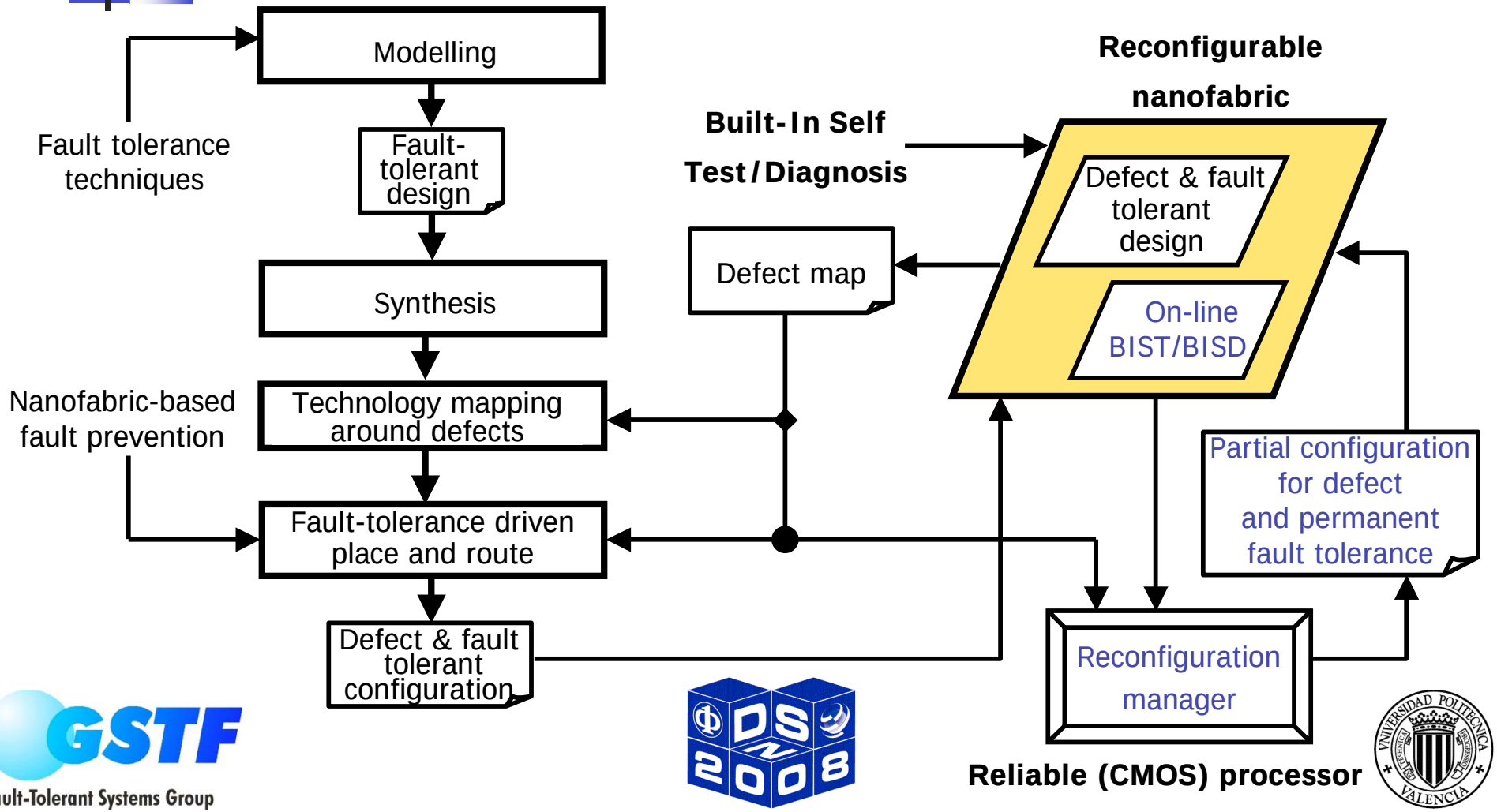
New Design flow for reconfigurable computing



New Design flow for reconfigurable computing



New Design flow for reconfigurable computing



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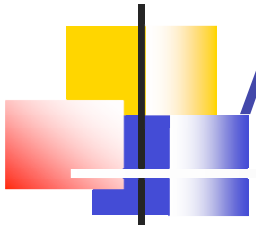
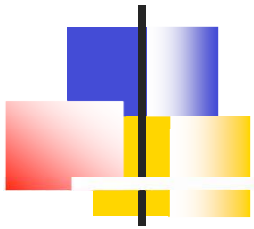
Future research work

- New design flow for reconfigurable nanocomputing
  - BIST/BISD strategies for reconfigurable nanofabrics
  - Automatic deployment of fault tolerance mechanisms
  - Fault-tolerance driven place and route algorithms
  - Reducing the dependency on a reliable (CMOS) external processor



Any question?

Thank you for paying attention!



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