BISM: Built-in Self-Map for Crossbar Nano-Architectures

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Outline

- Introduction
- Bottom-up Self-Assembly
- Crossbar Nano-architectures
- Built-in Self-Map
  - Various Schemes and Comparisons
- Conclusions

Bottom-Up Fabrication

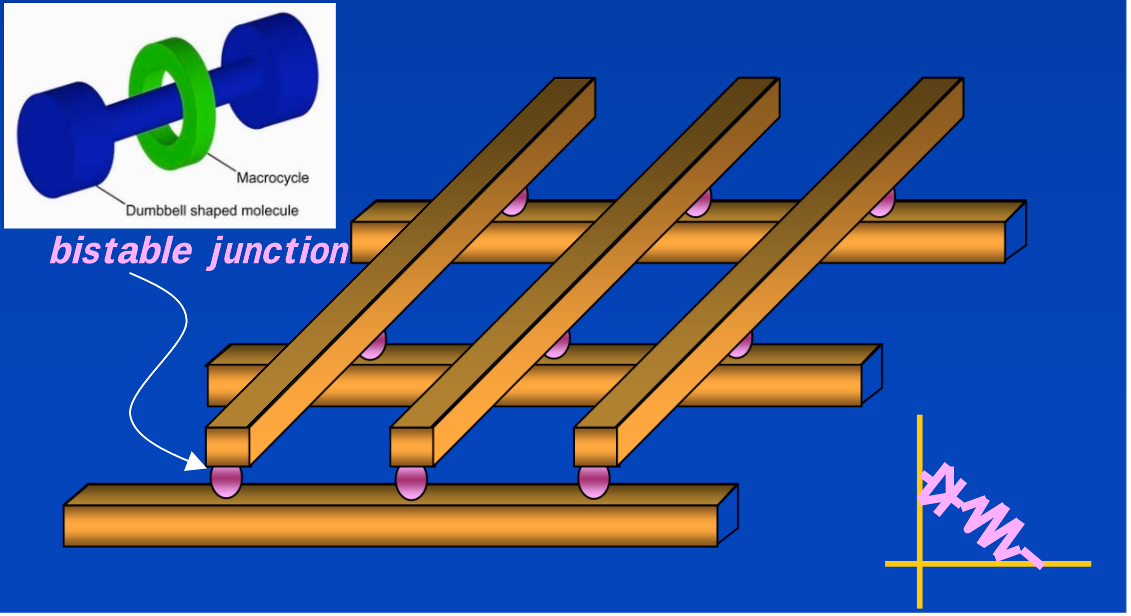
- Use bottom-up assembly as an alternative to top-down
  - Rely on self-assembly for defining device characteristics
  - Easier (less costly) fabrication process
  - Requires fabrication regularity
    - Lends itself more easily to a *reconfigurable* architecture

BUT…

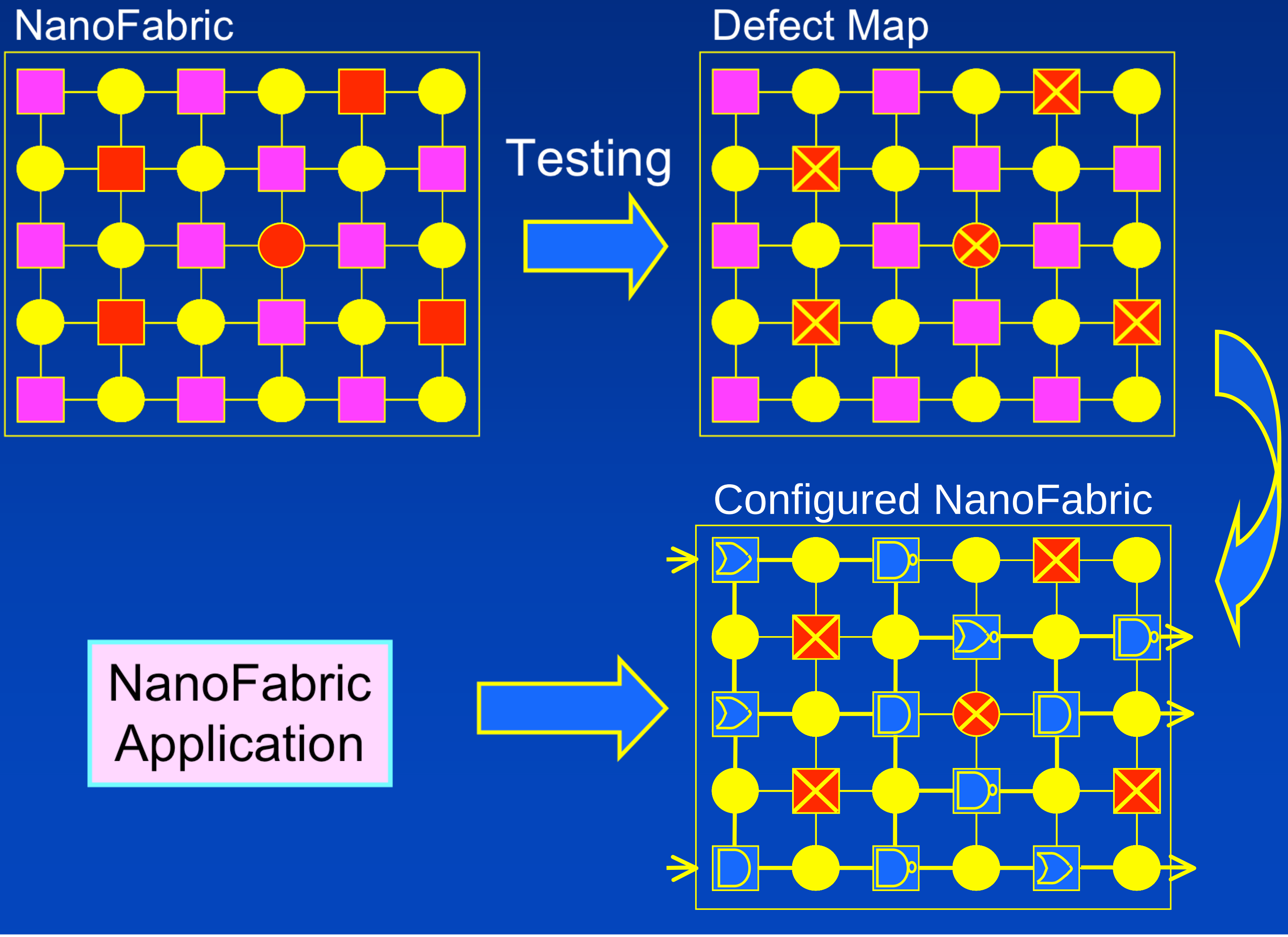
- This creates new challenges:
  - Can no longer arbitrarily determine device/wire placement.
    - Leads to higher defect rates
  - Fabrication may be restricted to simpler (less robust) structures
    - e.g., 2-terminal vs. 3-terminal devices

Molecular Crossbar

- Building Block for crossbar array architectures
  - Fabricated by chemical self-assembly process
- Two layers of orthogonal nanowires/CNTs
  - Programmable switch at each crosspoint
    - Rotaxane molecule
    - Located at each intersection of wires
    - Determine the configuration of the crossbar
- Can be used for
  - Signal routing
  - logic
  - Memory

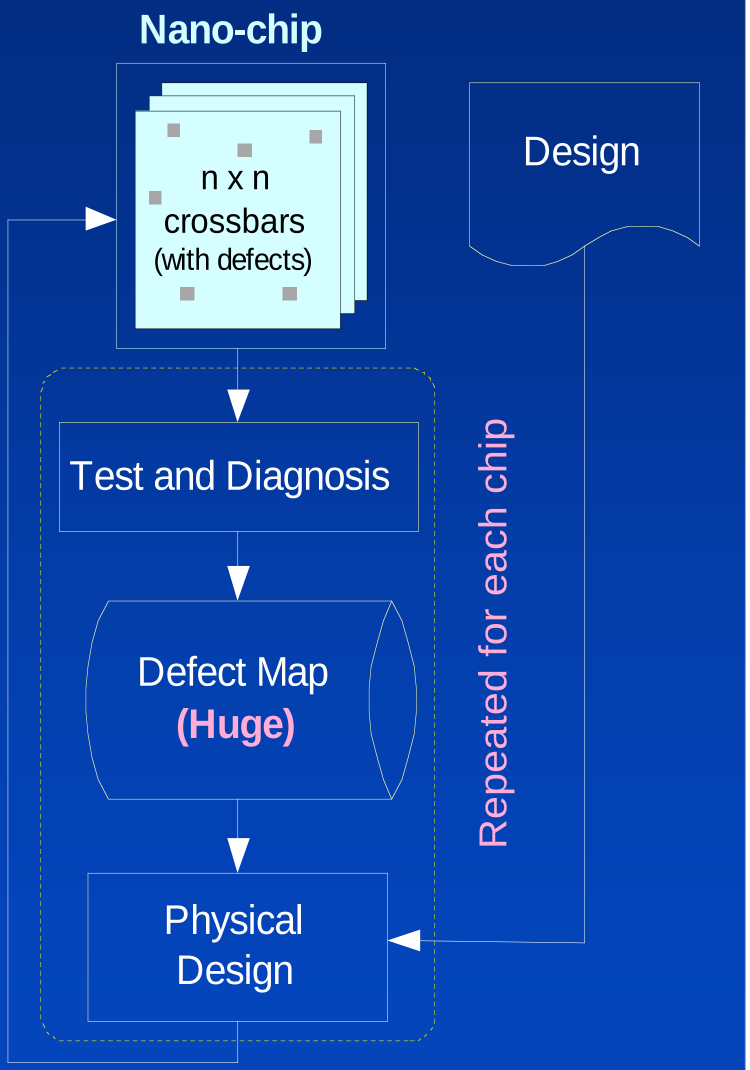


Application-Dependent Defect Tolerance



Application-Dependent Defect Tolerance

- Steps to be done per chip
  - Identify all defect-free resources
    - Using test and diagnosis
    - Generating a defect map
      - Location of defect-free resources
  - Use defect map during design phase
    - Bypass defective devices thru reconfiguration
    - Defect map used by design tools



Application-Dependent Flow

- Problems
  - ☹ Defect map is huge!
  - ☹ All design tools need to be defect-aware
    - Defect-map used during design
  - ☹ Post-fabrication customized design per chip!

    Test time

    + Diagnosis time

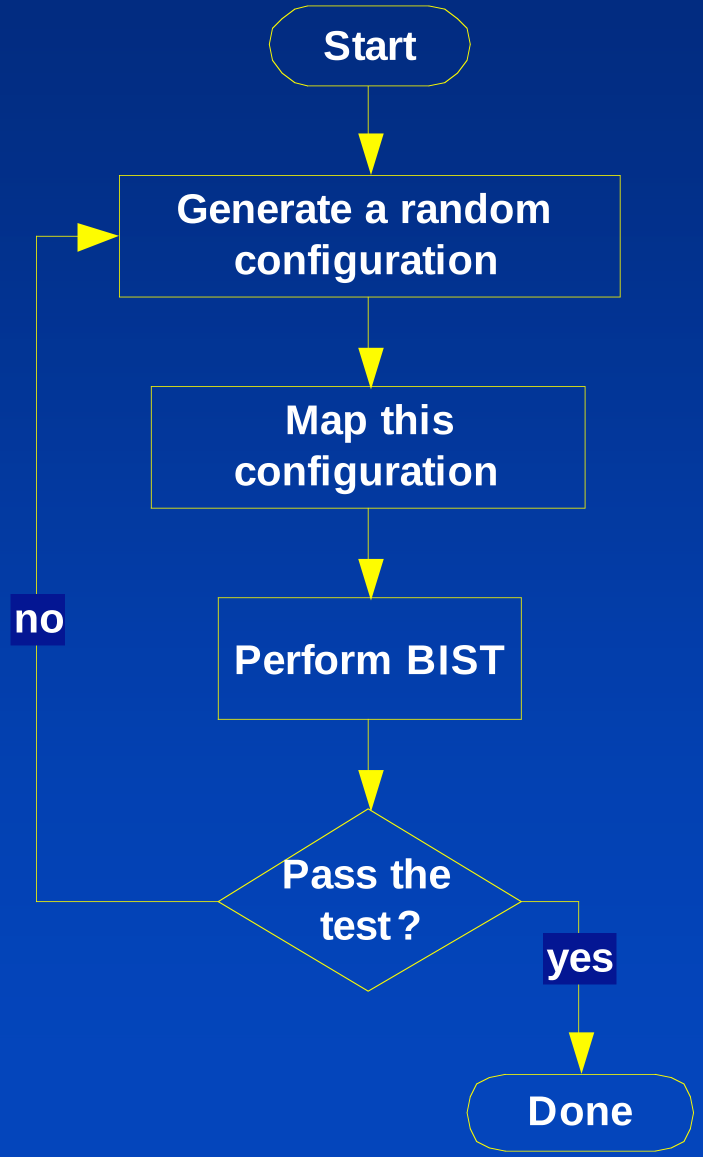
    + **Design mapping time**
    - Serious problem for high volume production

Built-in Self-map (BISM)

- Minimizes per-chip customized mapping efforts
- Allows crossbar array to
  - Configured by the on-chip interface circuitry
    - Bypass defective resources
- Reduces physical design efforts
  - Detailed placement and routing performed on-the-fly
- Used in implementation of
  - Fault tolerance schemes
  - Defect tolerance schemes

Blind BISM

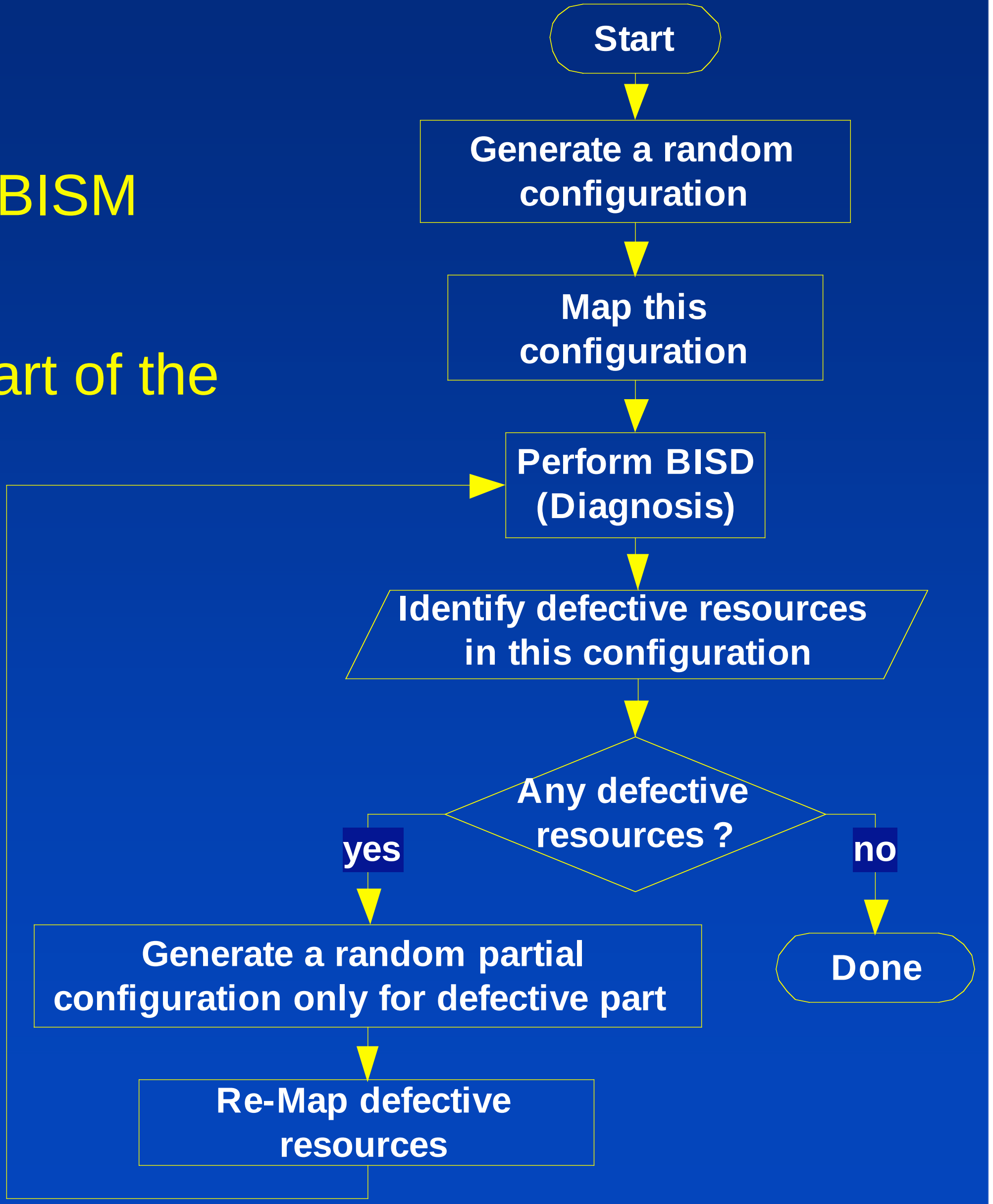
- Randomly re-generate configuration
  - Configuration implements required function by crossbar
- Until configuration passes test
- Fast and simple
  - No diagnosis involved
- Works best for
  - Small defect densities



Greedy BISM

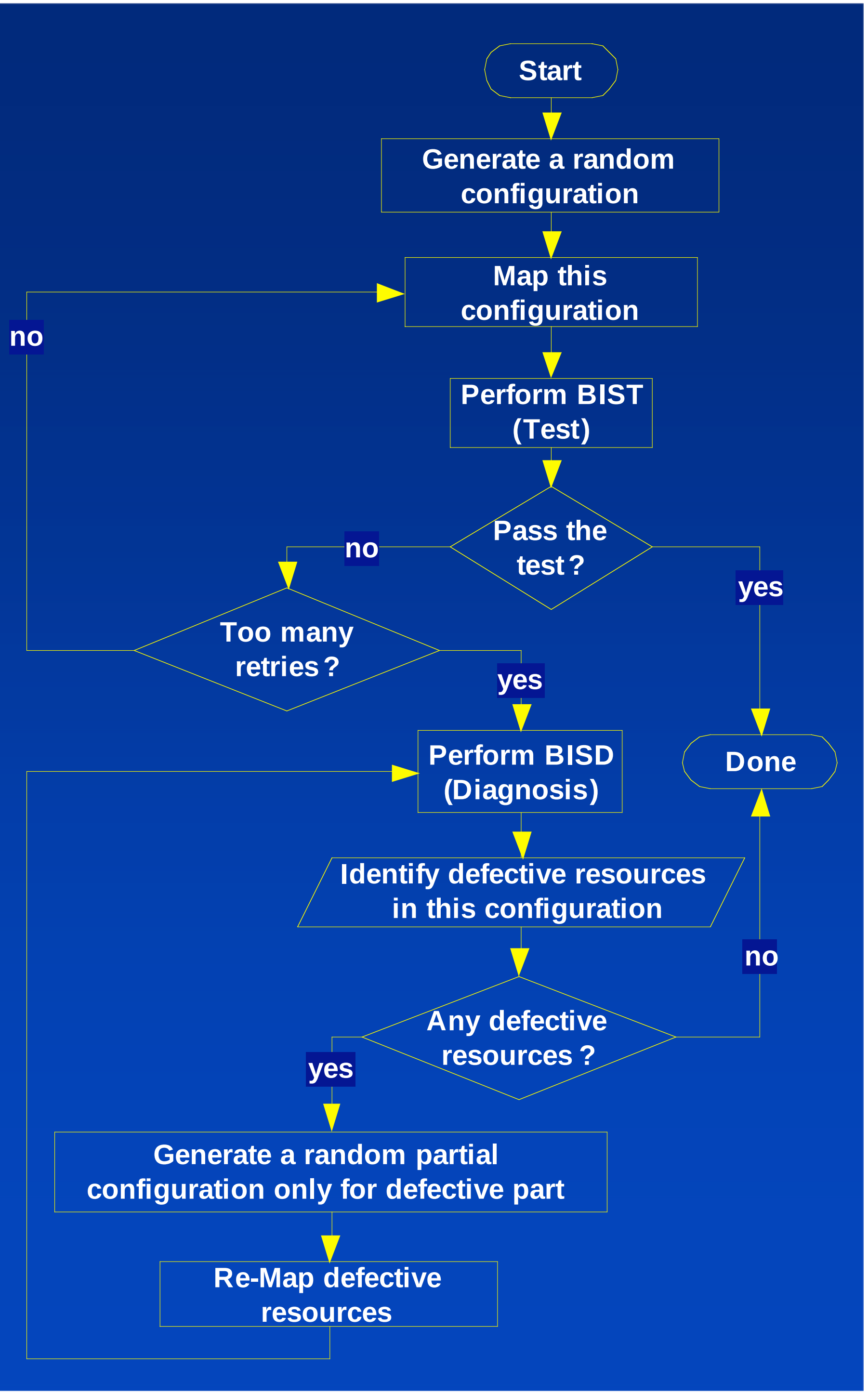
- High defect densities
  - Too many retries in blind BISM
- Greedy BISM
  - Only re-maps defective part of the configuration
    - Using BISD (diagnosis)
  - Partial configuration

- More complex than blind BISM
- Works better for
  - Higher defect densities


Start
Generate a random configuration
Map this configuration
Perform BISD (Diagnosis)
Identify defective resources in this configuration
Any defective resources ?
yes
no
Generate a random partial configuration only for defective part
Re-Map defective resources
Done

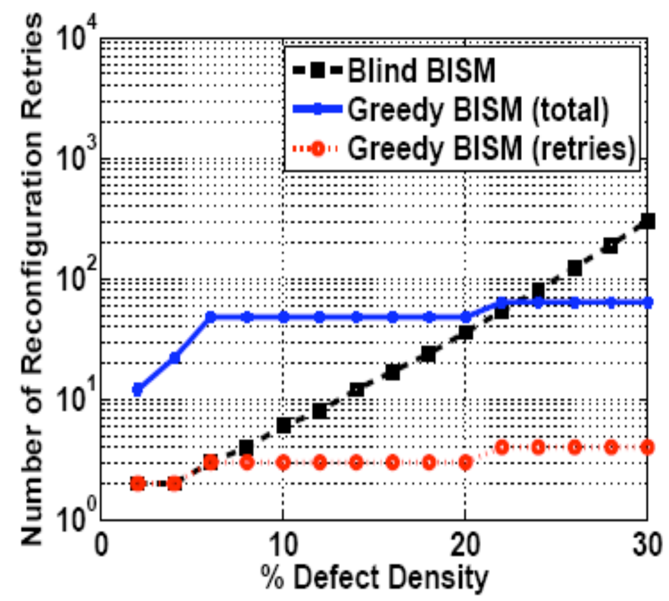
Hybrid BISM

- Combination of
  - Greedy and blind BISMs
- Approach
  - Starts with blind BISM
  - Switches to greedy BISM
    - If too many retries
      - Threshold
- Works best for both
  - Low defect densities
  - High defect densities

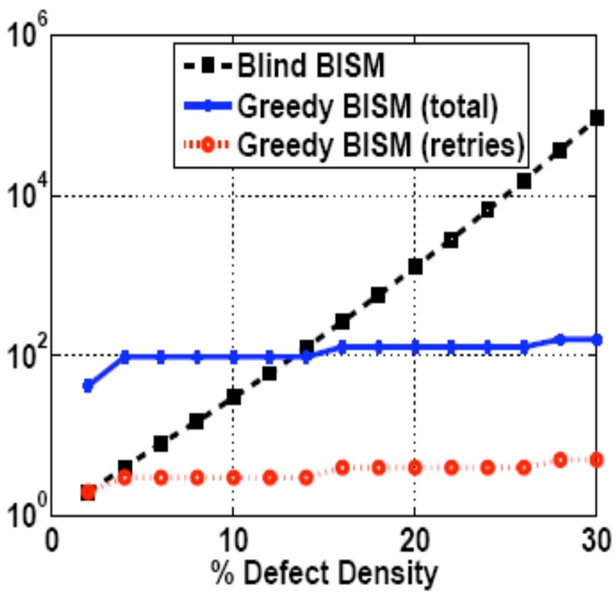

Start
Generate a random configuration
Map this configuration
Perform BIST (Test)
Pass the test ?
no
yes
Too many retries ?
no
yes
Done
Perform BISD (Diagnosis)
Identify defective resources in this configuration
Any defective resources ?
no
yes
Generate a random partial configuration only for defective part
Re-Map defective resources

Comparison of BISM Schemes

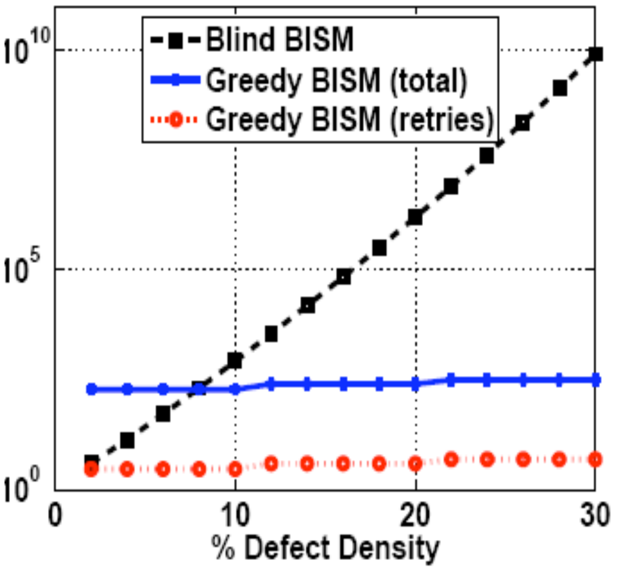
- Each retry in greedy BISM has more steps than blind BISM
  - Diagnosis configurations >> test configurations
- Greedy BISM outperforms blind BISM for higher defect densities
- Hybrid BISM is the minimum of these two schemes



16 × 16 crossbar



32 × 32 crossbar



64 × 64 crossbar

Conclusions

- Defect and fault tolerance inevitable for systems built using self-assembly processes
- Regular, tile-based architectures seem promising
- Built-in self map (BISM): physical mapping of the designs performed on-the-fly using on-chip resources
  - Simpler and faster design and test flows
  - Reduced post-fabrication configuration time.
- BISM enables effective defect/fault tolerance