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Fault Tolerance of the Input/Output Ports in Massively Defective Multicore Processor Chips

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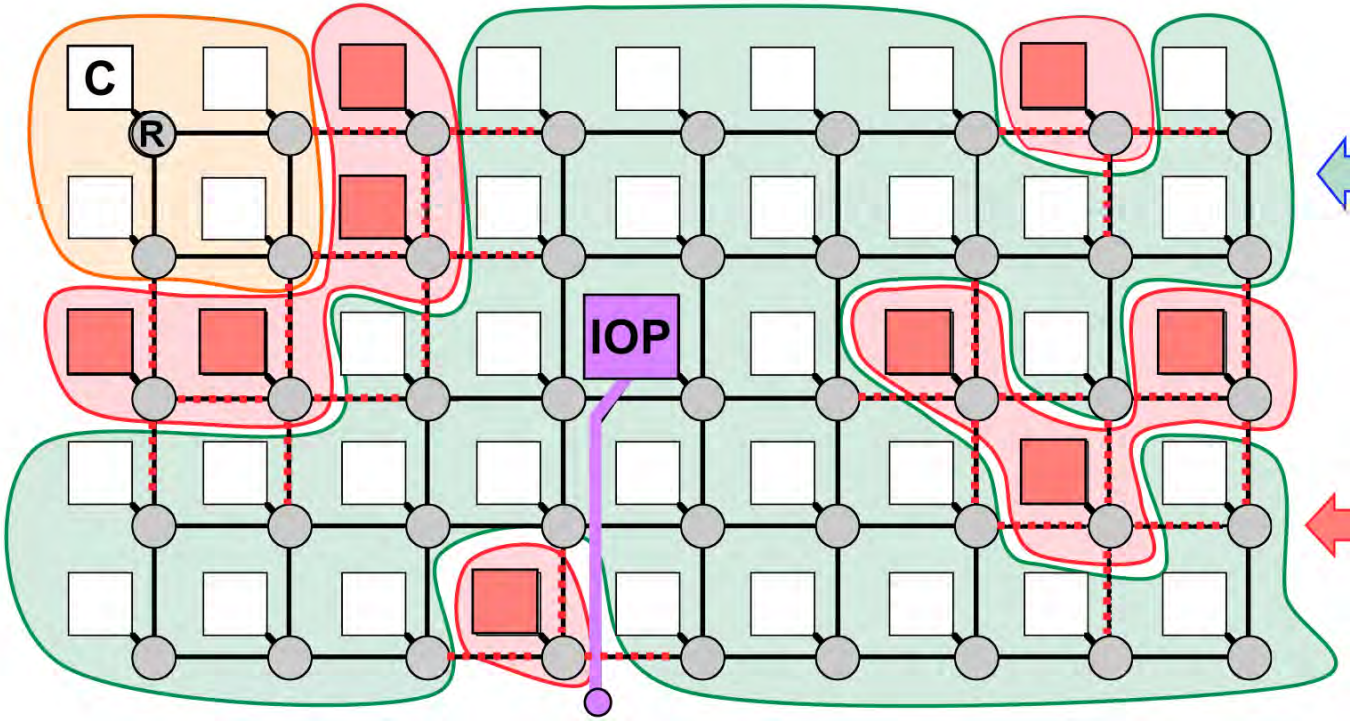
From Multi-Cores Architectures To Multi-Multi-Cores Architectures

- **Multi-Core: ↗ performance while coping with power dissipation issues (very high clock frequency)**
- **Still, ↘ transitor size for including many of such cores —> significant % of defective cores (more than 10% ?)**
- **Current context:**
  - **Chips are sorted according to frequency**
  - **Single core processor = “Downgraded” dual core circuits …**
- **How to go further: On-line reconfiguration to cope with faults?**

Example Target Architecture

(5x9-node Network — Connectivity: 4)

Disconnected Zone



Single Connected Zone

Mutual Diagnosis v Bad Cores Isolated

P. Zając, J. H. Collet, J. Arlat, Y. Crouzet, "Resilience through Self-Configuration in Future Massively Defective Nanochips", Supplemental Volume DSN2007, Edinburgh, Scotland, UK, pp.266-271, 2007

C Core Processor

R Router

IOP I/O Port

Failed Core Processor

Inhibited Inter-router link

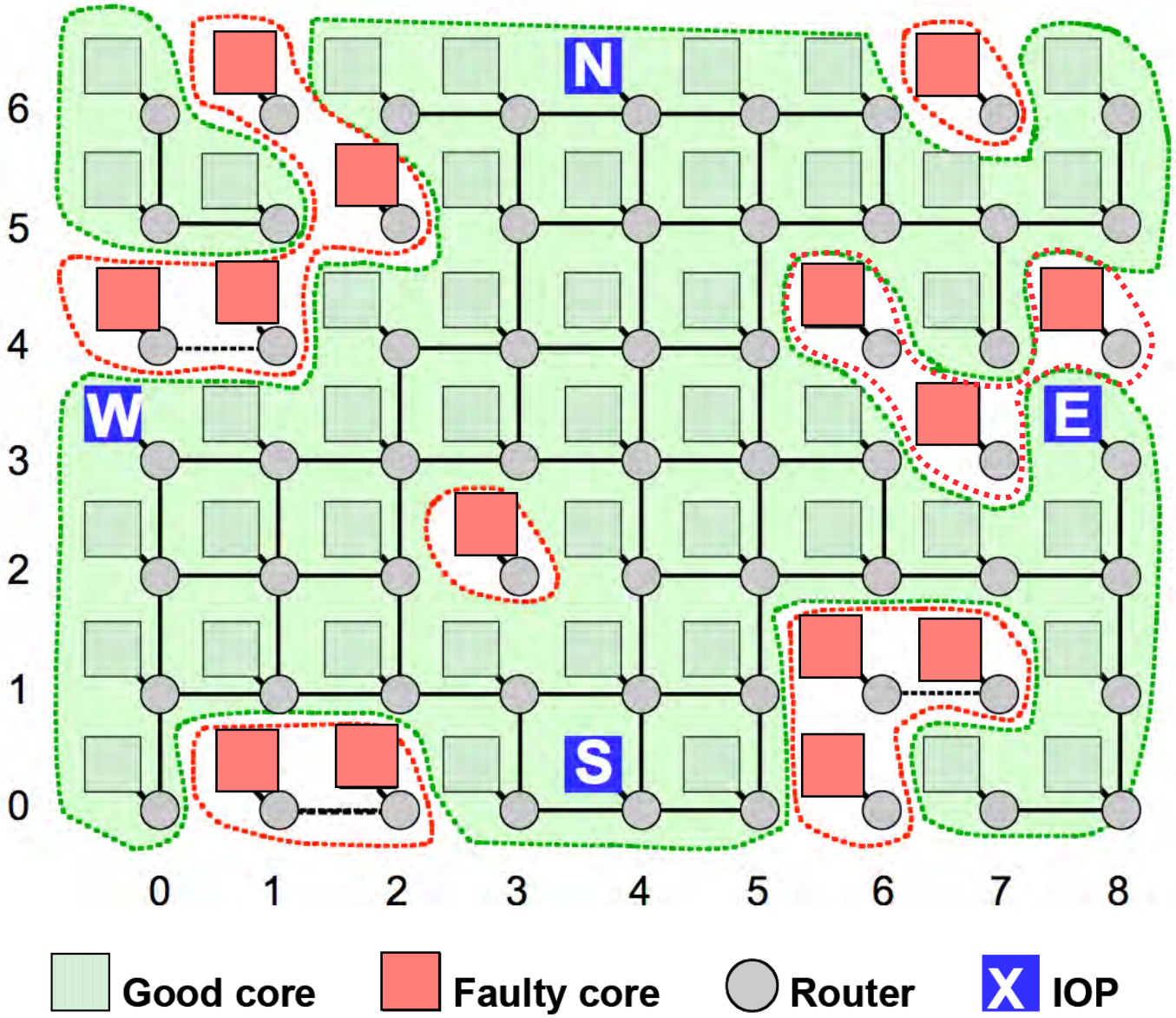
- The I/O Interface (IOP) is a Hardcore and a "Blottle Neck"

Preliminary Analysis of Several Options

- Increase the number of I/O ports
- Consider redundant IOPs
- Extend IOP connectivity with grid (adjacent nodes)
- …

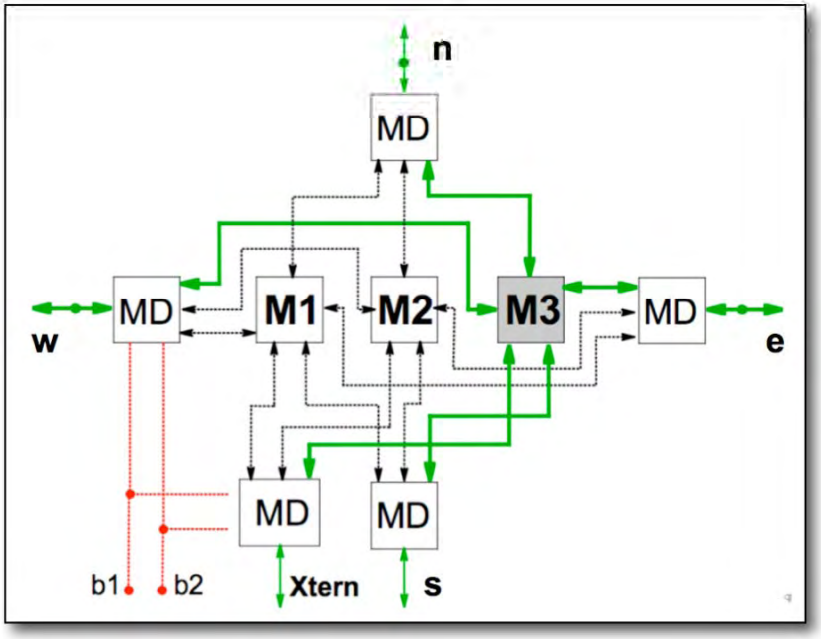
Increasing the Number of IOPs

Example of a 4-IOP Grid Including 14 Defective Cores



Redundant IOP Architecture

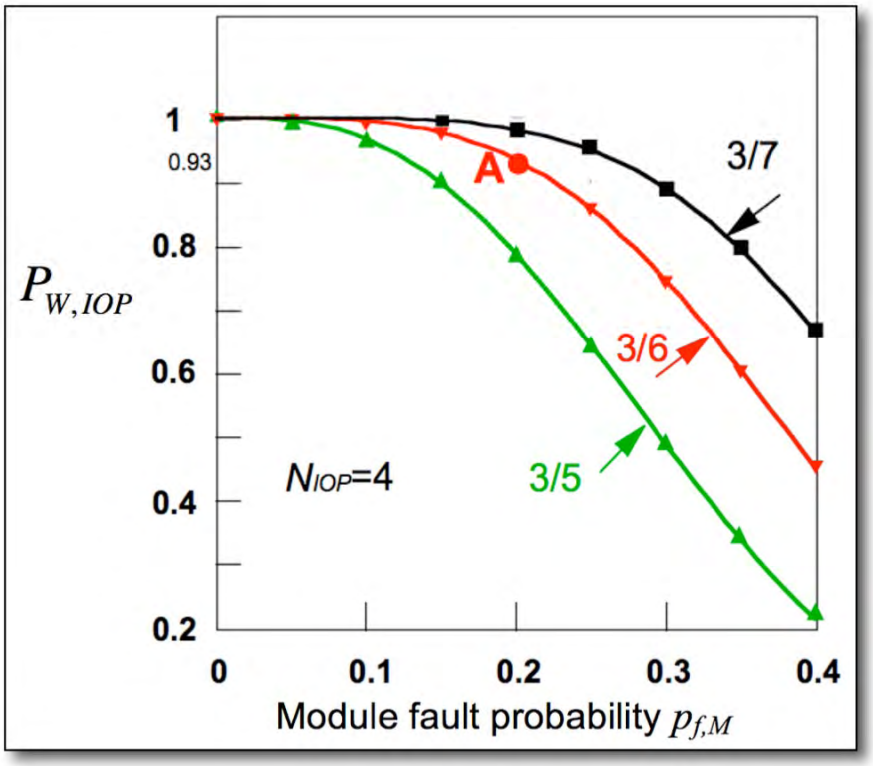
Example:
4-connect *R*IOP
with *R* = 3 Redundant I/O Modules (Mi)



Validation probability

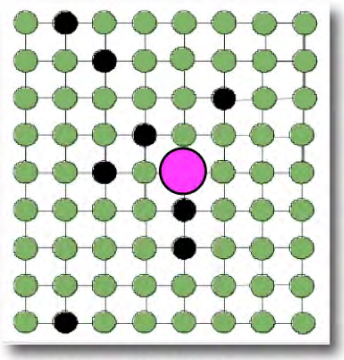
$$P_{W,IOP} = \left[\sum_{i=3}^{R} \binom{R}{i} \left(1 - p_{f,M}\right)^{i} p_{f,M}^{R-i} \right]^{N_{IO}}$$

Example:
Case of a 4-port Chip for *R* = 5,6,7 and *r* = 3

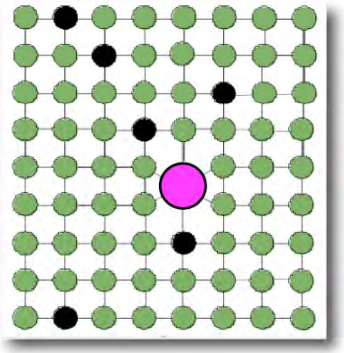


Chip Validation Criteria?
At least *r* out of *R* modules
are fault-free at start-up in each *R*IOP

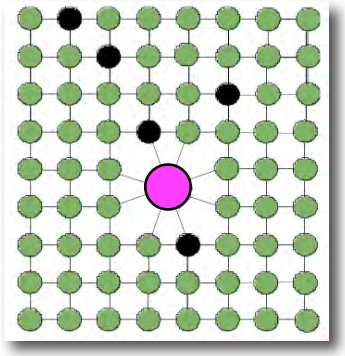
Modification of Grid Topology around each RIOP



Connectivity *nc* = 4



Connectivity *nc* = 6

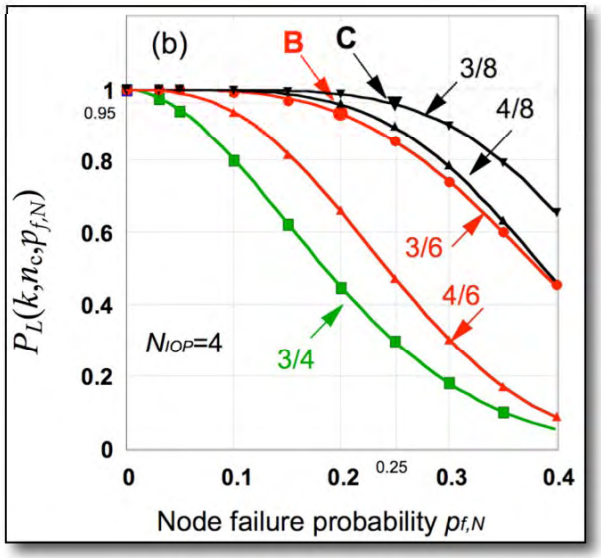


Connectivity *nc* = 8

RIOP

Prob. *k* / *nc* nodes adj / *R*IOP are OK

$$P_L(k,n_C,p_{f,N}) = \left[\sum_{i=k}^{n_C}\binom{n_C}{i}(1-p_{f,N})^i\, p_{f,N}^{n_C-i}\right]^{N_{IO}}$$



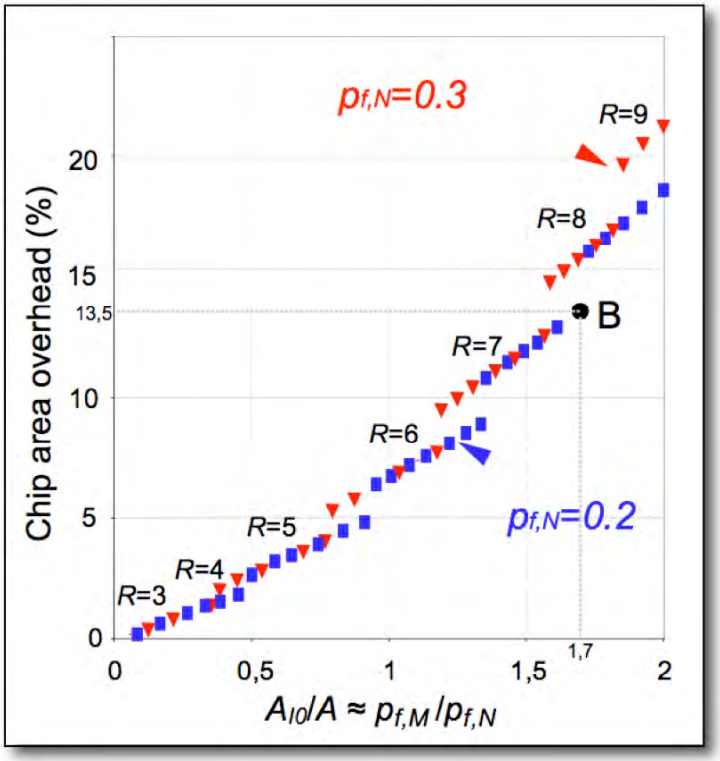
Example of Overhead Analysis

***N* = 300; *NIO* = 4; *nc* = 8**

VC1: To protect communication bandwidth of each *R*IOP, at least 3/8 neighboring nodes must be fault-free.

VC2: Validation yield threshold: $P_{W,IOP}$ x $P_L(k,n_c,p_{f,N})$ ≥ 80%.

$$Q = \frac{(R-1)\;\; N_{IO}\cdot A_{IO}}{N\cdot A}$$



Concluding Remarks

- Study of the protection of the IOPs in multiport grid architectures
- Analysis of the dependability gain and overhead induced: redundancy, connectivity and chip area

- Grid topology and connectivity
- Self-diagnosis and coverage
- Application reconfiguration