

No Free Lunch in Soft Error Protection?

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Results That Made Us Think

- ▶ [Seshia, Li, Mitra, DATE 2007]: validity of set of properties covering the specs of a communication chip
- ▶ Results: for two-thirds of flip-flops, properties hold even if a soft error occurs in that flip-flop (formally proven)
- ▶ Why?

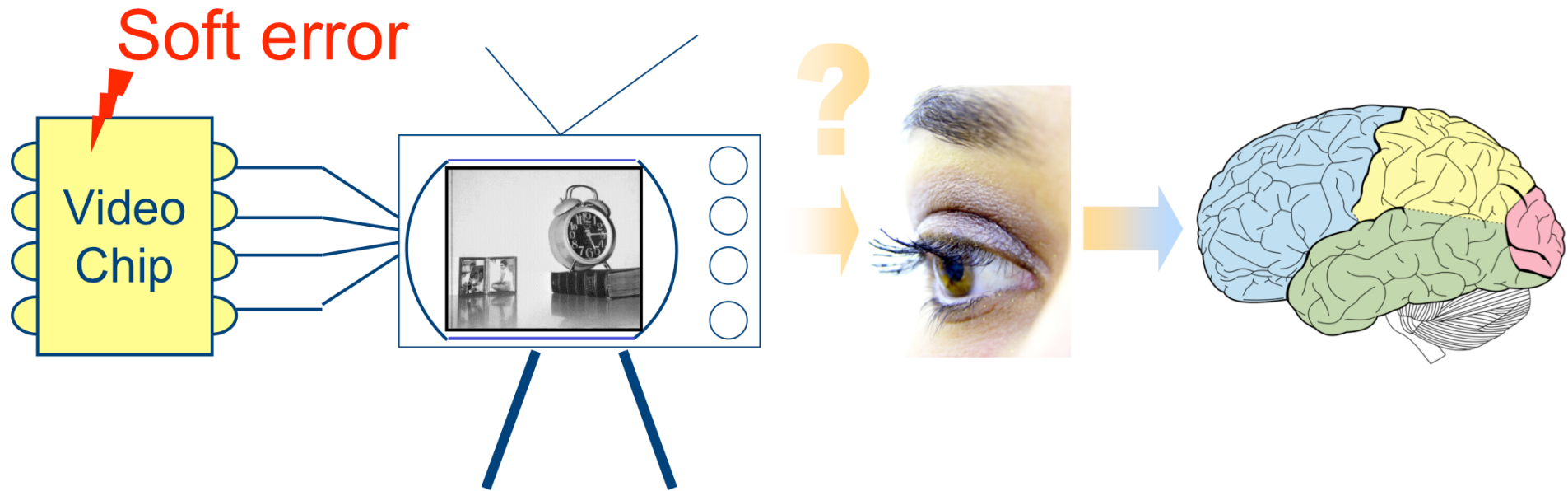
Possible Explanations (1)

- ▶ Explanation 1: these flip-flops are redundant
 - permanent errors on that flip-flops have no impact on system behavior (are masked)
 - we don't know for sure, but typically two-thirds of the design are not redundant!
- ▶ Explanation 2: they are one-cycle redundant
 - one-cycle bit flips on that flip-flops are masked
 - data for ISCAS circuits suggest that redundancy and one-cycle redundancy are very similar
 - see paper

Possible Explanations (3)

- ▶ Explanation 3: these flip-flops are not redundant in classical sense
- ▶ But design **resilient** against soft errors on that flip-flops **with respect to property set**
- ▶ General concept valid for several applications
 - applications with a human user (multimedia)
 - errors handled by application (communication)
 - inherently error-tolerant applications (recognition, mining, synthesis, tracking, control)

Example: Cognitive Resilience



- ▶ Are there errors which do not result in visible effects?
- ▶ Such errors require no hardening
- ▶ Details: our DSN paper

Summary

- ▶ Difference between „redundant“ and „resilient“ appears to be large
 - derived by exclusion
- ▶ Better understanding of „resilient“ could lead to low-cost hardening of unreliable hardware (e.g. nano blocks)
- ▶ Yes, this could be the free lunch!

Results

▶ Metric for imaging applications

- composition of PSNR, SSIM, psychovisual model

▶ Experiment: JPEG Compressor

- from www.opencores.org
- 54.8% error sites need no hardening



no error



acceptable error



unacceptable error

Vision: Computing of Tomorrow

Software

(including resilience and security mechanisms)



Reliable Hardware
(CMOS, fault-tolerant)

low integration density
high energy consumption

Unreliable Hardware
(Nano blocks, future tech.)

high integration density
low energy consumption