Performance Comparison between Self-timed Circuits and Synchronous Circuits Based on the Technology Roadmap of Semiconductors

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Agenda

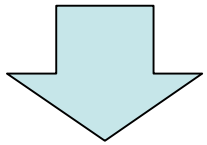
- Introduction
- Technology models and parameters
- Evaluation setup
- Evaluation results
- Conclusion

Background

- As VLSI technology advances, delay variations are becoming more important
- They can be typically classified as “Systematic variations” and “Random variations”
- Random variations caused by the following reasons are becoming main issues
  - Random process variations
    - Lithography-induced variations
    - Gate dielectric variations
    - Chemical-Mechanically-Polished variations
    - Dopant variations
  - Voltage supply noises
  - Heat generation in each device
  - Crosstalk noise

Background

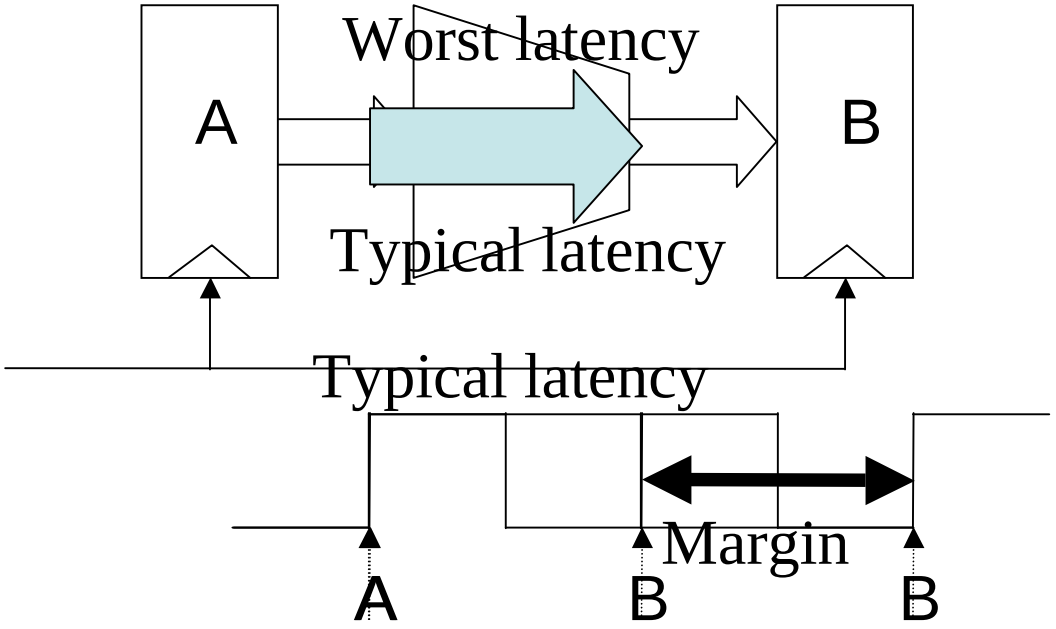
- As VLSI technology advances, delay variations are becoming more important
- They can be typically classified as “Systematic variations” and “Random variations”
- Random variations caused by the following reasons are becoming main issues
- They exhibit almost complete randomness even in the neighborhood devices



- The timing margin that guarantees the correct order relations of signal transitions must be decided under the worst conditions

Timing margin(1)

- Synchronous circuits
  - The latency between source latches and destination latches is obtained by the inverse of clock frequency

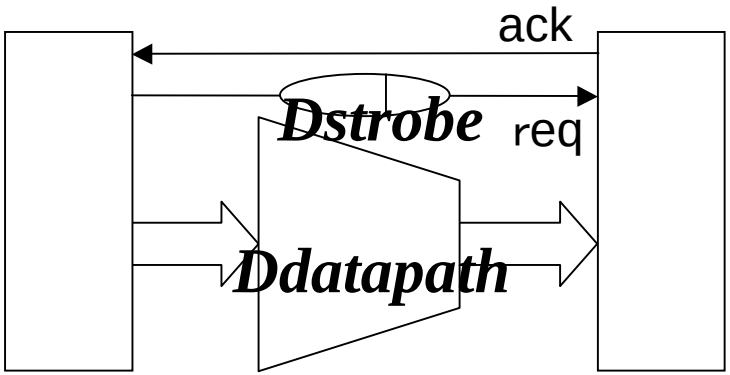


  - As random variations become large, the margin that guarantees the correct operations must become large

Timing margin(2)

- Asynchronous bundled data transfer circuits
  - Use some delay elements as a matched-delay whose delay is larger than the corresponding combinational circuit

$$Dstrobe > Ddatapath$$



- Delays of a combinational circuit and the corresponding delay elements are affected almost similarly by the changes in the operating environment
- As random variations become large, the margin that guarantees the correct operations must become large

Timing margin(2)

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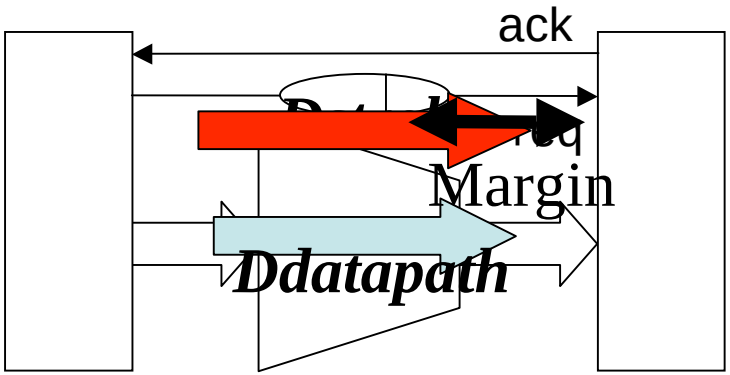

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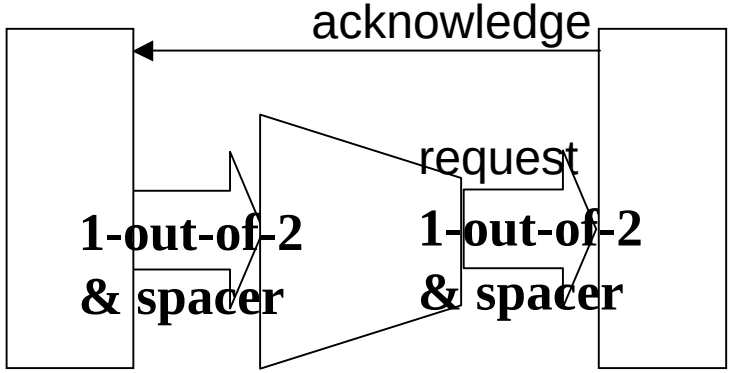
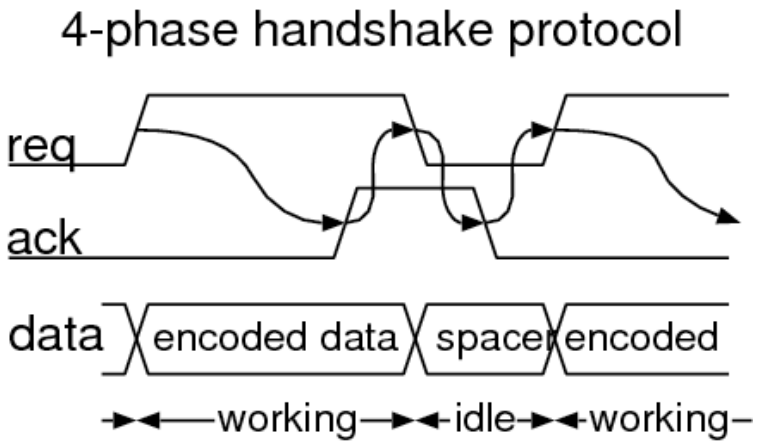
Timing margin(3)

- Asynchronous dual-rail encoded circuits
  - A logical value is represented by two physical lines



	(pos, neg)
Logic 1	(1,0)
Logic 0	(0,1)
Spacer	(0,0)



- Working phase
  - Encoded data is processed
- Idle phase
  - Combinational circuit must be initialized before the next data is inserted
  - The spacer is processed

Timing margin(3)

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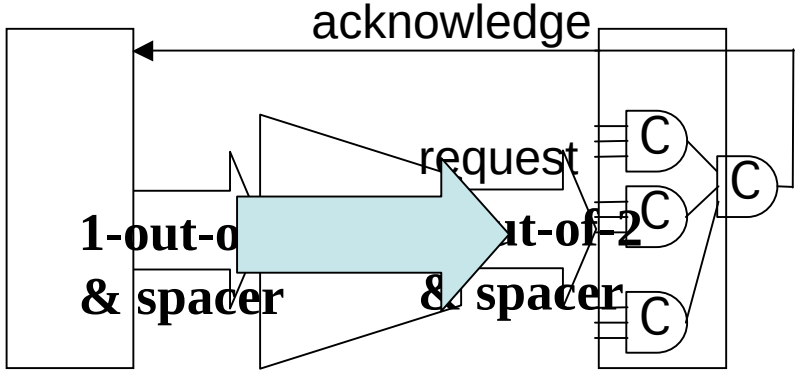

	(pos, neg)
Logic 1	(1,0)
Logic 0	(0,1)
Spacer	(0,0)

  - No timing constraint : Delay insensitivity
  - Can work in accordance with delay variations and no timing margin
  - Can apply the delay variations due to input vector differences
  - Large energy dissipation due to signal transitions in all the bits every cycle

Objective

- The purpose of this study is to compare synchronous circuits and 4-phase dual-rail encoded asynchronous circuits in the Moore's Law-based trend in chip development
- We will show some evaluation results using 90nm, 65nm, 45nm, and 32nm process technologies

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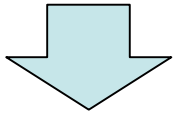
Technology models and parameters

- ITRS (International Technology Roadmap of Semiconductors)
  - A famous assessment of the semiconductor industry's technology requirements
  - It does not provide transistor models

- Asynchronous circuits address ITRS challenges
  - Impossible to move signals across large die within one clock cycle in a power-efficient manner
  - Difficult to run control and dataflow processes at the same clock rate
- Predicted shift to self-timed design style : 20% in 2012 and 40% in 2020

Technology models and parameters

- ITRS (International Technology Roadmap of Semiconductors)
  - A famous assessment of the semiconductor industry's technology requirements
  - It does not provide transistor models
- PTM (Predictive Technology Model)
  - Provides SPICE compatible parameters for future technology generation
  - Provides an online tool that can customize parameters with user's technology specifications. It also provides not only nominal models but also variation models



- We evaluate the variance of delays in the near-term future technologies using these models and parameters

Model parameters based on the ITRS and PTM

Technology parameters (ITRS07)

	90nm		65nm		45nm		32nm	
	HP	LSP	HP	LSP	HP	LSP	HP	LSP
Leff[nm]	32	32	25	25	18	18	13	13
Vth[V]	0.195	0.482	0.134	0.534	0.103	0.535	0.093	0.547
Vdd[V]	1.1	1.2	1.1	1.2	1.0	1.1	0.9	0.95
Tox[nm]	1.2	2.1	1.1	1.9	0.65	1.4	0.5	1.1
Rdsw[Ohm]	180	180	200	180	180	180	170	180

- HP: High-Performance model which refers to chips of high complexity, high performance, and high energy dissipation
- LSP: Low-Standby-Power model which refers to chips of lower performance with the lowest possible static energy dissipation for mobile systems

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Evaluation setup(1)

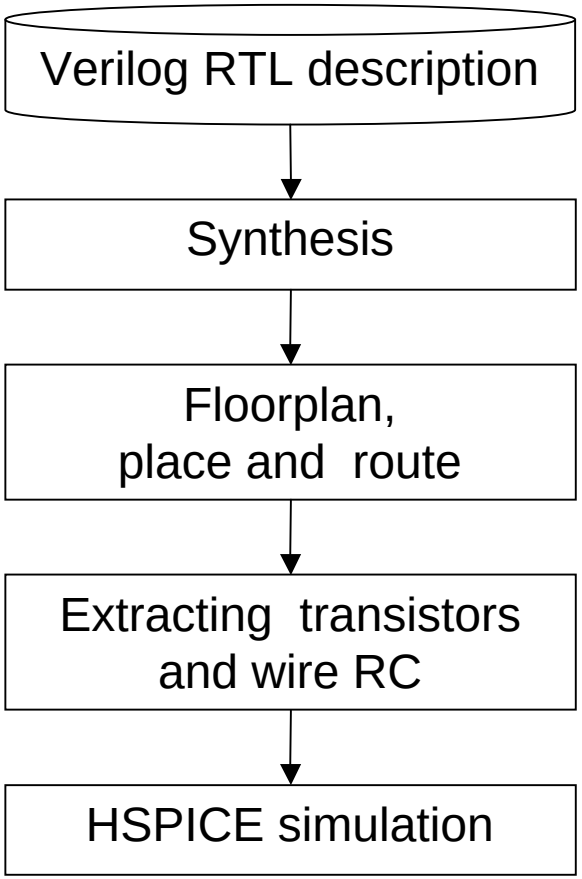
- We evaluate the performance under the standard, the best, and the worst conditions in order to compare the variance of delays.

	(a) Standard	(b)Worst	(c)Best
Process (PMOS, NMOS)	(Center, Center)	(Slow, Slow)	(Fast, Fast)
Supply voltage [V]	Std value	Std value - 0.1	Std value + 0.1
Temperature [C]	50	100	25

- Synchronous cycle-time : $\max\{D_{comb} + D_{setup} + D_{hold}\}$
  - Under the worst case conditions since a clock cycle must be decided considering the worst variations
- Self-timed cycle-time : $\mathrm{ave}\{D_{work} + D_{idle}\}$
  - Under the standard case conditions since they work in accordance with delay variations
  - Input vector differences : 100 random inputs (switch factor : 0.5)

Evaluation setup(2)

- Target functions
  - 32bit adder circuits
    - Synchronous : CLA, Binary-tree CLA
    - Self-timed : RCA
  - 32bit shifter circuits
  - ISCAS89 benchmark circuits
- Design flow
  - Synthesis : Synopsys Design analyzer using the same standard cell library
  - Floorplan, P&R : Synopsys Astro
  - Extracting SPICE file : Mentor Calibre
  - Simulation : HSPICE
    - Power : 100 random inputs (switch factor is 0.5)



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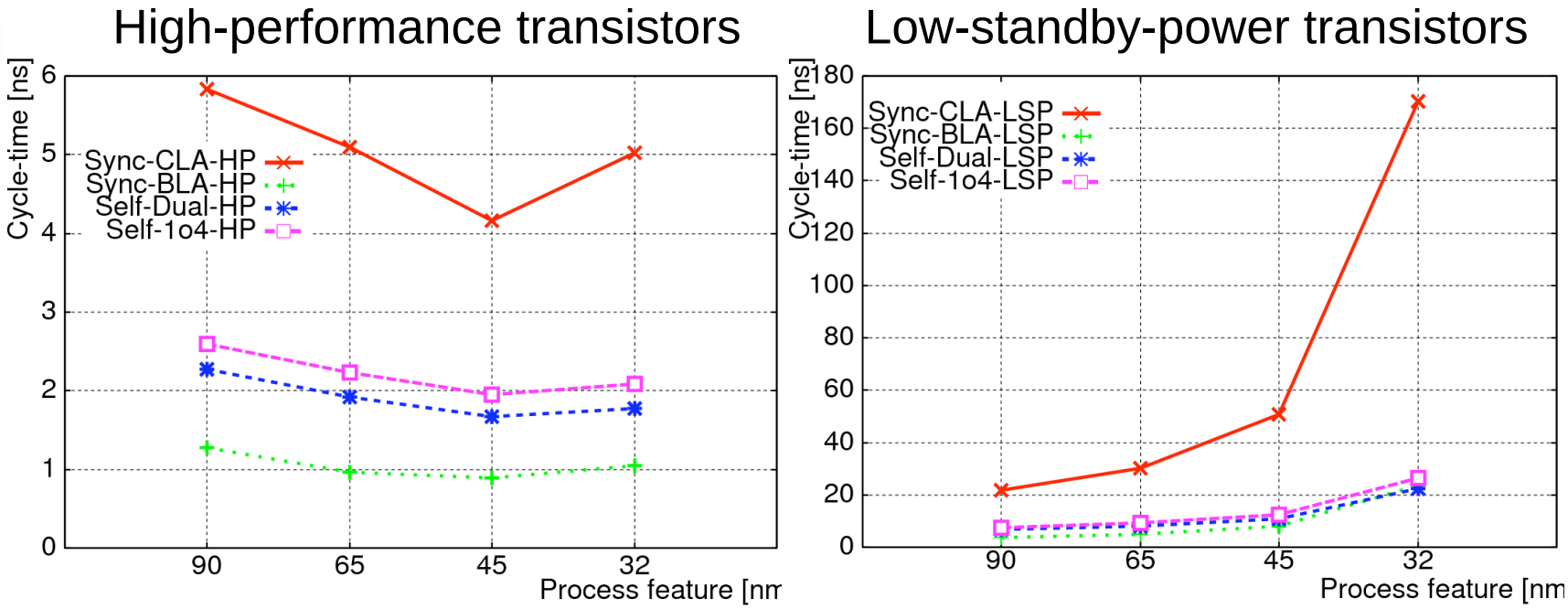
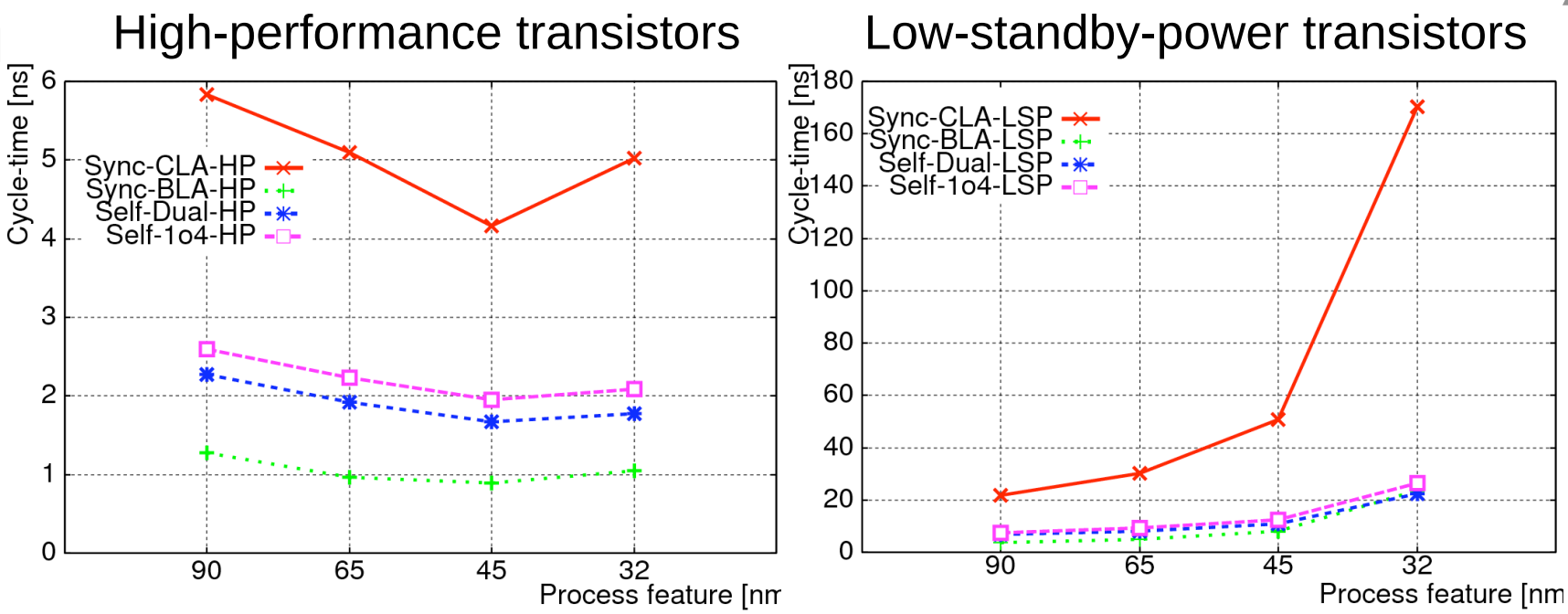
Cycle-time comparison : 32bit add



- The cycle-time becomes large in the 32nm process technology
- Self-timed circuits and small depth circuits are effective in the future technologies

- The cycle-time becomes large as the feature size decreases
- The delay of the synchronous BLA circuit is almost same as the self-timed circuits

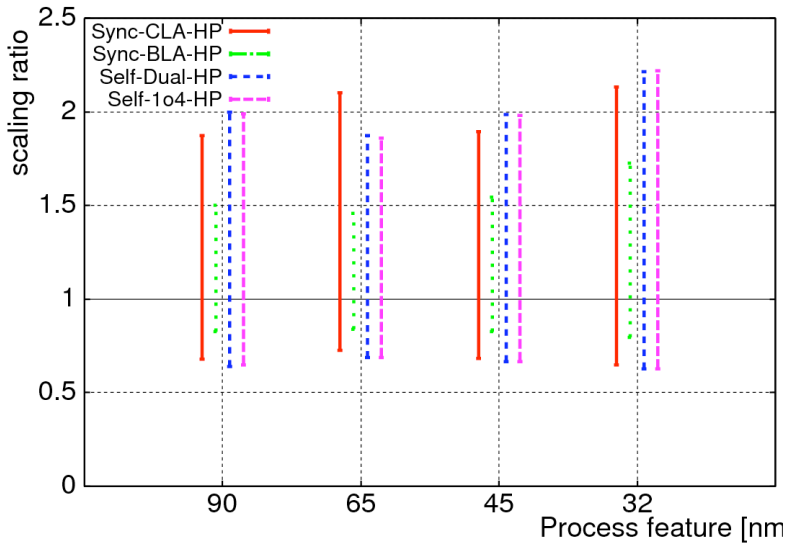
Cycle-time comparison : 32bit add

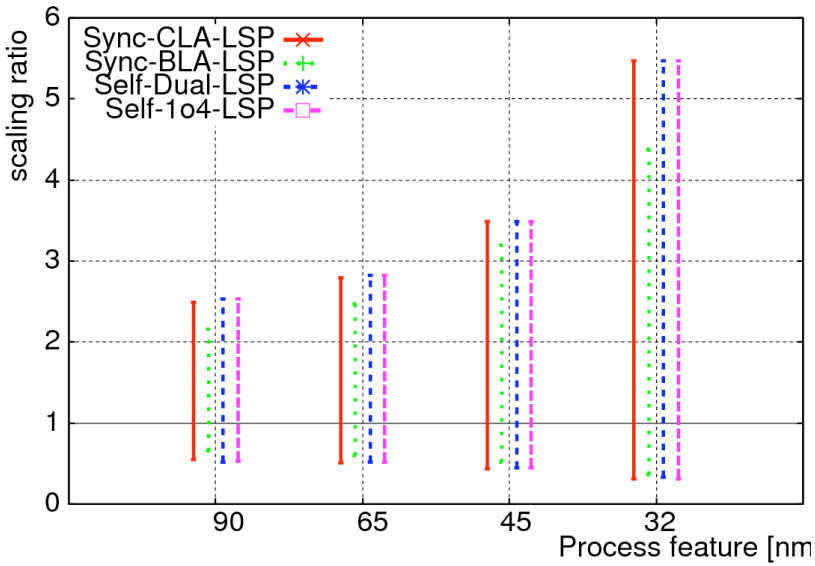


- The variations of Low-Standby-Power transistors is larger than that of High-Performance transistors
- It affects the performance of synchronous circuits directly

- In the view point of performance, self-timed circuits are suitable for LSP-oriented applications

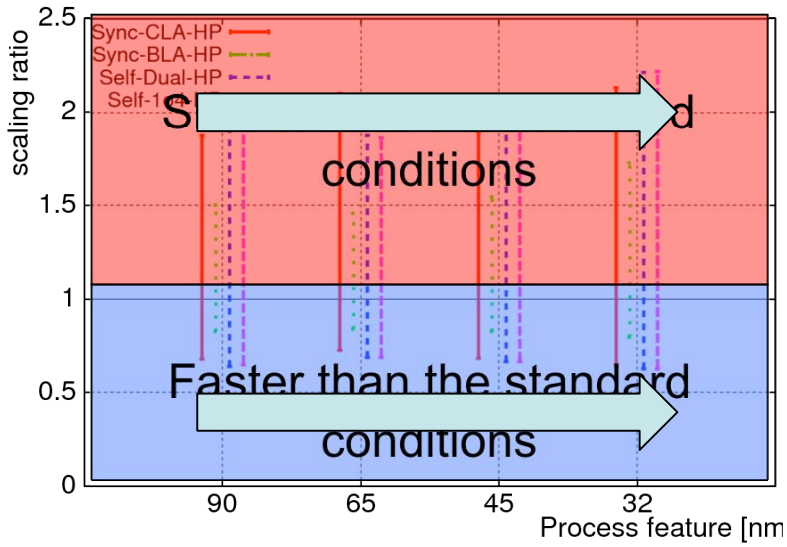
Variation comparison

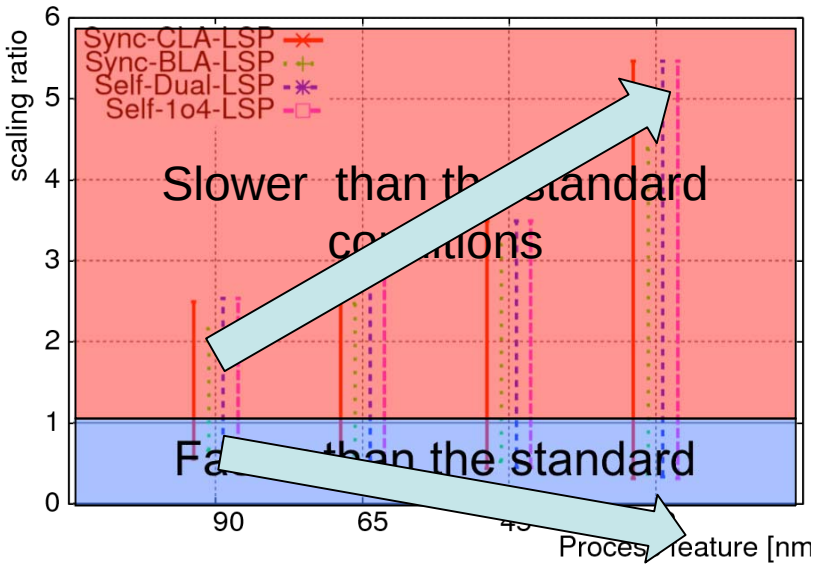




- Scaling ratio : the ratio of varied delay to the delay in the standard conditions
- The delay variance of HP transistors is almost same as the feature size decreases
- The delay variance of LSP transistors becomes large as the feature size decreases

Variation comparison





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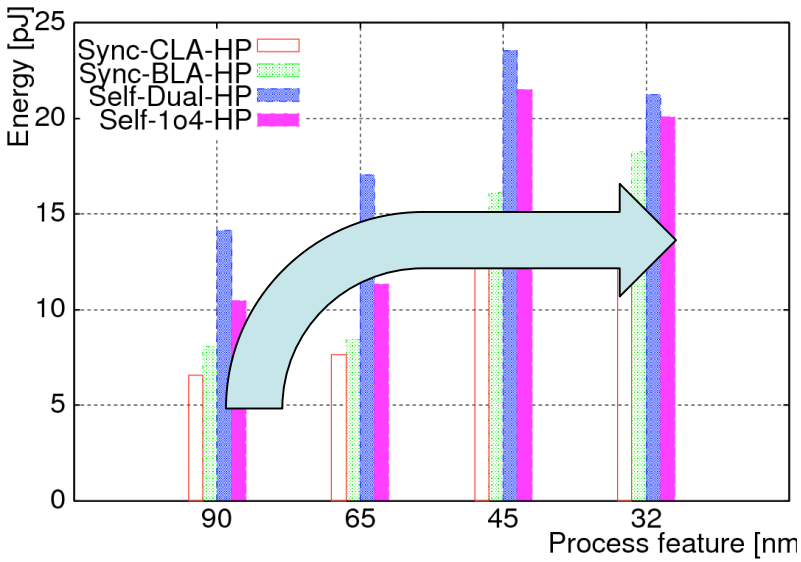
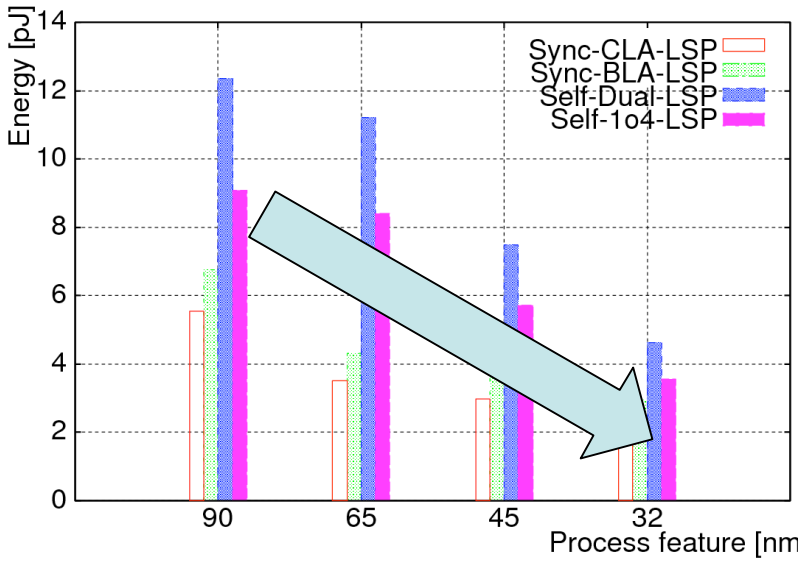
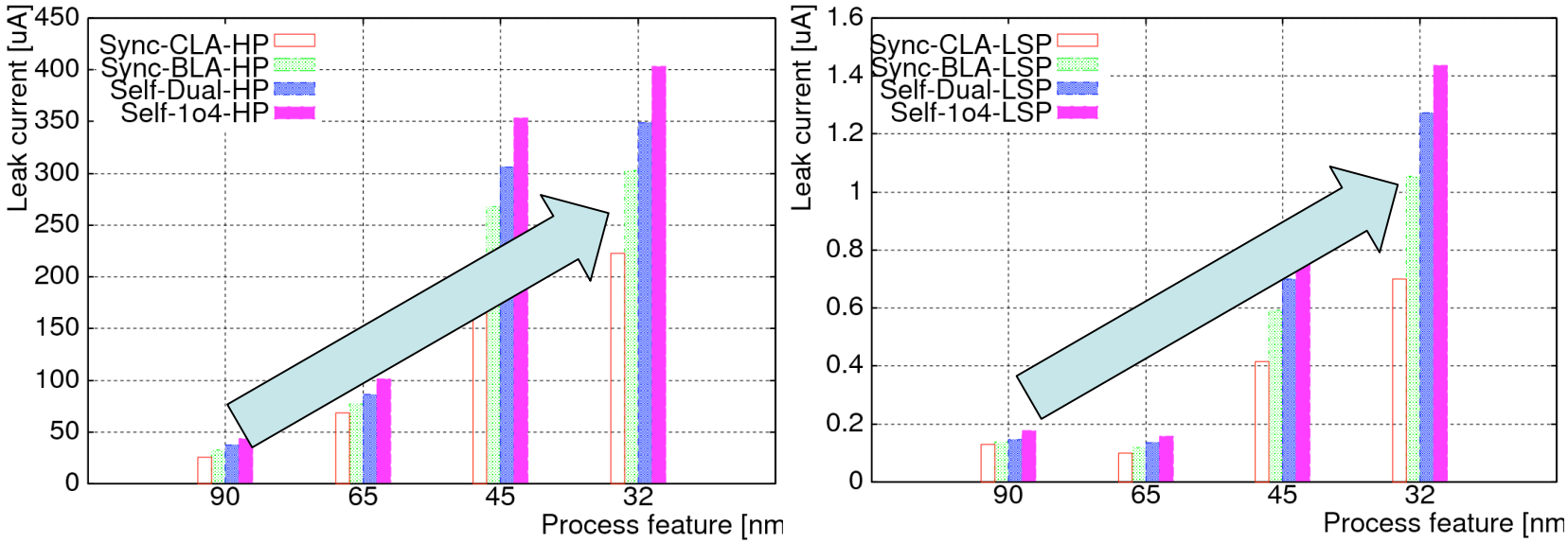
Energy dissipation comparison





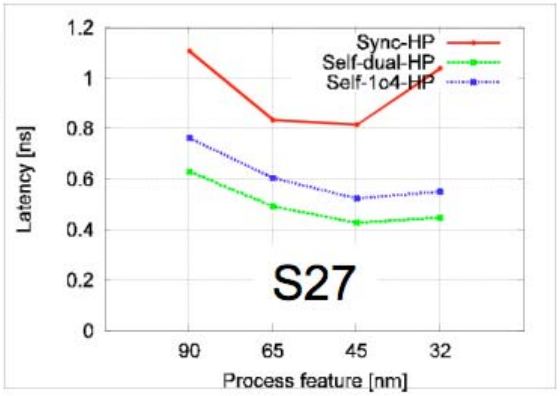
- The energy dissipation of self-timed circuits is 1.5 times larger than synchronous circuits in the 90nm process technology
- The difference between synchronous circuits and self-timed circuits decreases as the feature size decreases
  - The energy dissipation of HP transistors is saturated as the feature size decreases
  - The energy dissipation of LSP transistors decreases as the feature size decreases

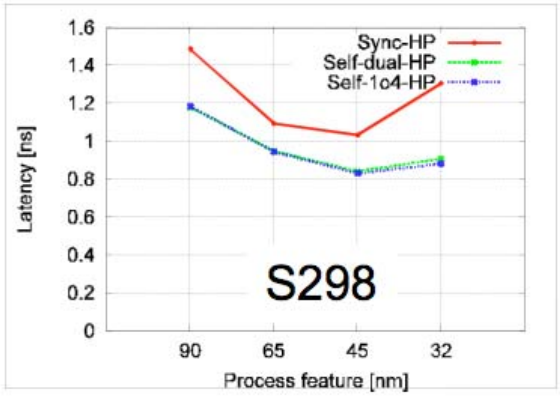
Leakage current comparison

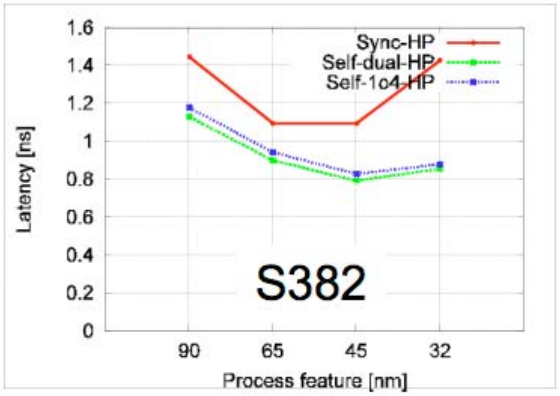


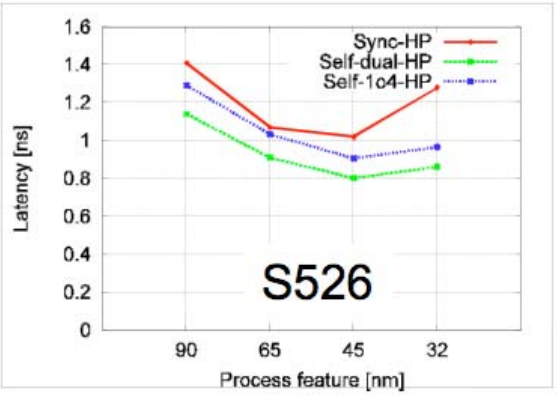
- Leakage current is almost proportional to the number of transistors
- The leak current of High-Performance transistors is about 175~280 times larger than that of Low-Standby-Power transistors
- The leakage current becomes large as the feature size decreases

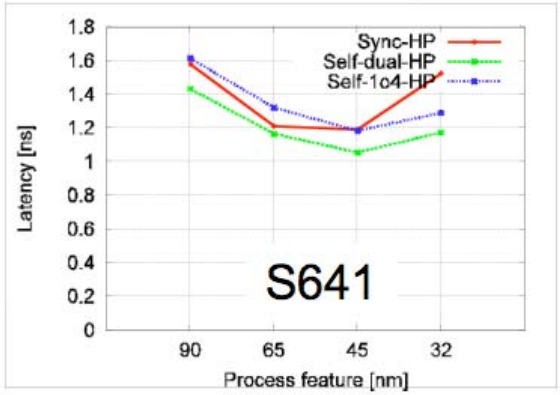
ISCAS89 delay comparison (HP)

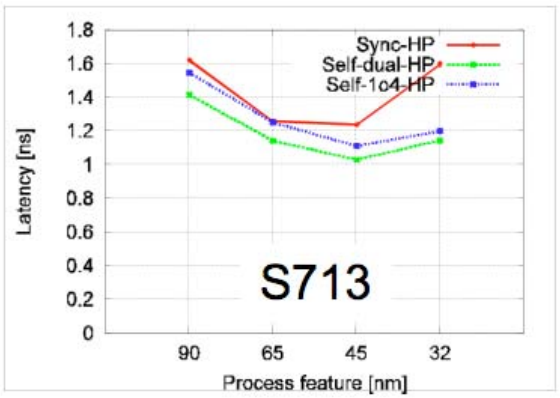


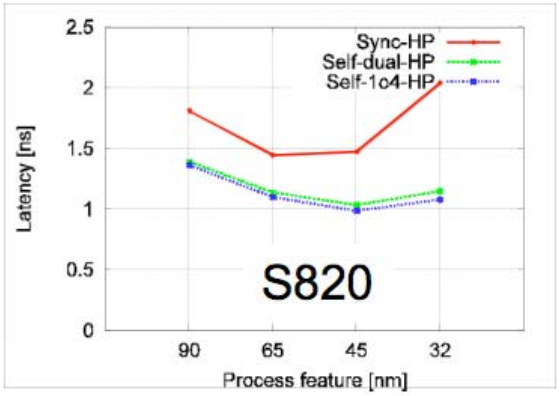


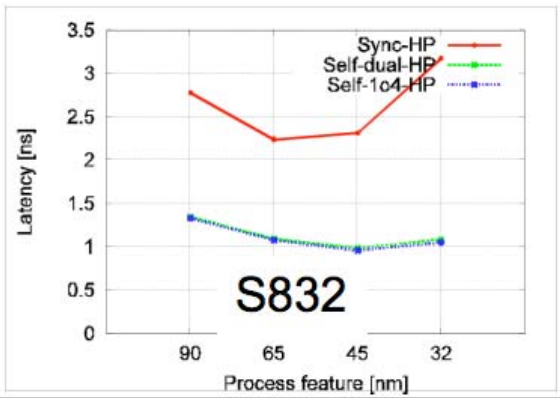


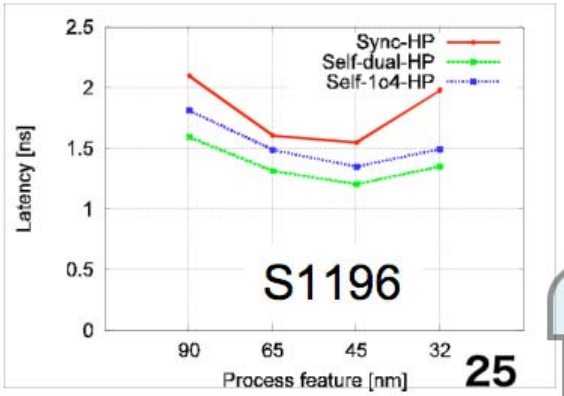




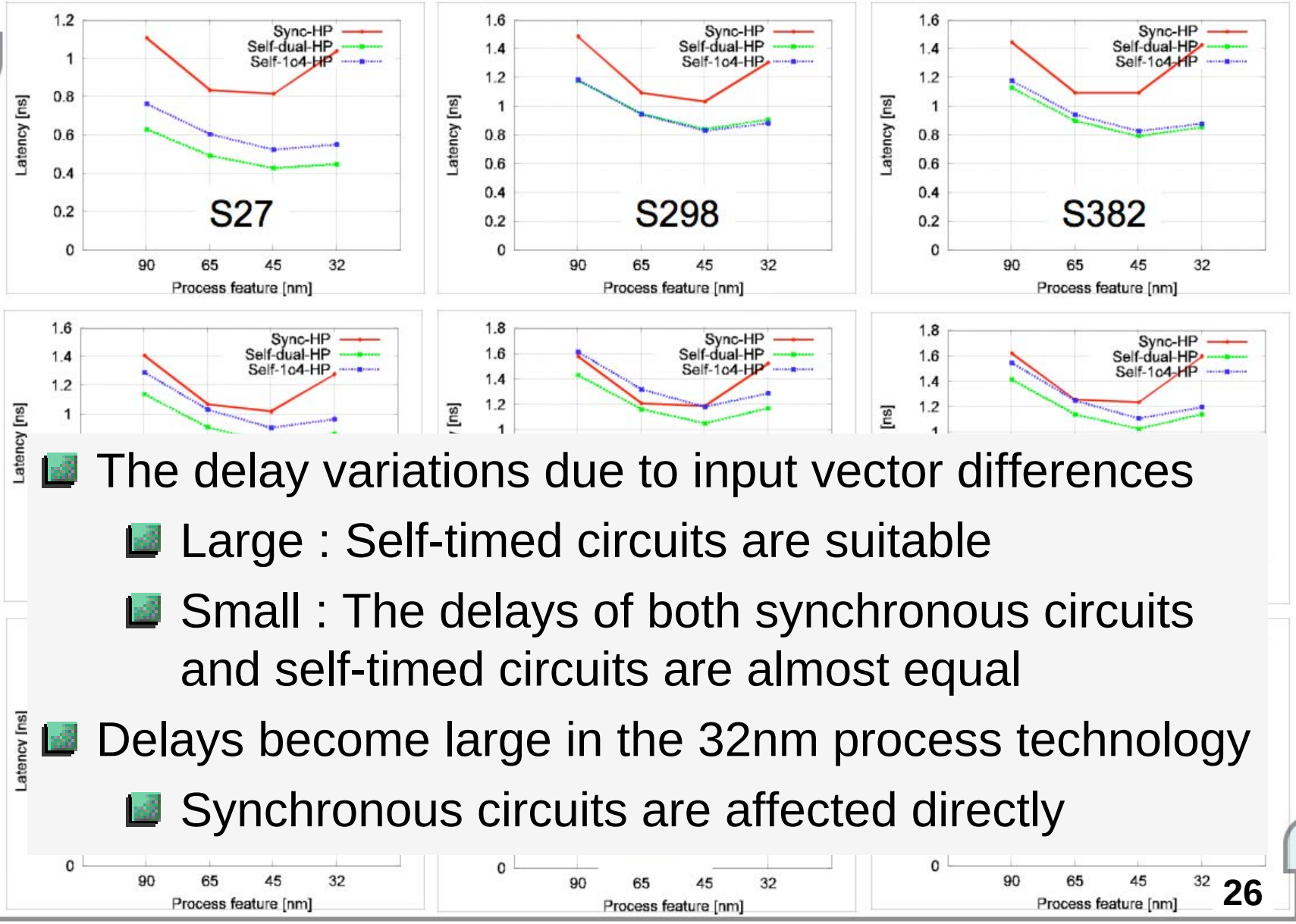






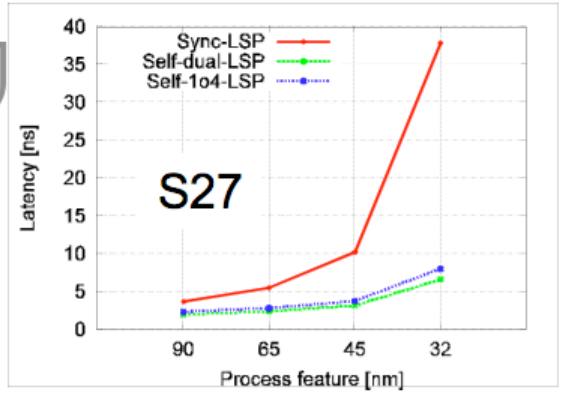


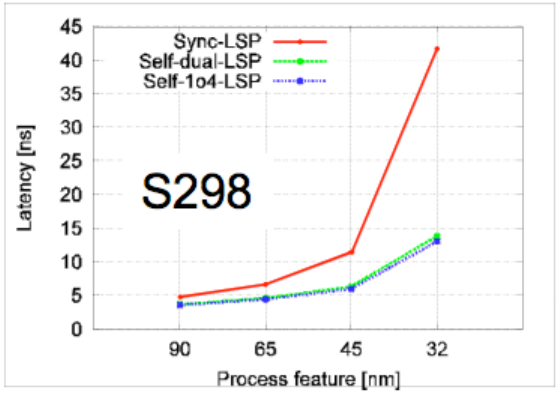
ISCAS89 delay comparison (HP)

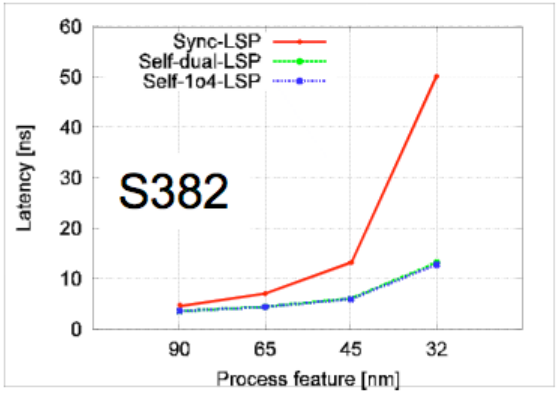


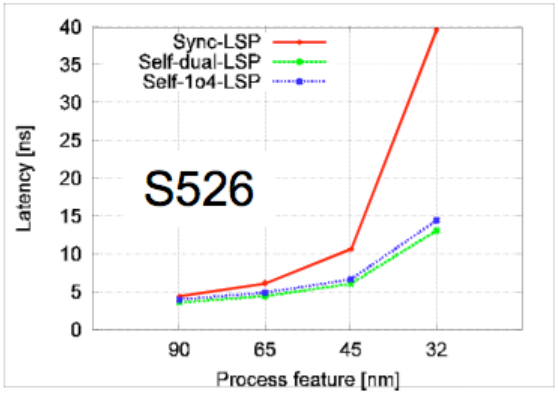
- The delay variations due to input vector differences
  - Large : Self-timed circuits are suitable
  - Small : The delays of both synchronous circuits and self-timed circuits are almost equal
- Delays become large in the 32nm process technology
  - Synchronous circuits are affected directly

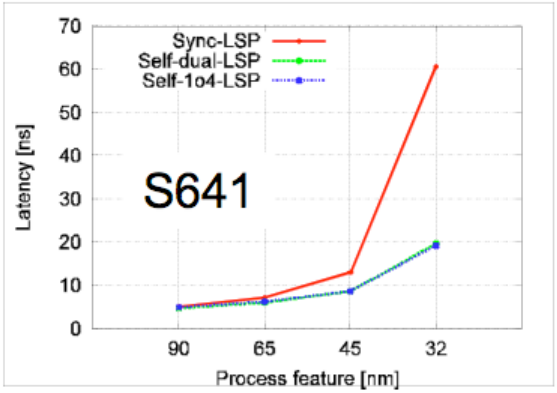
ISCAS89 delay comparison (LSP)

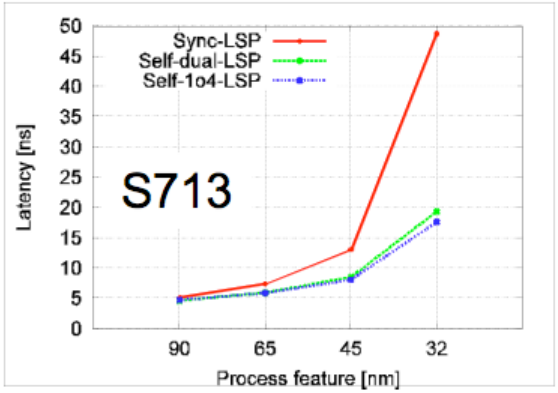


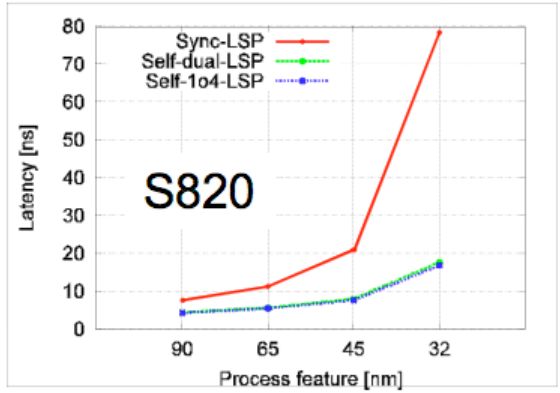


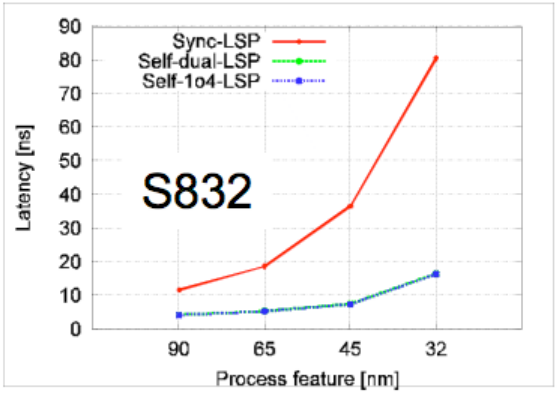


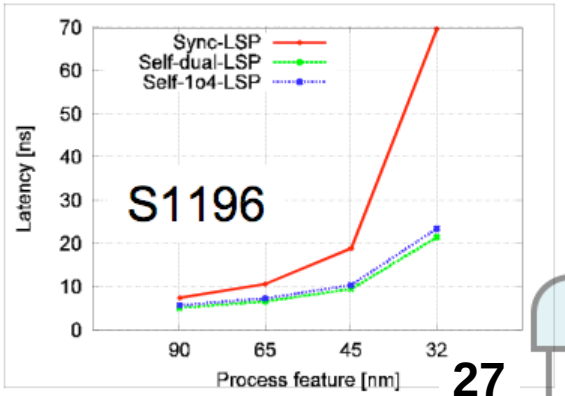












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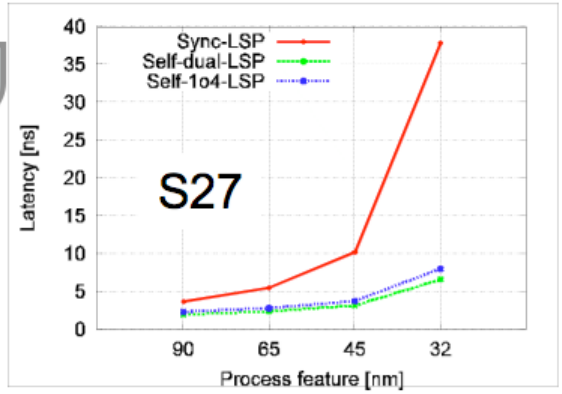
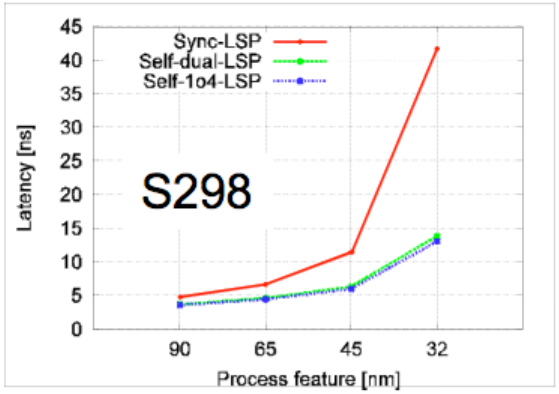
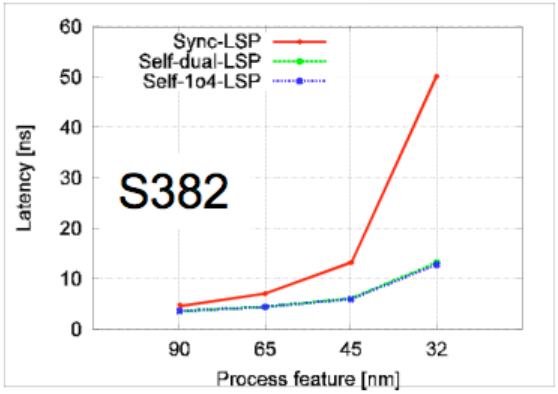
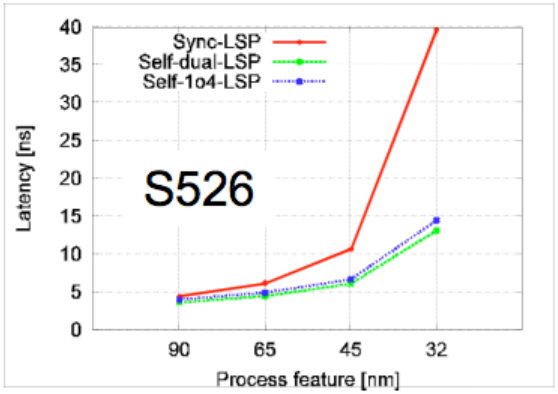
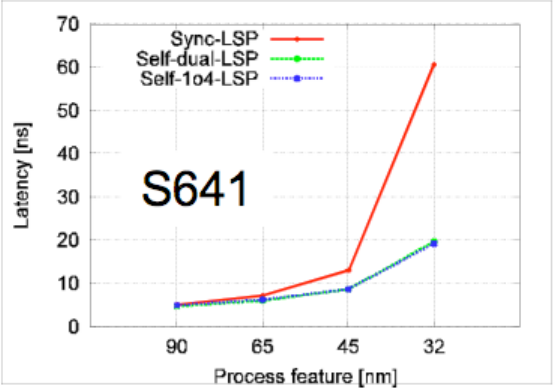
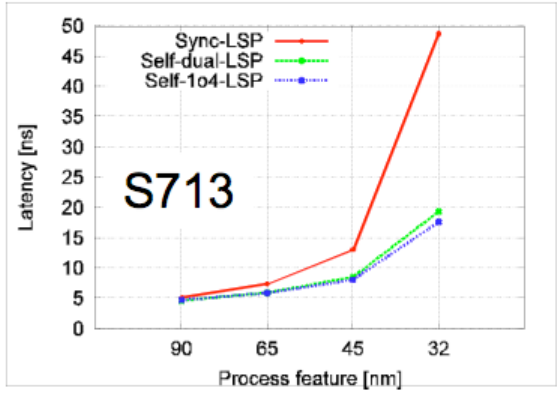


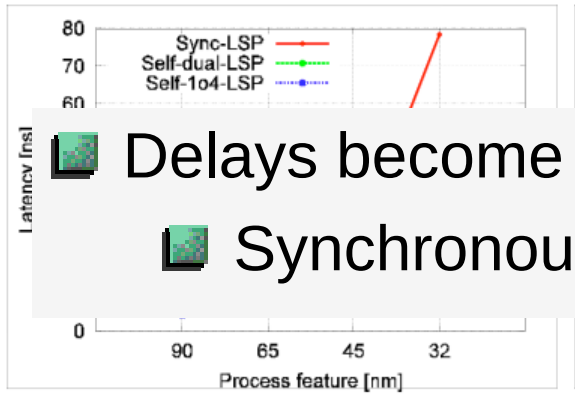


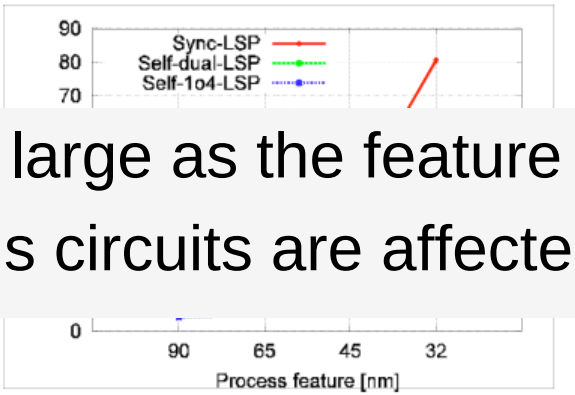


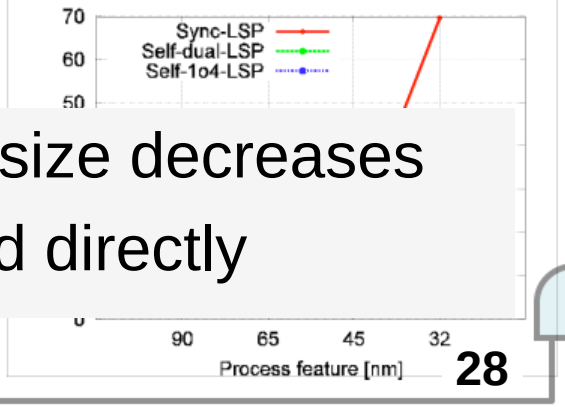






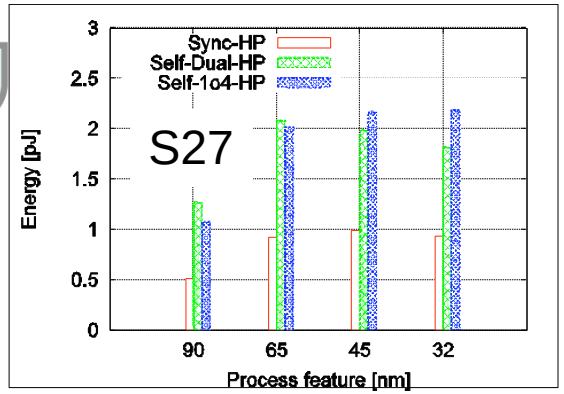


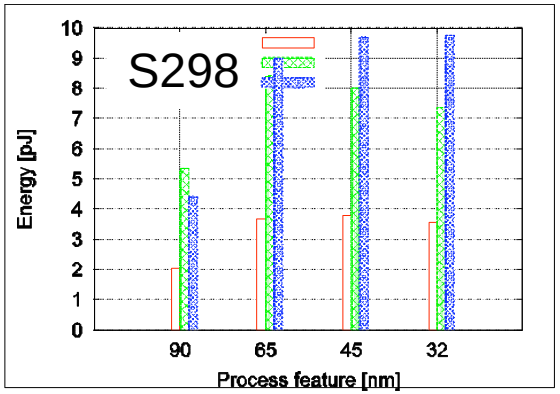


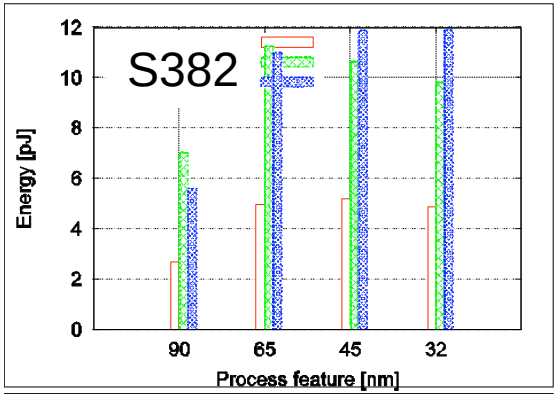


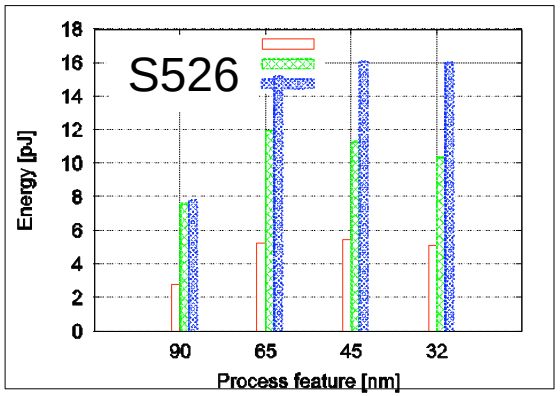
- Delays become large as the feature size decreases
  - Synchronous circuits are affected directly

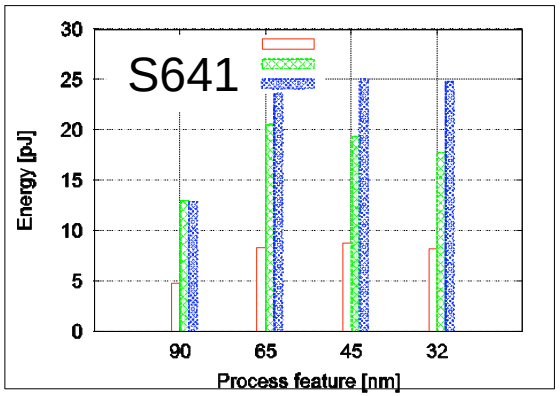
ISCAS89 energy comparison (HP)

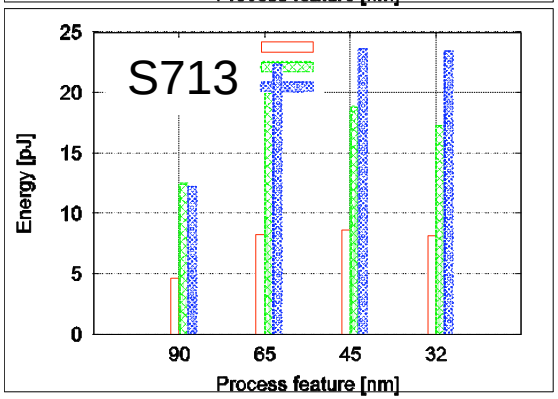


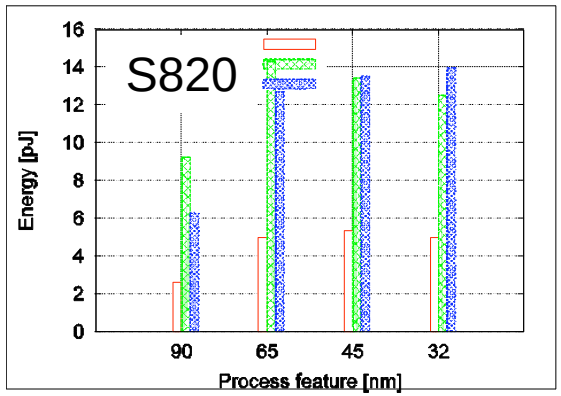


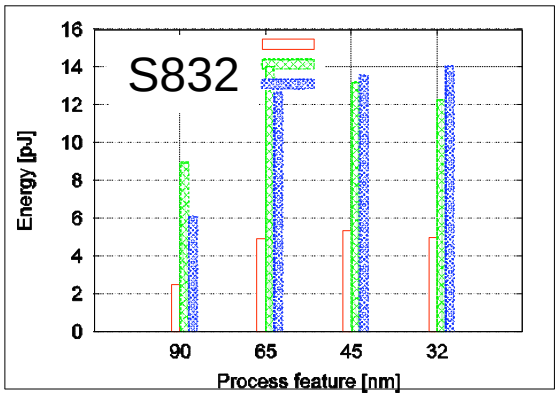


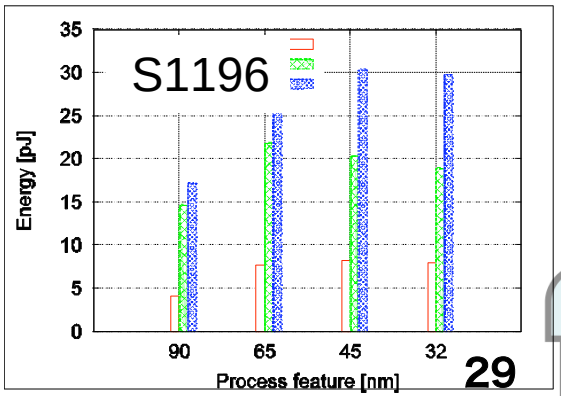




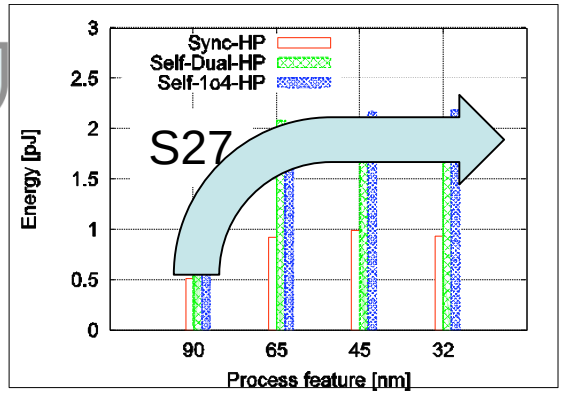


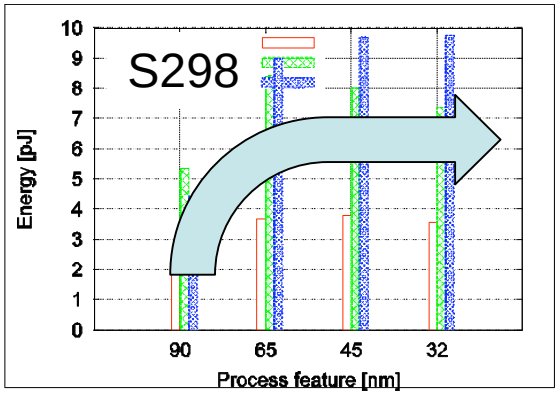


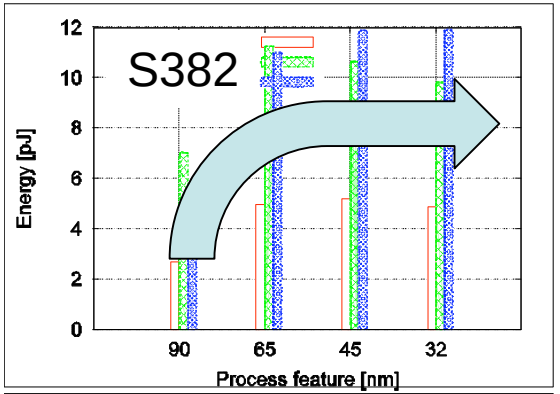


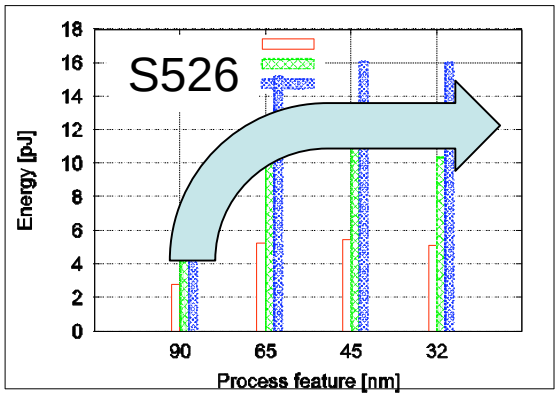


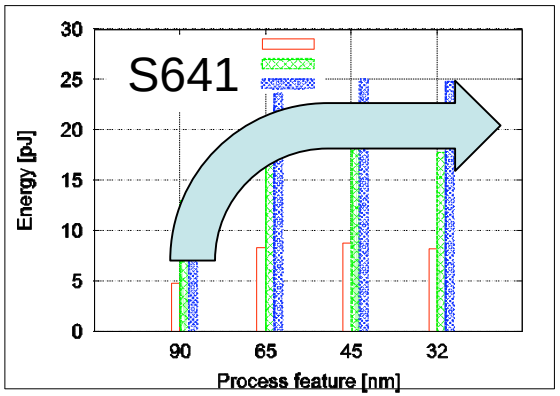
ISCAS89 energy comparison (HP)

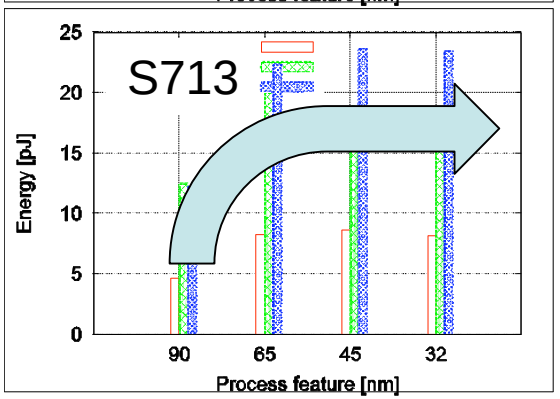


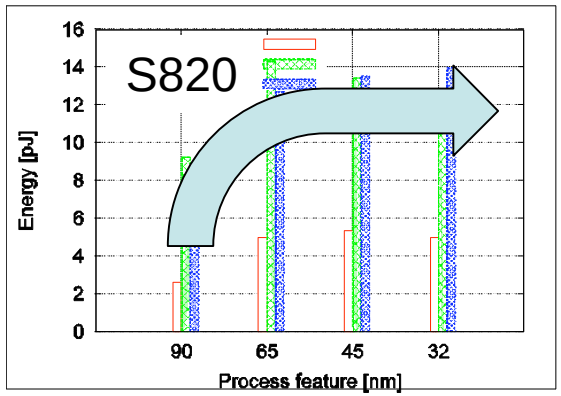


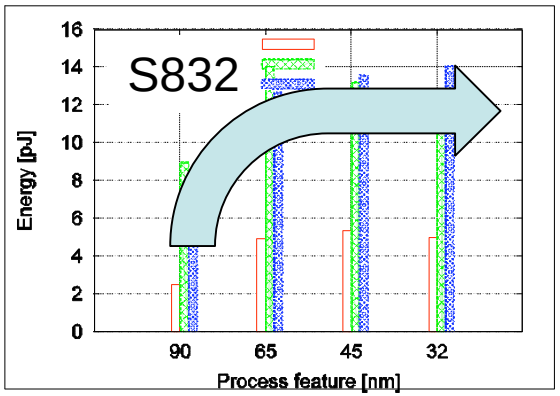


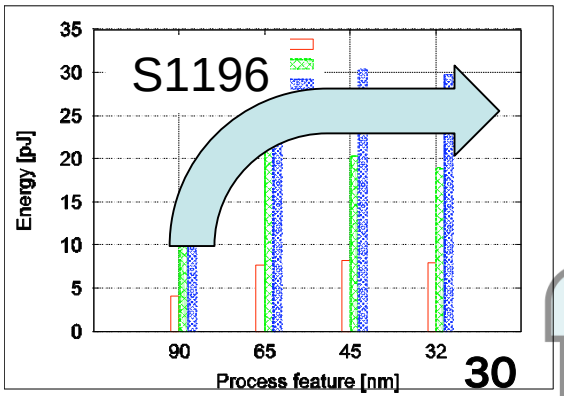




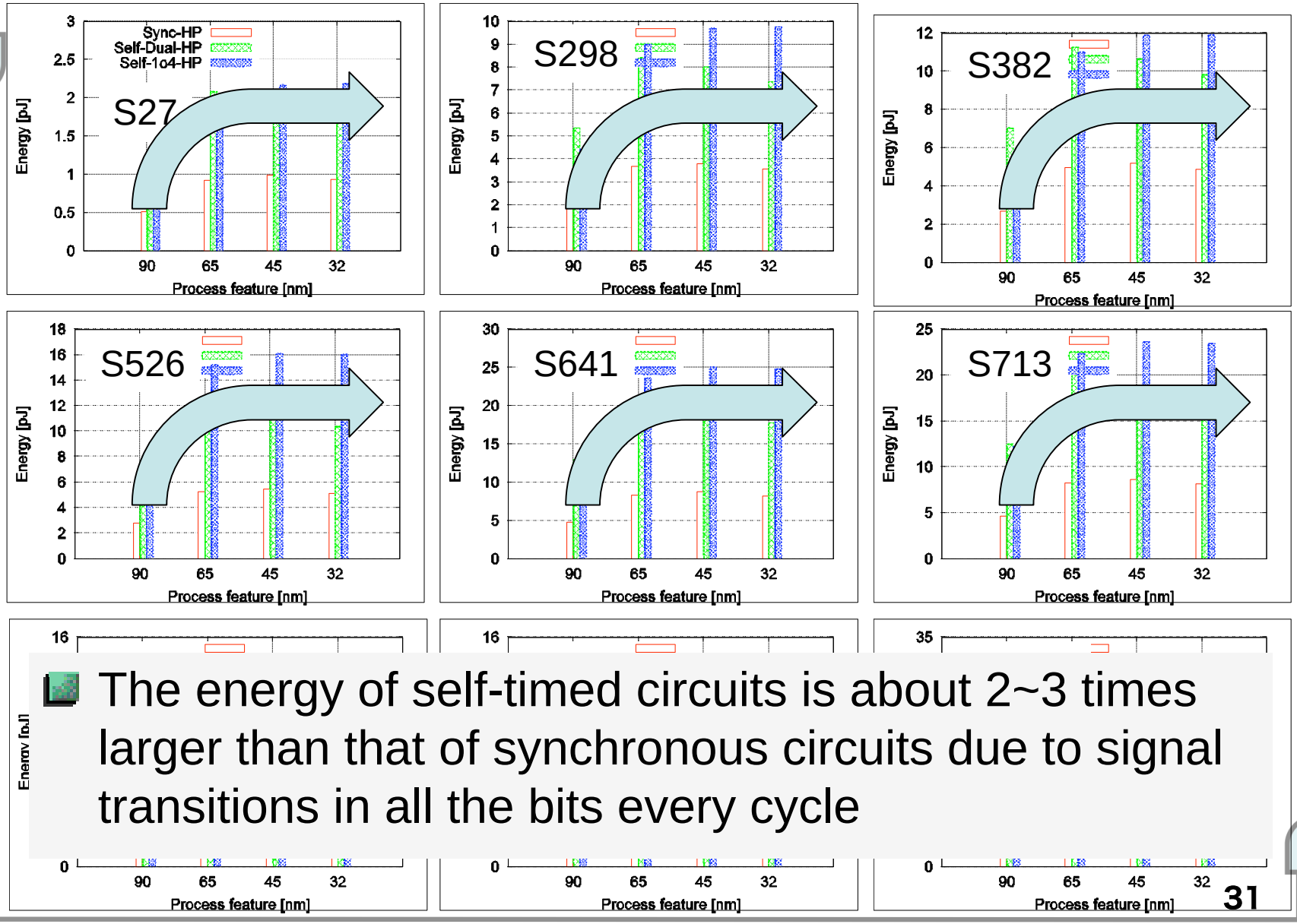






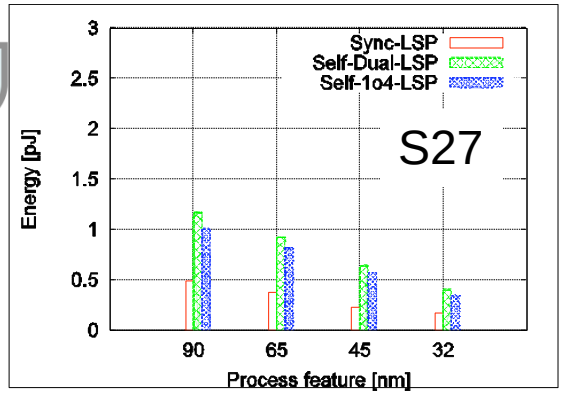


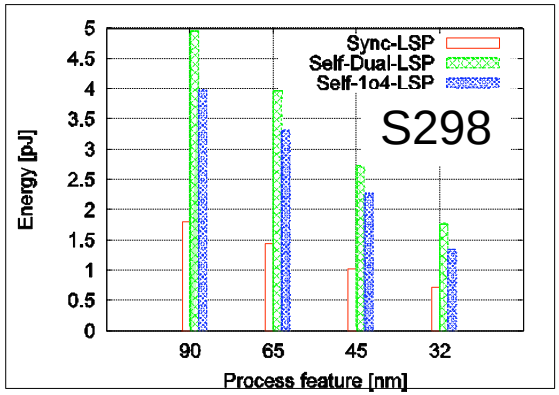
ISCAS89 energy comparison (HP)

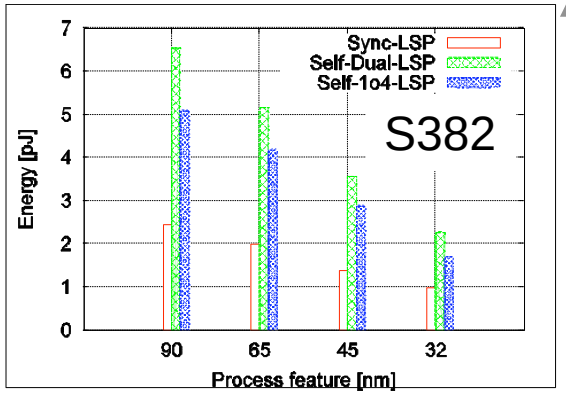


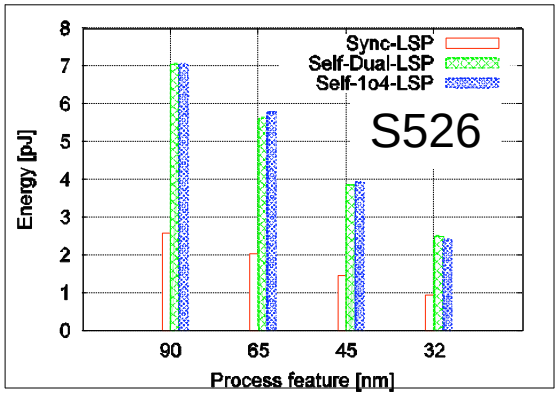
- The energy of self-timed circuits is about 2~3 times larger than that of synchronous circuits due to signal transitions in all the bits every cycle

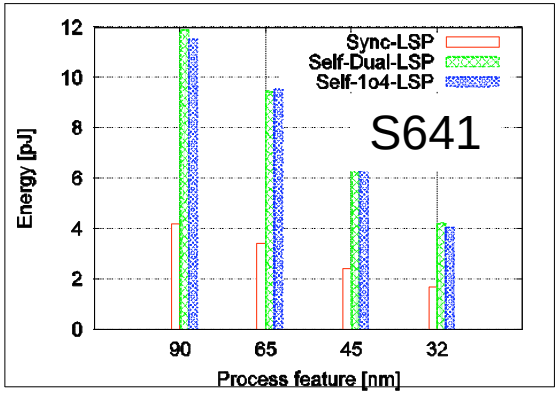
ISCAS89 energy comparison (LSP)

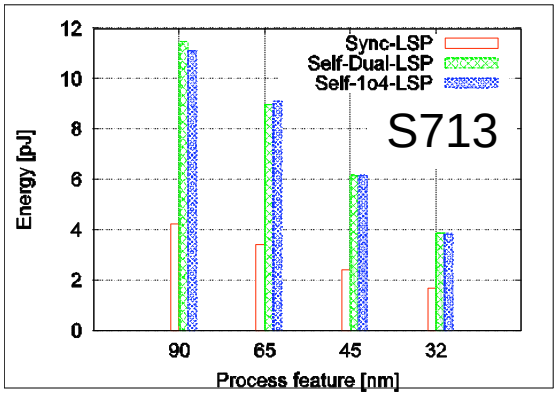


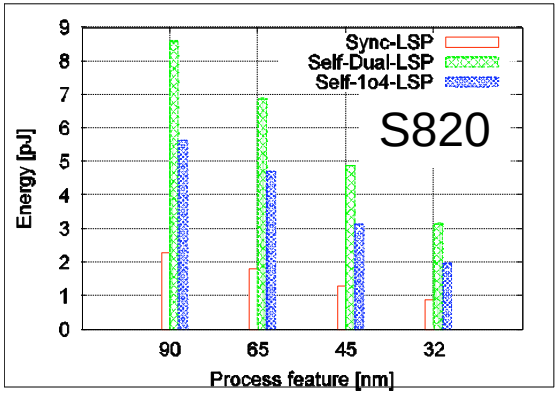


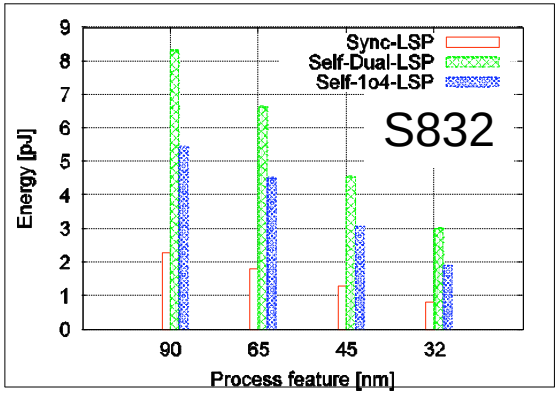


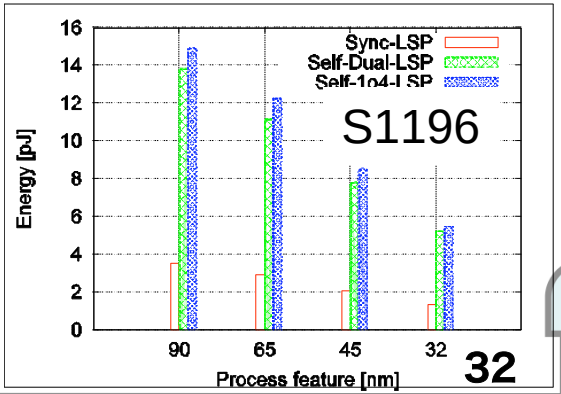




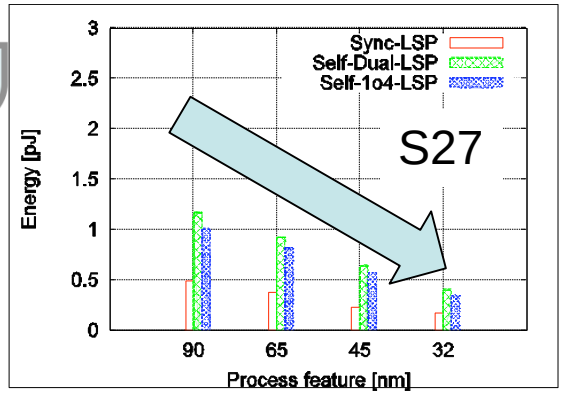


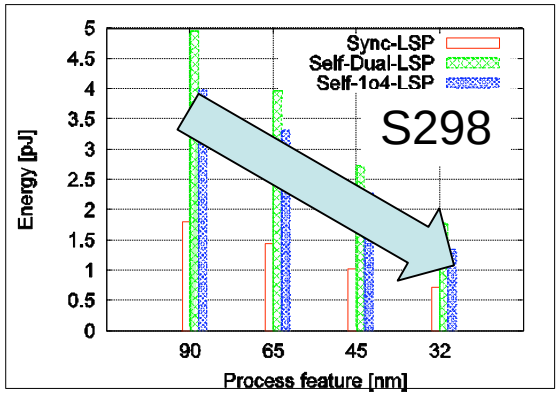


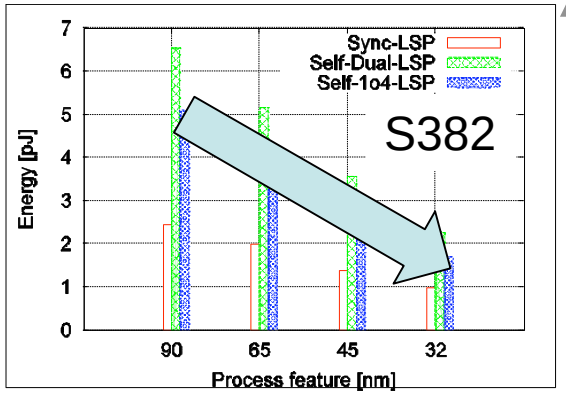


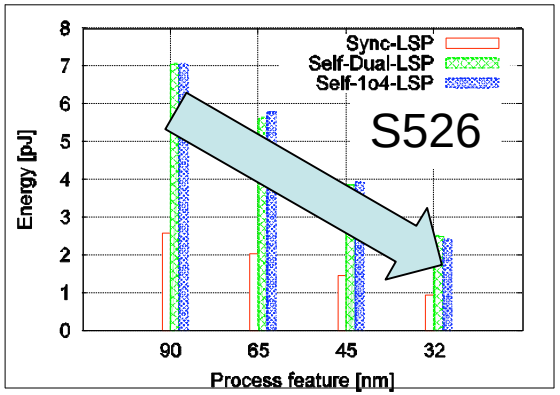


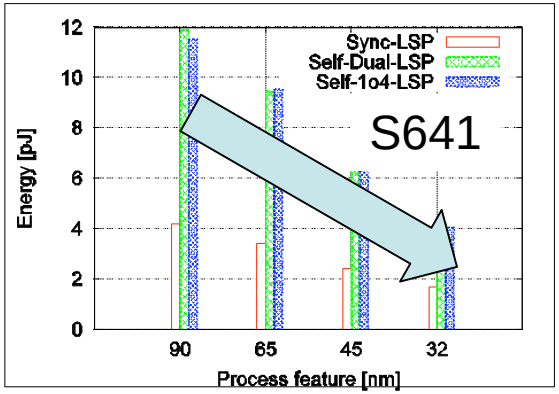
ISCAS89 energy comparison (LSP)

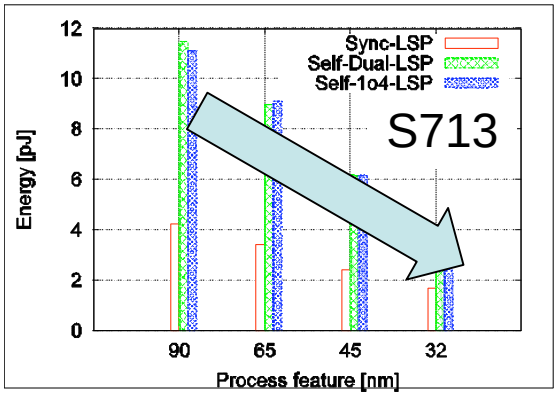


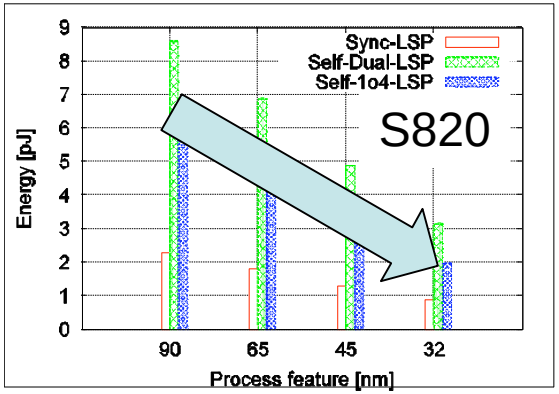


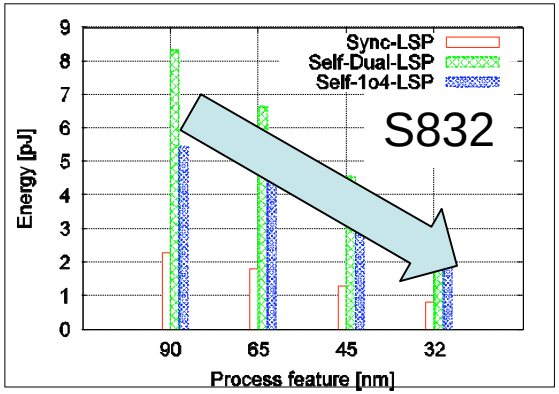


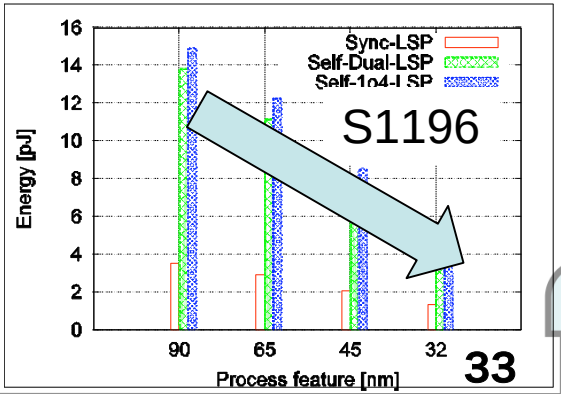




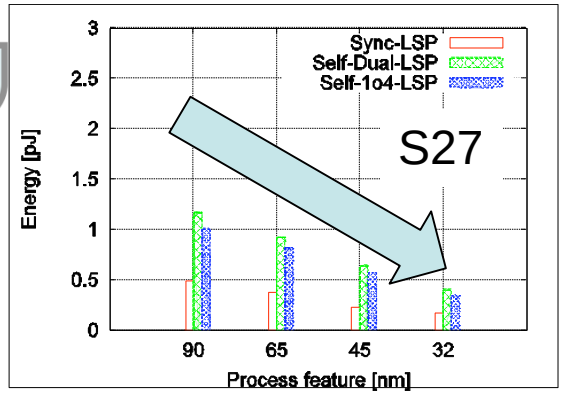


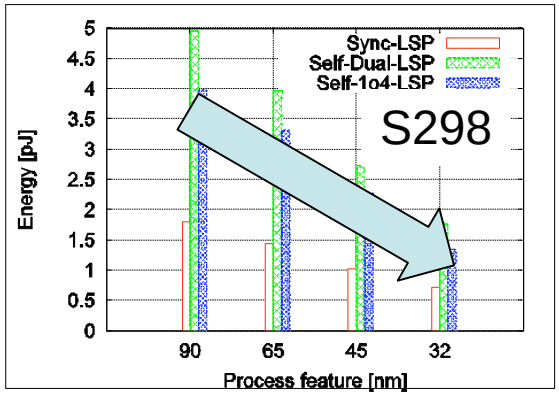


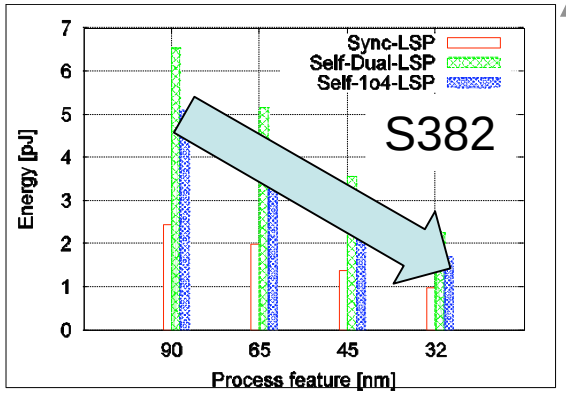


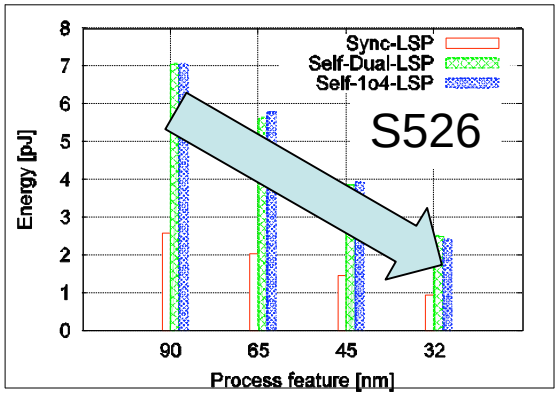


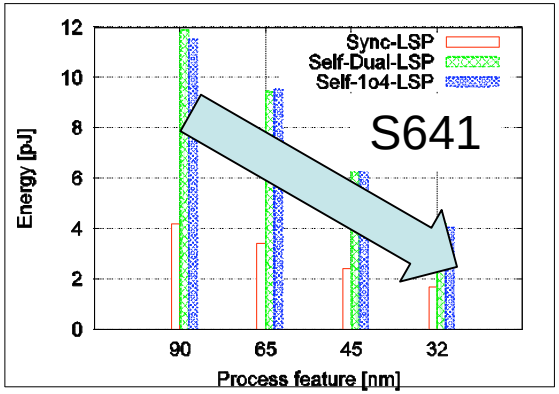
ISCAS89 energy comparison (LSP)

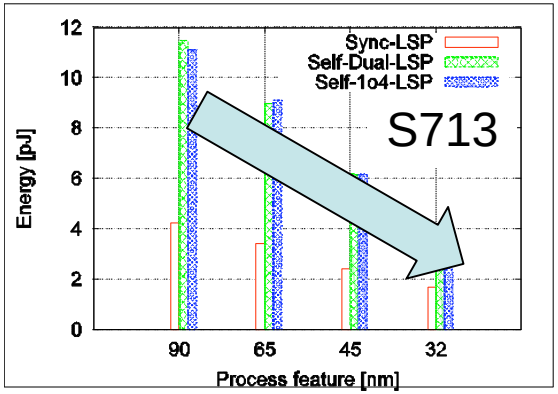


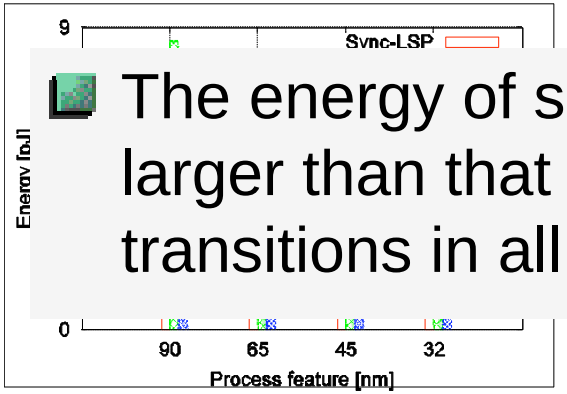


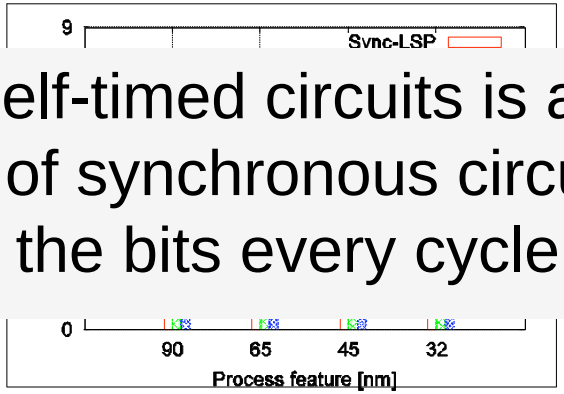


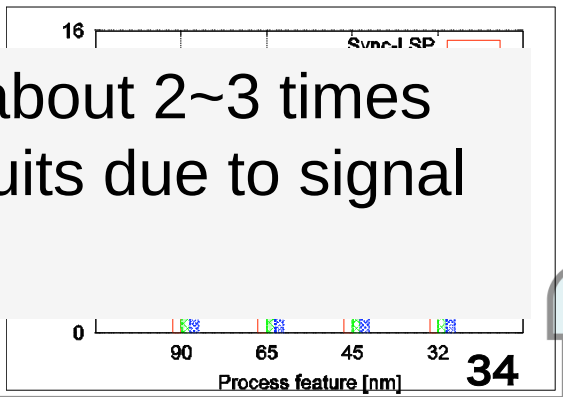












- The energy of self-timed circuits is about 2~3 times larger than that of synchronous circuits due to signal transitions in all the bits every cycle

Comprehensive comparison

- Average energy-delay product (ED) of self-timed circuits normalized by synchronous ED
  - 32bit adder, 32bit shifter, 14 ISCAS89 benchmark circuits

	90nm	65nm	45nm	32nm
HP	1.213	1.321	1.104	**0.869**
LSP	1.046	**0.951**	**0.685**	**0.360**

- Self-timed design styles are effective as the feature size decreases

Conclusion

- We have compared traditional synchronous circuits with self-timed circuits using the same standard cell libraries based on the Technology Roadmap of Semiconductors
- As the process feature size decreases, delay variations become large
  - Synchronous circuits are affected directly, resulting in slow circuits
  - The delays of self-timed circuits do not become so large since they depend on the average delay
- *Self-timed design styles are effective in the future technologies*

Thank you for your attention