Developing Fault Models for Nanowire Logic Circuits

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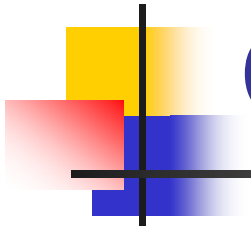
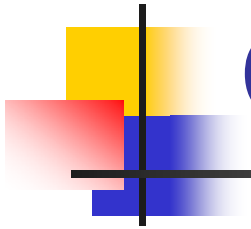


Outline

- Introduction
- NW-based logic circuits
- Fault models at device level
- Fault models at logic level
- Conclusions and challenges



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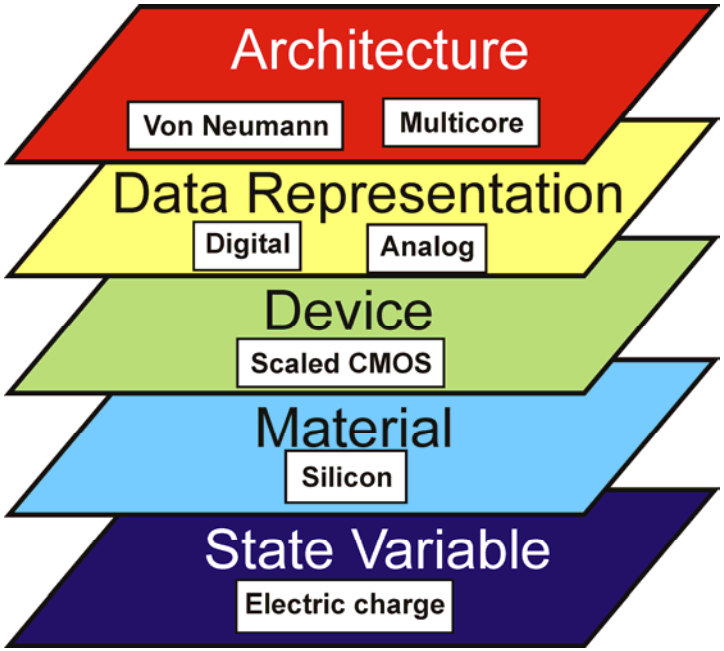
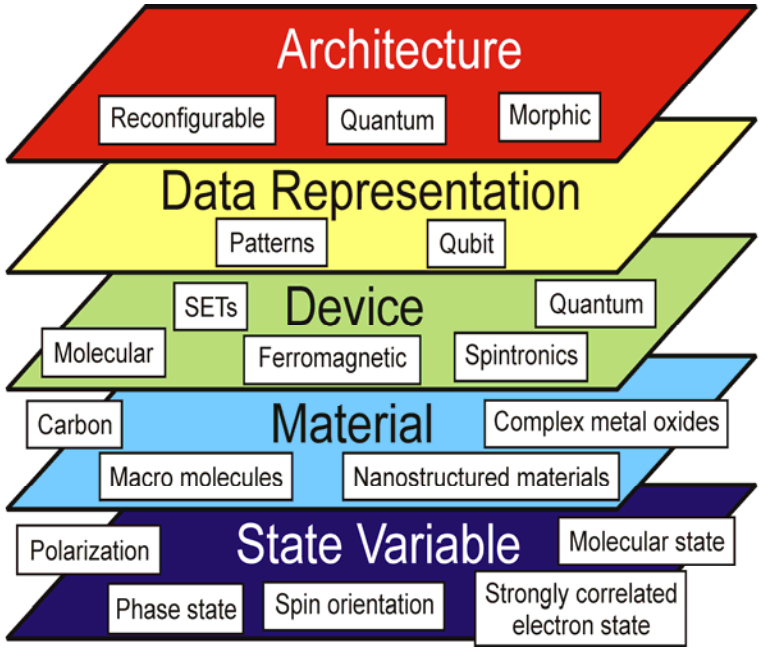
Emerging research information processing devices

Conventional scaled CMOS



New information process technologies



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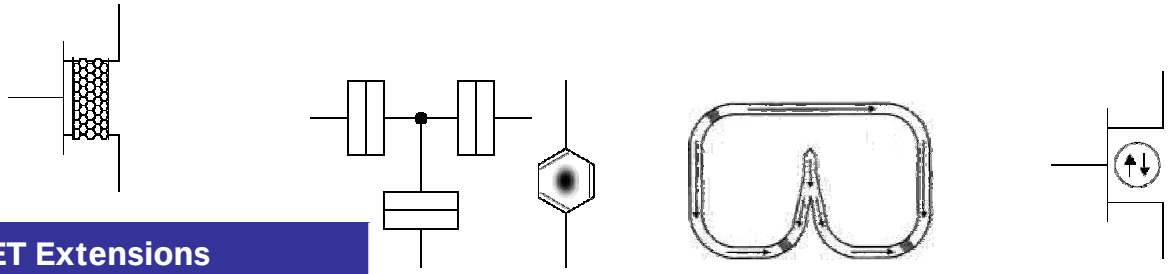
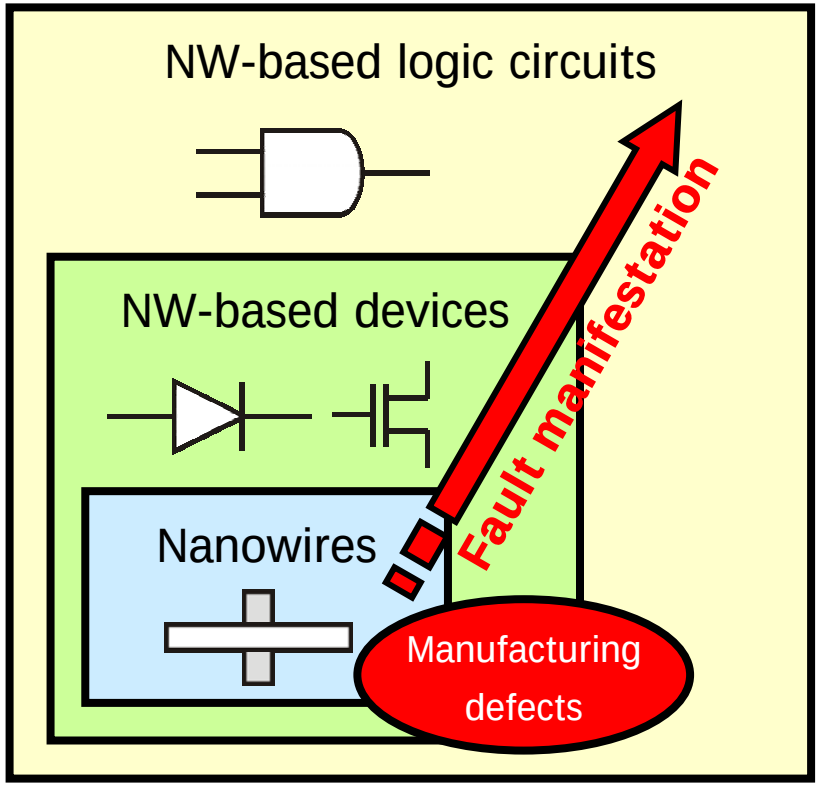
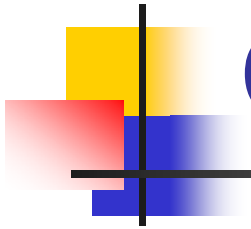


	FET Extensions					
Device	**1D structures**	**Channel replacement**	**SET**	**Molecular**	**Ferromagnetic logic**	**Spin transistor**
Typical examples	CNT FET NW FET NW hetero-structures Nanorribon transistors with graphene	III-IV compound semiconductor and Ge channel replacement	SET	Crossbar latch Molecular transistor Molecular QCA	Moving domain wall M: QCA	Spin Gain transistor Spin FET Spin Torque transistor
Research activity	379	62	91	244	32	122

Methodology





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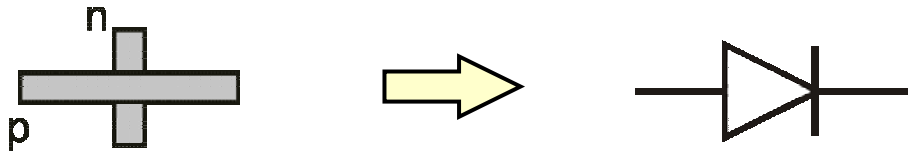
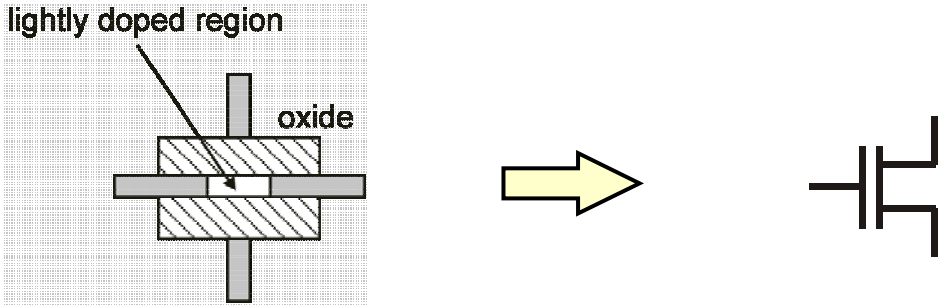
Electronic devices with NWs

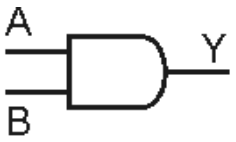
- Diode



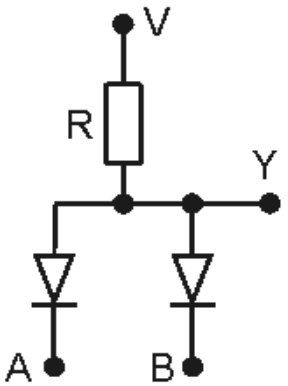
- NW-FET



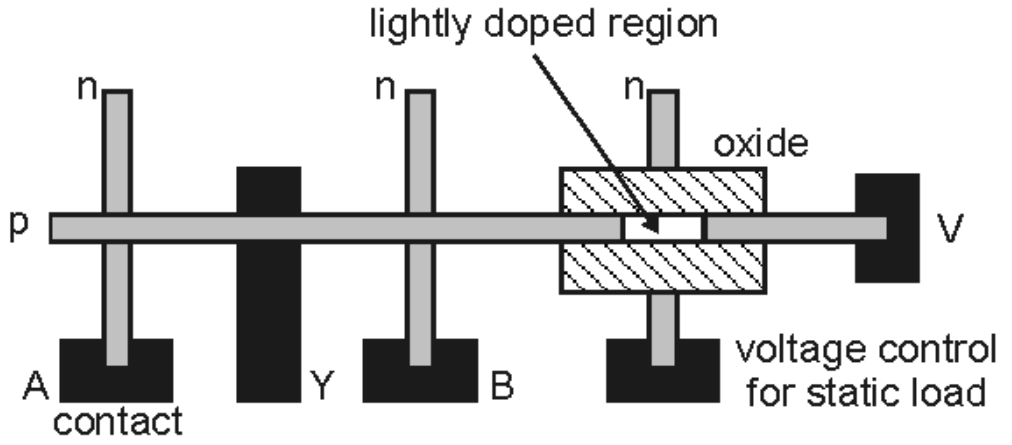
NW-based AND gate



(a) Logic symbol

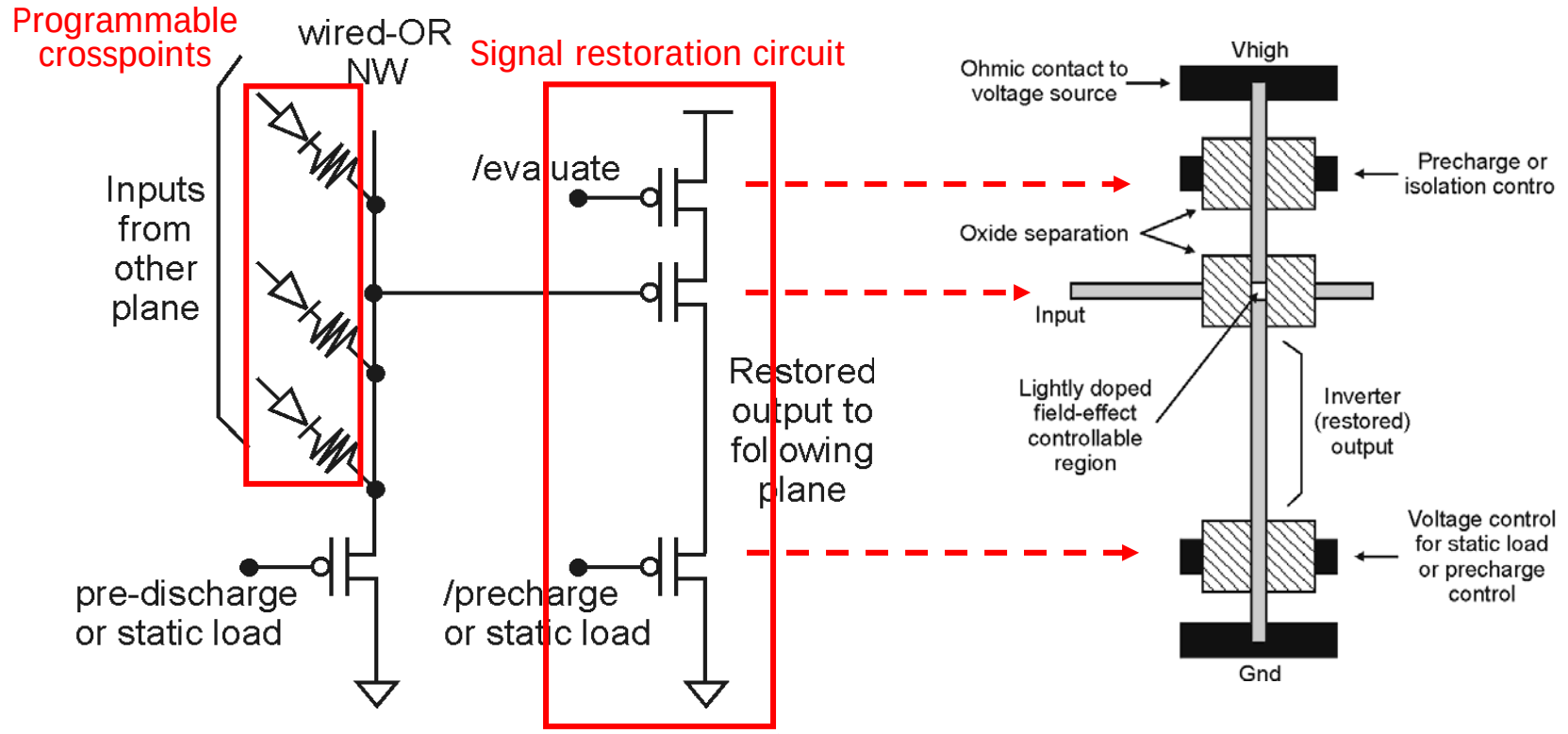


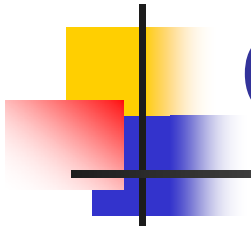
(b) Electronic circuit



(c) Two-dimensional crosspoint structure with nanowires

NW-based OR nanoPLA plane with signal restoration





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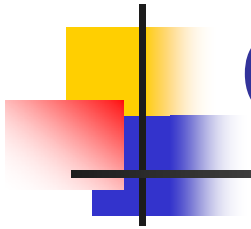
Manufacturing defects

Defect		Cause / Mechanism	Effect
Nanowire defects	Broken	Mechanical stress during assembly	Open I/O connections, p-n junctions or FET channel
	Poor contacts	Statistical number of atomic scale bounds	Increase of wire resistance
	Doping variation	Statistical doping	Variation of wire resistance
Crosspoint defects	Open	Statistical junction formation with tens of molecules	Open in diodes or NWFETs Non-programmable crosspoints
	Short		Short in diodes and NWFETs Shorted crosspoints
Bridging of adjacent nanowires		Imperfect planar NW alignment Variations in core shell thickness	Shorts between I/O connections or device terminals

Fault models at device level (manufacturing defects)

Causes and mechanisms (manufacturing defects)		Fault models at device level		
		Diodes	FETs	I/O connections
Nanowire defects	Broken wires	open	open	open
	Poor contacts	delay	delay	delay
	Doping variation	delay	delay	delay
Crosspoint defects	Open crosspoint	open/missing*	open	-
	Short crosspoint	short/extra**	short	-
Bridging of adjacent nanowires	Imperfect alignment	short	short	short
	Shell thickness variations	short	short	short

* In programmable circuits: missing devices due to permanent off crosspoints
** In programmable circuits: extra devices due to permanent on crosspoints



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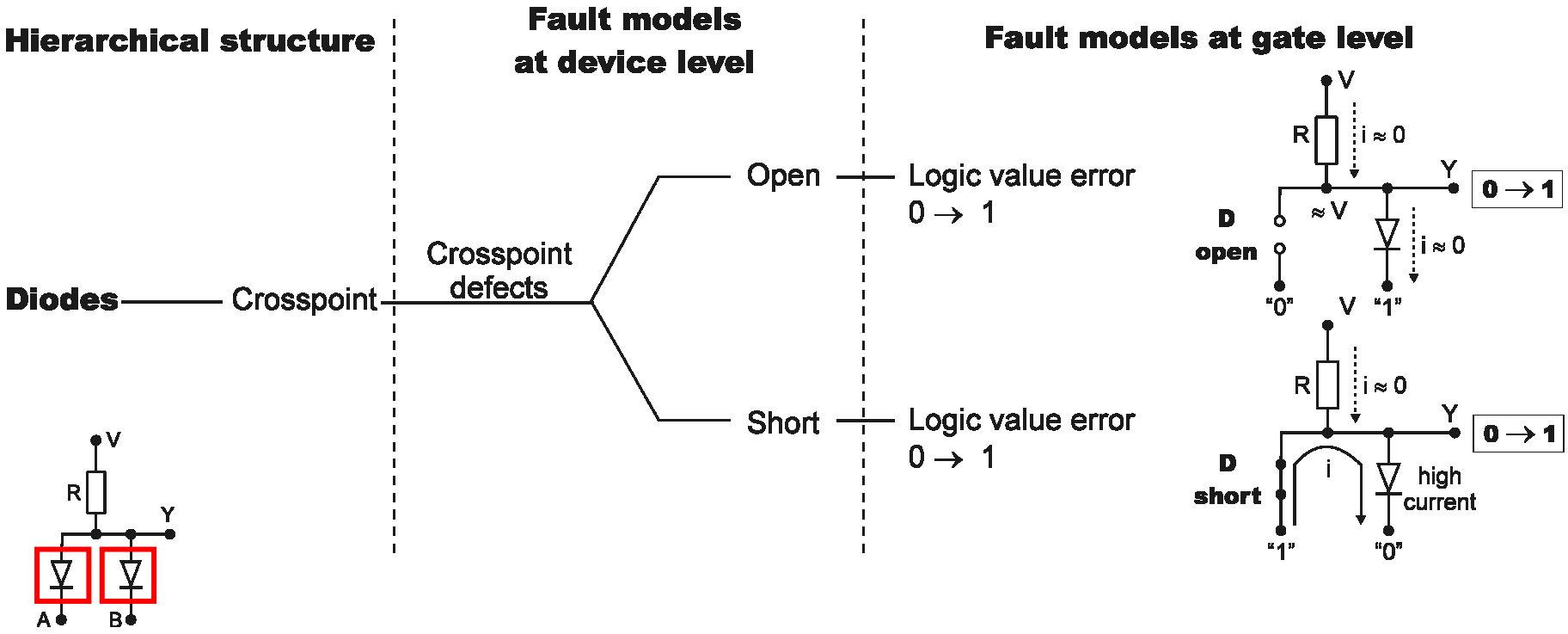
Fault models at logic level

- Hierarchical structure
  - *Logic circuit* made of *devices* made of *NWs*
- Single faults
  - For each *device* in the structure →
    - For each *fault model* at device level →
      - Analyse the fault propagation to the circuit's output

Fault models at logic level
Example 1: AND gate



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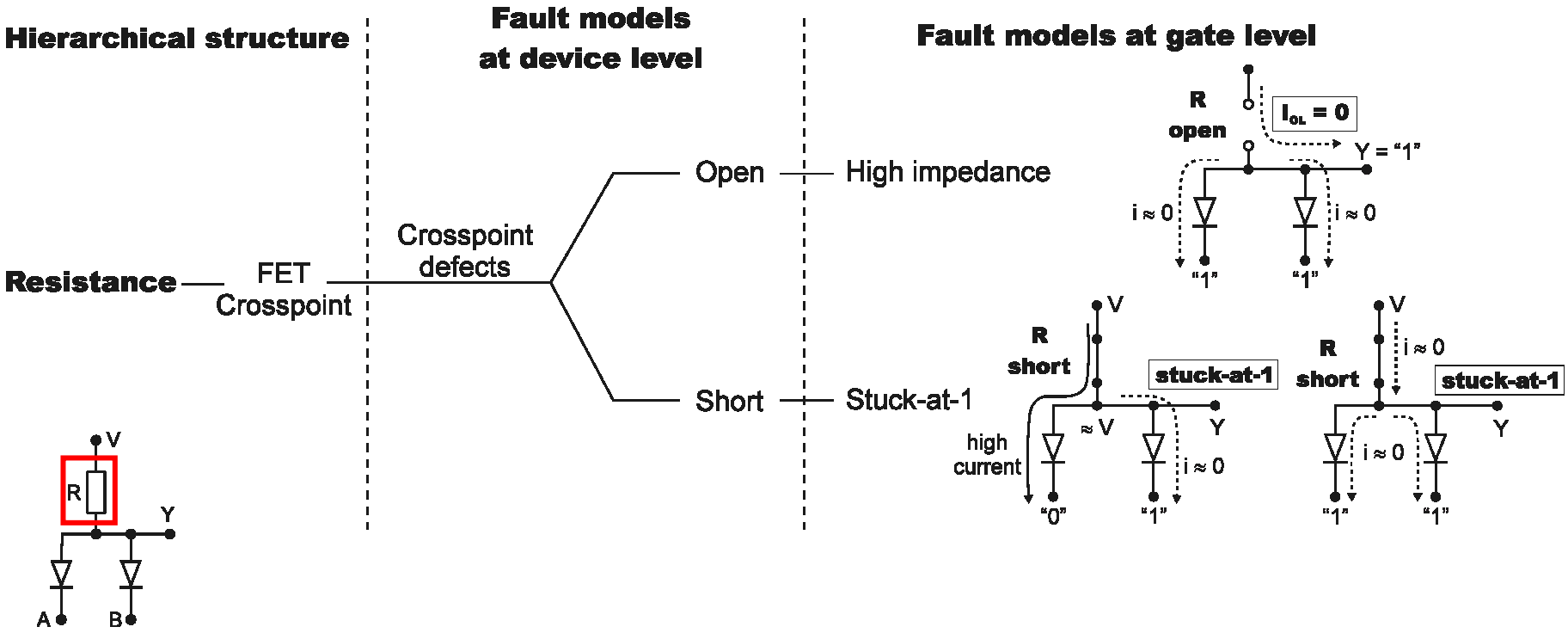

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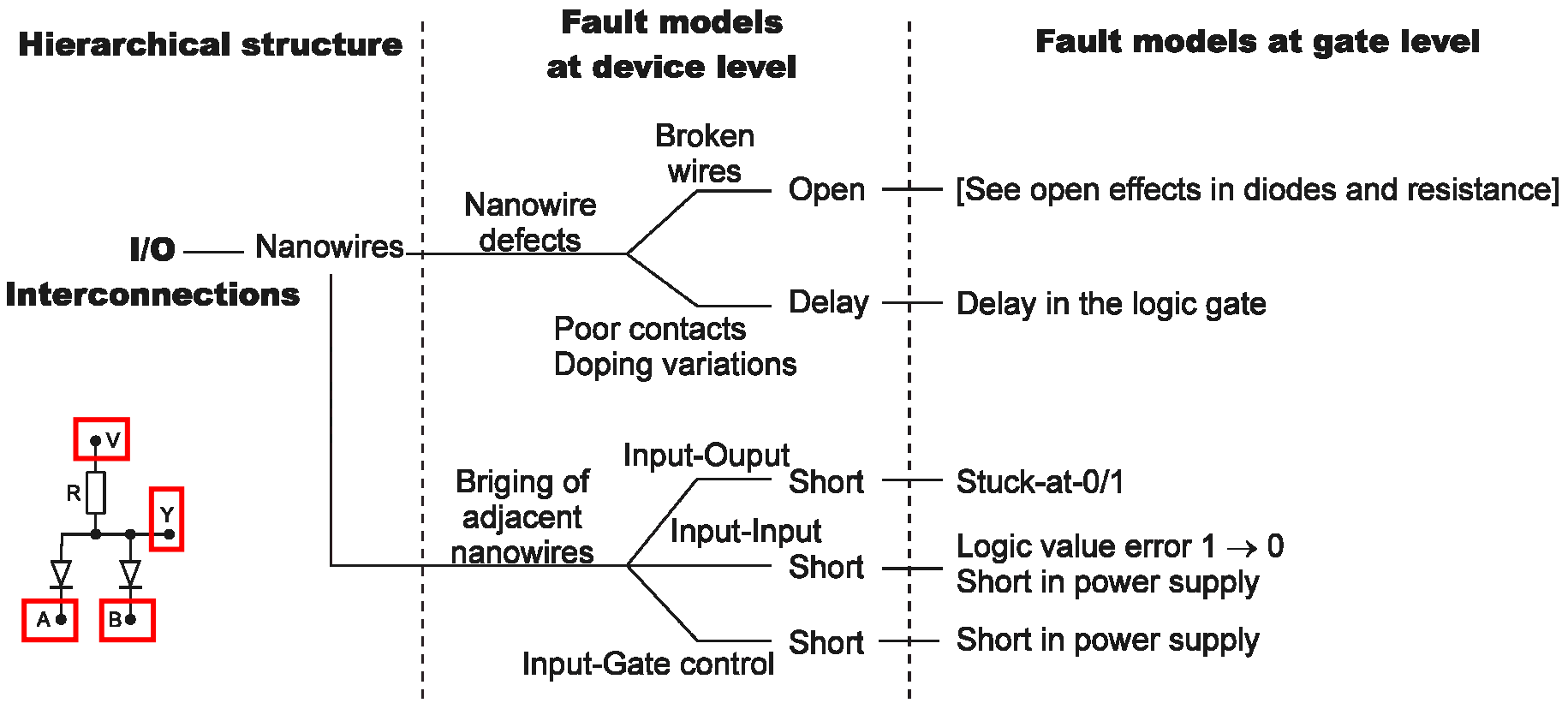
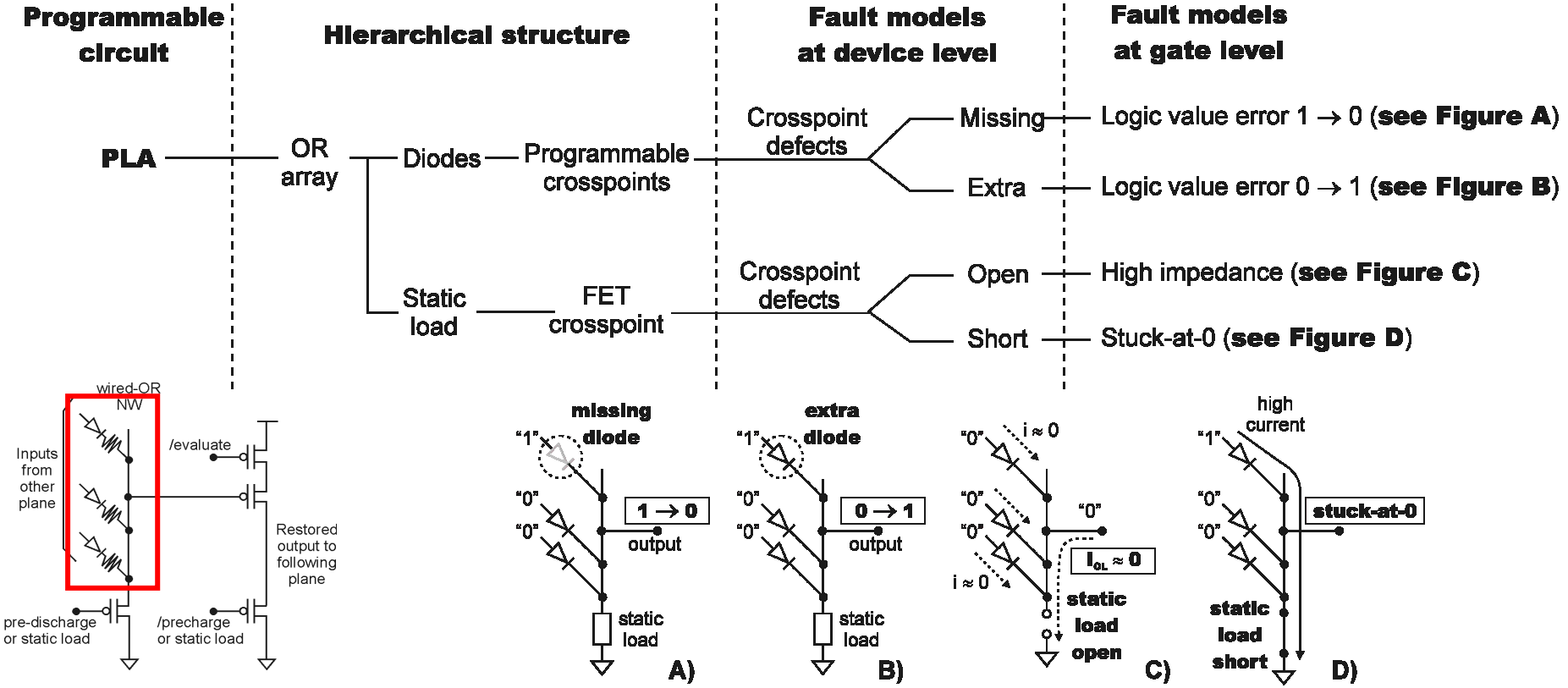


Fault models at logic level
Example 2: Programmable circuits



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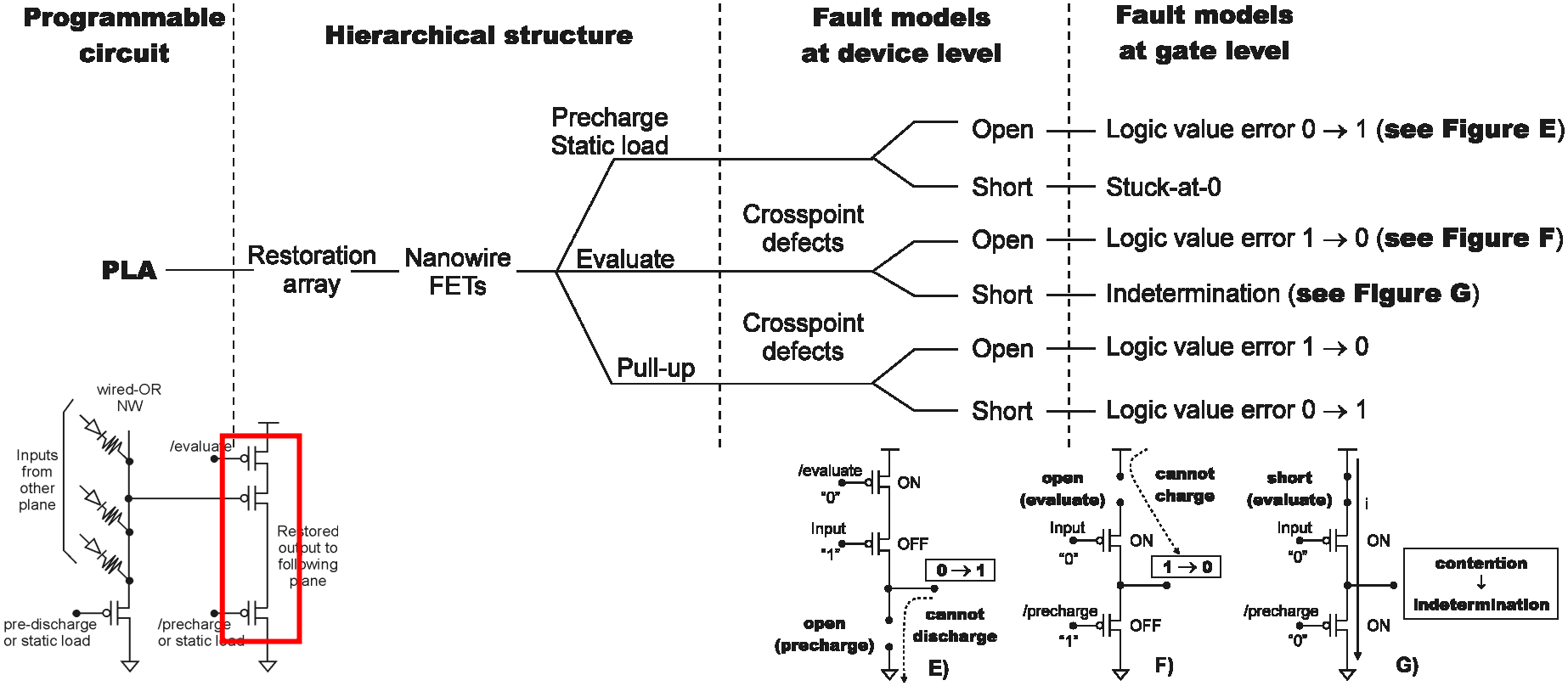

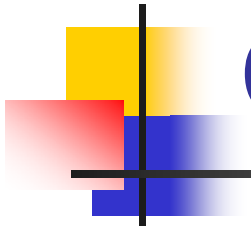

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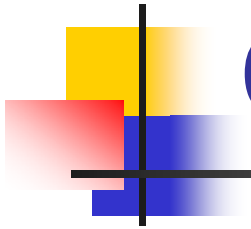
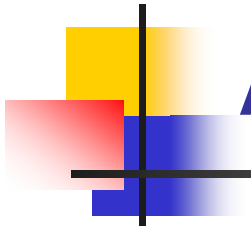
Conclusions

- Definition of fault models for nanowire-based logic circuits
- Bottom-up methodology
  - Physical → Device → Logic
- The methodology can be applied to other nanodevices and architectures



Challenges

- Modelling a wider set of faults
  - Wearout faults
  - Transient faults
  - Multiple faults
- Fault models for other nanodevices
  - CNT, molecular, spintronics, ...
- Dependability assessment of emerging (fault/defect tolerant) nanoarchitectures



Any question?

Thank you for paying attention!

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