Workshop on Dependable and Secure Nanocomputing - Preface

Jean Arlat
LAAS-CNRS & Université de Toulouse
7, Avenue du Colonel Roche
31077 Toulouse Cedex 04 – France
jean.arlat@laas.fr

Ravishankar K. Iyer
Coordinated Science Laborator
1308 West Main Street
Urbana, IL 61801 – USA
iyer@crhc.uiuc.edu

Michael Nicolaïdis
TIMA & iRoc Technologies
46, Avenue Felix Viallet
38031 Grenoble – France
michael.nicolaidis@imag.fr

The continuous progress in hardware technologies makes it possible to foresee a realm of unprecedented performance levels and innovative application-driven architectural designs. Nevertheless, the trends in nanoscale technologies raise serious challenges with respect to both dependability and security perspectives.

Accordingly, the Workshop is aimed at characterizing the various impairments including physical disturbances and malicious threats, as well as identifying design approaches and operation control paradigms that need to be enforced and/or favored in order to maintain dependable and secure computing. Three main goals are at stake:

- Reviewing the state-of-knowledge in emerging nanoscale technologies.
- Identifying suitable solutions attached to various design options for mitigating faults and attacks.
- Fostering new trends for combining various skills aimed at developing novel and more efficient solutions.

To tackle these multiple aims, a comprehensive program has been planned that is featuring varied forms of contributions: invited talks, submitted papers, a panel, as well as poster presentations.

The session that starts the Workshop is meant to set up the scene in identifying and coping with various kinds of threats: from dealing with an increasingly large number of defective devices to managing security vulnerabilities and malicious faults. We are pleased to announce the contribution of two distinguished ***invited speakers*** to address these issues:

- Janak H. Patel, *University of Illinois at Urbana-Champaign, USA.*
- Jean-Jacques Quisquater, *Université Catholique de Louvain, Belgium*.

The feedback received from the community to the call for contributions was excellent: 14 papers were submitted, originating from seven countries. Each of these submissions has been reviewed by at least three members the Program Committee. Thanks to their dedicated efforts, the evaluation process led to the selection of eight contributions. These ***selected papers*** constitute the program for the second session of the Workshop and are included hereafter. They cover a comprehensive set of topics ranging from environmental conditions and power-induced disturbances to architectural issues for on-line self-test and chip-level configuration. The authors of the other submissions were offered the opportunity to present a poster and to provide a summary of their contributions. The ***posters*** will be displayed during the breaks and these summaries are also included hereafter.

The afternoon session is devoted to a ***Panel on Emerging Hardware Technologies and Related Dependability & Security Challenges***. It is meant to identify trends in hardware technologies and foresee the related challenges from the dependability and security viewpoints, as well as forecast solutions to address them. The panel gathers experienced contributors that will provide diverse perspectives to the topic addressed. They are:

Moderator:

Johan Karlsson, *Chalmers University, Göteborg, Sweden.*

Panelists:

- Jacob A. Abraham, *University of Texas, Austin, USA.*
- Helena Handschuh, *Spansion EMEA, Levallois-Perret, France.*
- Takashi Nanya, *University of Tokyo, Japan.*
- Alex Orailoglu, *University of California, San Diego, USA.*

We sincerely hope that you will enjoy the Workshop and actively participate by interacting with the various contributors. We also very much welcome your comments and hints for future plans of this event. Further information is available at the Workshop website (http://www.laas.fr/WDSN07) and will be updated after the Workshop.