Design and Test Techniques for Better Defect Screening and Improved Reliability in Automotive Integrated Circuits

Udayakumar H. and Rubin A. Parekhji
Texas Instruments, Bangalore, India.
Email: [uday,parekhji]@ti.com

Automotive Requirements

Electronics in automotive systems must meet stringent test and reliability requirements. This is due to a variety of reasons:

- Automotive systems are highly safety critical.
- Automotive sub-system components are used in larger control systems, e.g. for on-board telematics, engine control, cruise control, etc. Often there is no scope of replacing individual components therein. As a result, entire systems may have to be replaced.
- The lifetime of automotive systems is high. Not only does the design and development of the sub-systems take a couple of years, their deployment, usage and overall lifetime extends to several more years thereafter.

The associated cost of replacement in each of the above cases is, therefore, prohibitively high, and implications on the system manufacturer potentially severe, especially since the feasibility of replacement of faulty components may be low, and may also require several preventive measures to be taken, leading to further implications.

Impact on Design and Test

These applications, therefore, drive the need for very high test quality at manufacturing time, as well as very high reliability during normal operation. Integrated circuits used in automotive electronics correspondingly have several differentiating requirements for manufacturing test, field testability and field reliability. They impact the design and test practices in a few ways:

- Additional DFT requirements for better fault coverage.
- DFT architecture changes for tolerance to observed errors and adopting corrective measures.
- More conditions for normal / stress mode tests.
- Additional design margins for tolerance to defects and variability.
- Additional screening of silicon at manufacturing time for better identification of outlier devices which fail marginally or under certain conditions, and methods to classify them as good or bad devices.

SOC Design and Test Considerations

The implications of the above methods are well-known. However, they become even more critical when large high performance SOCs (system-on-chips), designed in deep sub-micron technologies, are being used in automotive electronics. This is due to the following reasons:

- The traditional measures of test cost quality based on standard fault models are no longer adequate. Test escapes in defective parts per million (DPPM) must now be accurately estimated based on the actual defect coverage and correlation of the effectiveness of various tests on the targeted coverage. These numbers must be then compared with the actual number of field returns through additional analysis. (As a representative example, automotive devices set DPPM goals in single digits; even “zero”).
- The cost of test for such SOCs is significantly higher, and an even larger component of the overall device cost. This is due to both a larger number of tests, higher test time, and also a larger number of test insertions.
- Design and test optimizations through better DFT and pattern merge optimizations become more critical now to contain the test cost, and target the required quality at an acceptable cost, or maximize the quality for a given cost.
- The stringent design and test requirements adversely impact the yield. Design for manufacturability (DFM) and design for yield (DFY) techniques correspondingly become even more important. (It is understood that neither DFM nor DFY techniques guarantee lower DPPM; however, the contrasting requirements of low DPPM and high yield make them important).
- The ability to perform accurate failure analysis (FA) through physical design and tool based ATPG techniques becomes even more important, since the results of FA drive further investigation into fails and defect screening mechanisms. This requirement is also crucial for the system designer / manufacturer since corrective measures which have to be adopted outside the device must also be applied to the system under development at the earliest.

Design and Test Techniques

- Memory testing including run-time programmable algorithms, functional BIST, use of error detection / correction logic, and built-in self-repair for field recovery.
- At-speed testing including coverage of interacting / non-interacting logic between multiple clock domains, and path delay ATPG or small delay defect ATPG for a large number of near critical paths across different modules.
- Defect coverage including defect based ATPG, logic BIST for unmodelled faults, N-detect coverage, and detection of static and dynamic bridges.
- Stress testing including parallel testing of multiple modules, reduced margin testing for lesser tolerance, high speed bus operation, high speed burn-in, device internal self-test and loop-back modes, and stress monitoring.
- Electrical and physical design including managing NBTI threat to reliability, robust clock tree design, reducing critical path sensitivity, reducing fabrication process sensitivity, package design and bond pad placement, and power plane partitioning for Iddq tests.
- Application tests including evaluation of functional tests in normal configurations, and generation of functional tests triggering worst case operating conditions.
- Analysis including statistical post-processing of test application data for outliers, IR drop and power analysis for normal and stress test modes, and data collection from on-chip parametric modules.