Nanoelectronic Architectures: Reliable Computation on Defective Devices

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Nanoelectronics is increasingly poised to occupy an important role in providing solutions to surmount obstacles imposed by Moore's Law in semiconductor electronics [1]. While the fundamental issues may remain largely intact, nanoelectronics imposes significant quantitative changes resulting in qualitative modifications to the way we design; paramount among them are an increase in fabric size, density and fault rates which result in (i) increased emphasis on parallelism, (ii) strict constraints on localized interconnection, (iii) regularity in nanofabrics, and (iv) repair of faulty circuits, offline and possibly online.

Perhaps, the most fundamental challenge to be overcome in constructing any nanoelectronics based systems is the high unreliability of nanoelectronic devices which manifests mainly in two forms. First, manufacturing defects increase significantly, due to the defect prone fabrication process in nano environments needed to pro-duce the small scale devices with a bottom-up self-assembly process. The defect rates of nanoelectronic systems are projected to be many orders higher than the current CMOS systems. Second, not only is high occurrence of transient faults expected during run-time, but so is a high variance in the fault rate and a clustered behavior of faults. These are essentially caused by the nano-scale size of the de-vices as well as the low voltage utilized, which result in extremely high sensitivity to environmental influences, such as temperature, cosmic ray particles and background noise.

The emerging new challenges of nanoelectronics result in a reevaluation of the components typically utilized, and the approaches usually undertaken in generating designs. Particularly, how does one map design descriptions to such regular nanofabrics with massive defects? How does one make the design defecttolerant, particularly in the face of significant defect occurrence rates and constrained test access? How does one develop efficient fault tolerance techniques to address the dynamically occurring faults with clustering behavior, and time varying rates without exhaustively exploiting the abundant hardware facilitated by the nanoelectronics? How does one ensure reliability without sacrificing performance?

The new characteristics of nanoelectronics impact fault tolerance approaches in distinct ways: 1) severe constraints on the fault tolerance approaches; examples of relevant solutions that address topological issues in defect/fault tolerant nanoelectronic systems can be found in [6, 7]; 2) the opportunity to develop efficient fault tolerance schemes, such as the reconfigurability and multi-valued logic support exhibited by the nanoelectronic devices; relevant research approaches exploiting such characteristics include [5, 2].

Furthermore, due to the difference in complexity at the various system hierarchical levels, appropriate fault tolerance schemes vary. At the logic gate level, defect/fault tolerance is tightly coupled with the mapping of logic functions to the underlying cross-bar based regular structure [7]. For arithmetic components such as adders, fault tolerance schemes need to target the specific component structure [2, 5]. At the processor level, new computational models need to be developed, which focus on the tradeoff between hardware, performance and reliability, under particular topological constraints imposed by the nanoelectronic environment [4, 3, 8, 6].

The new realm of nanotechnology imposes manifold challenges on attaining fault resilience. The practical applicability of nanoelectronic solutions necessitates that the dramatic overhead for achieving reliability somehow be moderated. The application requirements necessitate that any such techniques continue to ensure that the highest levels of resilience be indeed attained. And the regularity and adaptivity requirements necessitate that the fault tolerance techniques fit topological constraints to ensure viability within the expected constraints of nanofabrics. Research addressing the aforementioned challenges will span multiple design hierarchical levels, and will eventually lead to an understanding as to how to construct high performance, reliable nanoelectronics based systems in the face of defect and fault occurrences.

References

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