Dependability in Conventional and Emerging Nanosystems

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Summary

Integrated circuit technology has continued to advance following Moore's law, shrinking features to nanoscale dimensions. Projections are that the technology can continue to scale to produce billions of transistors on a chip using Silicon technology, with minimum feature sizes on the order of 10 nm.

These advances are being made in spite of the fact that the circuit features are smaller than the wavelength of light being used in the lithographic process.

In contrast with the mask-based lithographic techniques being used for conventional transistors, techniques are being developed in the laboratory to produce nanostructures using self-assembly with features on the order of 1 nm or less. Technologies being studied include carbon nanotubes, quantum wells and DNA structures.

Both directions have potential problems with defects:

1) The conventional approach is resulting in increasing amounts of variability in the transistors, leading to potential errors in the results. In addition, increases in physical defects are expected. Defective memory cells in high-density memories are being corrected today through the use of spare rows and columns.
2) The self-assembly techniques will result in defects and mis-alignments in the assembly process.

These trends underscore the need to develop techniques for dealing with the defects and non-idealities in the manufacturing process.

However, it is particularly important to realize that many techniques for dealing with faults and errors have been developed over many decades, and that many of them will be applicable to the emerging technologies. This foundation will provide the basis for new techniques for ensuring dependable nanosystems.