Judicious choice of waveform parameters and accurate estimation of critical charge for logic SER

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Abstract

In this paper, we discuss various important factors during critical charge estimation of a logic block. We present results on how does the choice of input pulse - its shape and its duration affect the critical charge estimation. We also present first report on the impact of undershoots induced because of the particle strike in the struck transistor and transistors affected by the induced transient. It is shown that such undershoots can transiently alter the inference of device properties and may even lead to erroneous critical charge results. Finally, we present first results on how does the choice of input waveforms and device age (affected because of NBTI) alters the vulnerability ranking of different node within the same logic block, making it challenging for the designer to choose the top few critical nodes to harden.

1 Introduction

With the minimum geometry fabricated on an integrated circuit constantly decreasing, to entitle higher densities, vulnerability to soft errors and single event upsets has become a serious concern. Soft errors are typically caused when a circuit node collects electrons (or holes) created by a incident energetic particle, such as alpha particle, neutrons or other heavy ions [1], [2]. Depending on various factors, the particle strike may cause no observable effect, a transient disruption of circuit operation, an erroneous logic state - "upset" or in some cases, even permanent damage to the device or the circuit. As a consequence, advanced characterization and mitigation techniques are required in order to assure chip reliability from soft errors. An important measure of the soft error rate (SER) sensitivity of the node is it's critical charge (Qcrit), which is the minimum amount of charge that needs to be injected in a circuit node to produce a soft error.

Traditional methods of Qcrit evaluation employ iterative injection of a current pulse at a circuit node to figure out the magnitude of pulse when it *just* flips, either the node itself (as in a bit-cell), or the content of the latch. It has been previously reported that high energy particle strike typically leads to current pulses with varying pulse widths, and also that Qcrit of the node is a strong function of the waveform, [3], [4]. In this report, we present a detailed study of how the critical charge of the node varies with the shape and width of current pulse. We show that the critical charge of the node saturates both at very small and very large pulse widths. Additionally, we also assess the impact of undershoots and overshoots produced when simulating circuits with such small pulses. The study helps designers to identify a prudent current waveform to harden their logic block for a given stress condition.

Furthermore, we also present the results on how does the NBTI induced aging of the pMOS device over time, will affect the critical charge of the node. Our results indicate that the critical charge of the node gets worse, if we consider the aging of pMOS.

Finally, traditional way of designing logic blocks hardened against SER is to estimate critical charge of several nodes and try to harden most vulnerable nodes (nodes with smallest Qcrit). Hence, the relative merit of nodes is more important to designer, rather than their absolute values. We report that above factors play crucial role in ranking the nodes in order of criticality and a different choice of input parameters will lead to a different criticality order, making it challenging for the designer to identify key nodes to harden.

The simulation methodology is described in the next section. The basic phenomenon of single-event upset is revisited briefly followed by the results on how does waveform shape/widths affect the critical charge, along with the discussion on the undershoots. Impact of aging on the critical charge is discussed in subsequent section and the paper is concluded with discussion on how above parameters alter the criticality ranking of nodes.

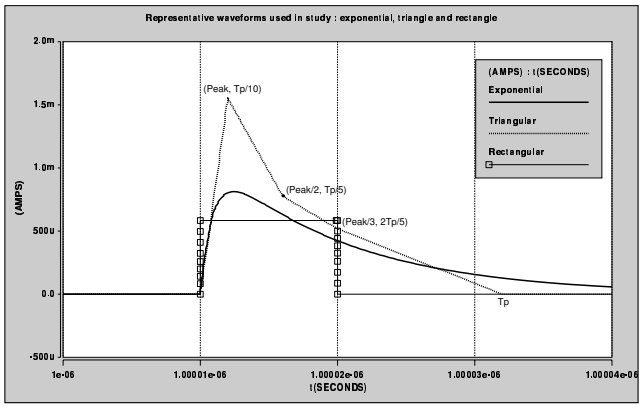

Figure 1. Representative waveforms used in present study

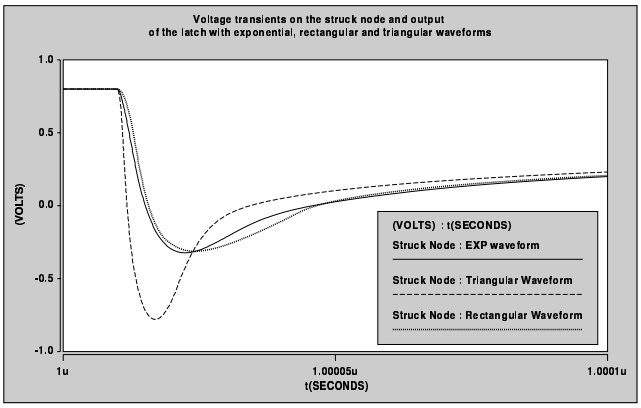

Figure 2. Undershoots with exponential and triangular current source models

2 Simulation Methodology

Proper choice of input waveform for critical charge estimation is important, since the current transients are closely coupled with the voltage transients. Hence, choosing a waveform also inherently means deciding on the resulting voltage waveforms. One way of estimating critical charge on the nodes is through doing coupled device-circuit simulation (mixed mode), wherein the generation of electron-hole pairs is simulated in the device and its impact is translated electrically through circuit simulations. This, however, is computationally expensive and is usually not practical to be run on design libraries. Another related approach is to take the currents waveforms directly from the TCAD simulations of a discrete transistor and inject it back into SPICE. This procedure, however, becomes unpractical to iterate, and is also associated with the limitation of not capturing the circuit changes which happen during the particle strike.

Consequently, designers have often resorted to modeling the particle induced transients through current pulse shapes, [1]. The commonly used waveforms includes triangle, rectangle and exponential shapes with chosen rise and fall times to denote the contribution from drift and diffusion charge collection processes, as shown in Fig. 1.

For the present study, we have used the exponential current source model, rectangular current source model and triangular current source model to evaluate their impact on the node critical charge. The triangular waveform is designed to be controlled through the time period - the rise time, half-peak and the fall time are all a function of time period. Once the time period of the waveform is fixed, the peak of the waveform can be scaled till the point the event results into the flip at the latch. Identical iterations are done with a rectangular waveform of given width. The exponential waveform is as described in Equation 1:

$$I_{exp} = \frac{Q_{tot}}{\tau_f - \tau_r} * (exp(-\frac{t}{\tau_f}) - exp(-\frac{t}{\tau_r})) \qquad (1)$$

where τ_r and τ_f denote the rise time and fall time respectively. Herein, the total charge (Q_{tot}) is varied till the upset occurs.

3 Impact of waveform shapes and undershoot on critical charge estimation

A representative flop from 65nm technology was chosen to assess the impact of waveform shape on the critical charge estimation. The results from hit with different waveforms are as shown in Fig. 2. The sharp fall time of the triangular current waveform causes the struck node to collect all the charge immediately, with a little circuit response coming into action. As can be seen from Fig. 2, the drain voltage lowers immediately because of the large surge in charge collection at the junction, following the particle strike. The drain voltage still lowers further, resulting in an under-shoot.

This undershoot gets inferred as a transient body bias by the SPICE, which lowers its threshold for a small period. Considering that the initial logic on the node (drain) was high, the large undershoot on the node will indeed assist the

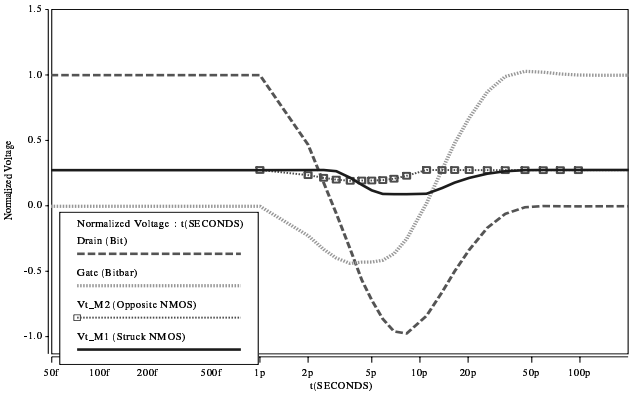

Figure 3. Undershoots and transient threshold voltage shift seen in transistors of bit-cell through circuit simulations

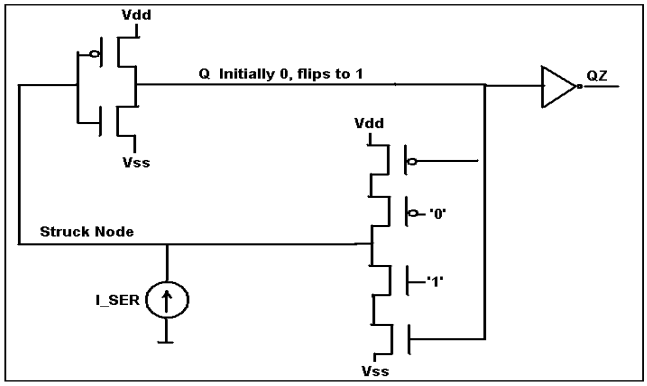

Figure 4. Partial schematic for circuit in static configuration before upset, used to study impact of pulse width and circuit response time. Q flips from 0 to 1

transistor to turn 'ON' quickly. The analogy becomes more clear in a bit-cell (Fig. 3), where the struck node sees an undershoot. Because the 'source' of the transistor is tied to the 'body' at 0V, the drain voltage going negative is equivalent to the application of transient body bias on the transistor. It can be seen that this effect indeed leads to lowering of the threshold voltage of the transistor. It can also be seen that the gate of the struck transistor also lowers (due to capacitive coupling). Above study confirms that use of waveforms with small fall times induces undershoots and associated non-physical changes in the device properties. We see small undershoots with rectangular and exponential waveforms.

It is important to note here that these undershoots are different from what has earlier been reported in literature as a results of 2-D or 3-D device simulations [6]. The physical phenomenon occurring at device level, during the particle strike, is a reversal in the polarity of source current, attributed to the barrier lowering. Roche *et al.* have reported the positive component of the source current in [7] using 3-D simulations, where they attribute its origin to the collection of the electrons at the source junction, enhanced because of the reduced ability of the drain to collect anymore charge. However, what we see here with SPICE is kind of a simulation artifact, induced because of very sharp transient and small fall time, [8]. One can do an elaborate study of these undershoots to figure out how much do they erroneously contribute in critical charge. The study indicates the importance of avoiding undershoots while estimating critical charge through SPICE based circuit simulations. We have seen that small rectangular pulses, often leads to such undershoots, and hence, should be avoided during Qcrit estimation.

4 Impact of pulse widths : circuit response time

It has been reported in the literature that a high energy particle strike is usually associated with generation of transients, which have variability in the pulse widths, [4]. Hence, it becomes important for the designer to assess the critical charge of the node given this variability.

In order to study the impact of pulse width on the critical charge, we chose the flop in a static configuration (with data initially at logic low, and clock and clockz etc set accordingly), as shown in Fig. 4. As can be inferred from the schematic that the flop is currently in a vulnerable state, where-in the strike at the node mentioned may lead to a logic flip. Further, we have chosen rectangular waveforms for this study as the results from rectangular waveforms are readily de-convolved with other effects.

The impact of the pulse widths is shown in Fig. 5. As can be distinctly seen, the critical charge of the node is a strong function of the pulse width. Further, it is saturating, both at lower and higher pulse widths. The critical charge is defined here, in traditional fashion, as the area under the current waveform, till the time at which the output of the latch flips irrecoverably, [6]. This time has been denoted as the flipping time, t_{Flip}.

We know that typically, the critical charge of the node can be approximated by following formulation, [9] :

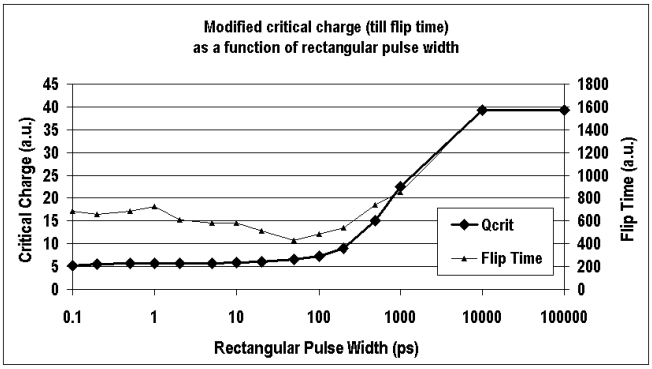

Figure 5. Saturation in critical charge at very small and large rectangular pulse widths

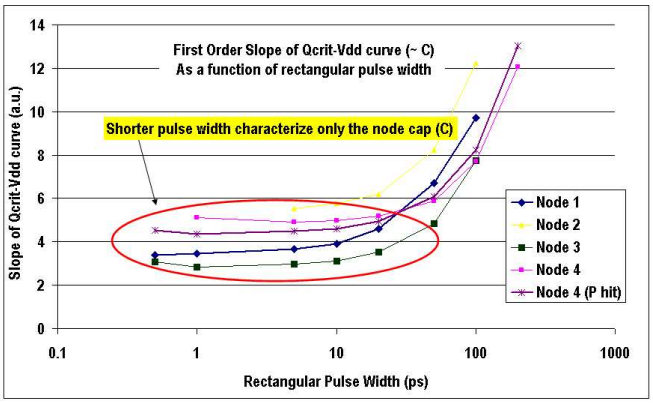

Figure 6. First order slope of Qcrit vs Vdd for different nodes and different pulse widths

$$Q_{crit} = C_{node} * V + I_{restore} * t_{Flip} \quad (2)$$

where C is the nodal capacitance and $I_{restore}$ is the recovery current supplied to the node by the restoring transistor (pMOS in 0 to 1 flip and nMOS in 1 to 0 flip). Above observations can be explained with the understanding that at very small widths, we are not able to sensitize the recovery transistor and it is only nodal capacitance which comes into play. As the pulse width increases, we start seeing recovery current from pMOS and also the circuit response comes into the play, increasing the critical charge. However, beyond a particular width, the charge deposited is sufficient to overcome the recovery (and the associate circuit response) and the node eventually flips. This causes a saturation in the critical charge at very high pulse widths.

Above premise is further validated through Fig. 6, wherein the first order slope of Qcrit vs Vdd is plotted for different nodes for several pulse widths. As can be seen, the slope remains constant for smaller pulse widths, as the slope essentially means node capacitance for smaller pulse widths.

Typically, the short width pulses arise when the particle strike is directly on the drain terminal of the transistor. When the transistor is OFF (gate at logic low and drain at logic high), high drain-bulk electric fields exist and a particle strike at such a junction leads to immediate charge collection through drift transport. On the other hand, if the particle strikes at junctions with lower electric fields, the charge collection is much slower and elongated, leading to wider pulse widths. While studies indicate that as much as 90% of particle strikes are non-drain, [3], it is crucial for designer to understand the impact of short and wide width current pulses. Above study helps to give a bounding estimate of the critical charge for the node, given the variability in the widths of the transient current pulse.

5 Impact of aging

There has been a recent escalation in the interest of designers in Negative Bias Temperature Instability (NBTI), which is seen as one of primary front-end reliability challenges, [10]. NBTI degrades the performance of pMOS transistor over time, degradation being a strong function of the applied gate voltage, application temperature and the ON-time of the device. While designers have long been taking into account the impact of NBTI in timing closure, its impact on the soft error rate reliability is not yet well understood. Single-event sensitivity of a circuit depends on the transistor drives and timings, which in turn are dependent on the threshold voltage and mobilities. It follows that the SEU sensitivity of a circuit should depend strongly on the "aging" of the transistor. Previous works have demonstrated the dependence of SEU sensitivity on transistor aging due to total dose radiation [11]. In this section, we will present our understanding of how does the aging of pMOS transistor will affect the critical charge of the node.

There are sophisticated tools available to assess the aging of the device, under representative operating conditions. One of them is a BERT based tool, [12], which works on an input stimulus and the expected lifetime of the device. The output is a degraded device model, which can be used for further performance analysis of the circuit at the end-of-life

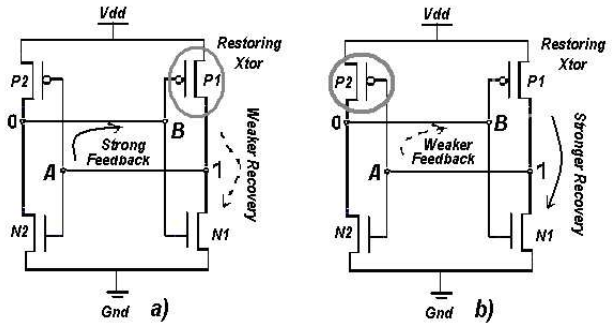

Figure 7. Understanding impact of aging on bit-cell

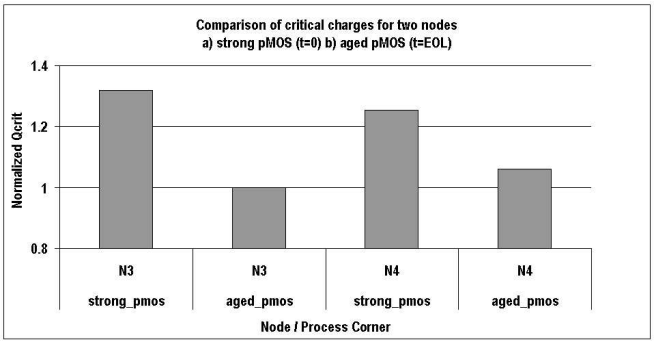

Figure 8. Variation in critical charge after considering device degradation

(EOL). For the present study, we have used the EOL model for Qcrit evaluation.

The basic mechanism for an upset and the impact due to aging is best understood through a bit-cell (Fig. 7). The flip in a bit cell is strongly dependent on two factors: a) feedback, provided by the cross coupling inverter and b) recovery, provided by the restoring pMOS transistor. A bit-cell, storing logic 1 at node A for most of the lifetime will have pMOS P1 degraded the most (Fig. 7a). Invariably, the single-event induced current flowing through the struck device is limited by the drive of the restoring transistor. At EOL, pMOS P1 will only be able to provide a weaker restoring current, while the feedback through the coupling inverter is as strong as it was at time zero. It is now easy to see in logic blocks that the pMOS, which provides the recovery current in Equation 2, weakens due to aging and hence, the Qcrit of the node invariably goes down. This is substantiated by the results from one of the logic blocks, as seen in Fig. 8. The critical charges for the nodes becomes lesser at EOL.

It is interesting to note from Equation 2 that critical charge contributions of the node from nodal capacitance and restoring current can be de-convolved to further assess the impact of aging. This can be easily done by characterizing the critical charge at several widths, with the understanding that the at lower pulse widths, the entire contribution is from nodal capacitance. As future work, we plan to evaluate how the results from Fig. 5 change with the aging.

6 Re-ordering of critical nodes

While the absolute value of the critical charge may not be directly important to the designer, it is the relative strength of the nodes which is a key care-about. Typically, the designer may run Qcrit estimation flow on all the nodes of the logic block and may come up with a ranked list of node, in order of their criticality to strengthen. It, hence, becomes important to assess the impact of waveforms shapes, widths and aging on the relative ranking of nodes in order of critical charge.

Fig. 9 shows a comparison of three nodes : N3, N4 and N5 (as shown in the schematic Fig. 10), how their critical charge vary with the choice of input waveform. The different exponential waveforms used for this study are as described in Fig. 9 and in Equation 1. The rise times and fall times are respectively shown (in order) on the X-axis mark against the critical charge for each node. Triangular and rectangular waveform gets characterized only by the time period (the shape being the same as in Fig. 1. It is readily inferred that N5 has the smallest critical charge computed with most of the waveforms, thereby making it a 'critical' node, which needs to be hardened. However, there are instances of waveforms with which N3 and N4 also becomes 'critical' (with triangular 10 and rectangular 10 pulse width waveform for example).

We believe that such difference in result comes basically from Equation 2, where a given input waveform may not have been able to initiate device response. Additionally, it can also be inferred from Fig. 8 that nodes N1 and N2 interchange their criticality order with the change in the aging of the pMOS. We hence see that the ranking list changes significantly with different choices of input waveform shape, width and the device age.

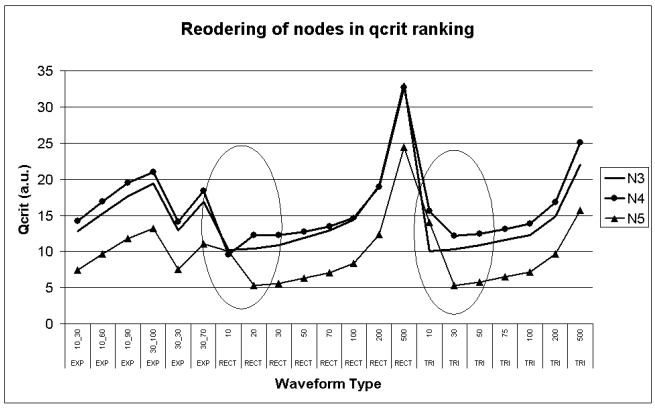

Figure 9. Re-ordering of nodes in order of criticality

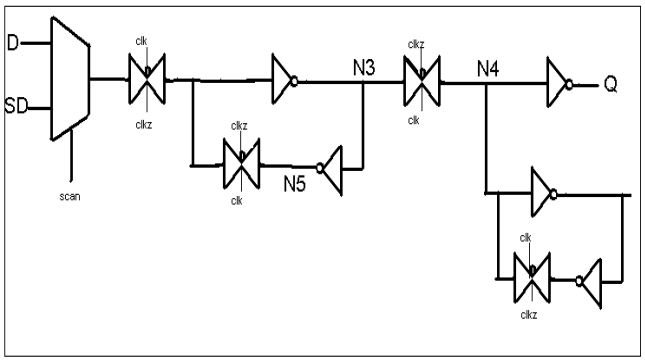

Figure 10. Schematic of the logic block with nodes N3, N4 and N5

7 Conclusion

An elaborate analysis of several key factors affecting the critical charge estimation of a logic block was presented in this paper. We discussed how the choice of input pulse - its shape and its duration affect the critical charge estimation. We also presented results on the impact of undershoot induced because of the particle strike in the struck transistor and transistors affected by the induced transient. An understanding of how does the NBTI induced aging affects the SER reliability of the block was also presented. does the choice of input parameters alters the criticality ranking of nodes.

Finally study provides a way for designers to rank order the logic blocks, based on their Qcrit result. We show that the rank-order is a function of pulse width, and hence, this makes distribution of the pulse width an essential parameter to such ranking.

References

[1] P. Dodd *et al.* "Basic Mechanisms and Modeling of Single-Event Upset in Digital Microelectronics", *IEEE TNS*, Vol. 50, No. 3, 2003, pp.583-602.

[2] R. Baumann, "The impact of technology scaling on soft error rate performance and limits to the efficacy of error correction", *2002 IEDM Proceedings*, pp.329-332

[3] Tino Heijmen *et al.*, "Factors that impact the critical charge of memory elements", *2006 IOLTS Proceedings*,pp.6

[4] Benedetto *et al.*, "Variation of Digital SET Pulse Widths and the Implications for Single Event Hardening of Advanced CMOS Processes", *IEEE TNS*, Vol. 52, No. 6,2005, pp.2114

[5] H. T. Weaver *et al.*, "RAM Cell Recovery Mechanism Following High-Energy Ion Strikes", *IEEE EDL*, Vol. 8, No. 1, 1987, pp.8-9.

[6] R. L. Woodruff *et al.*, "3-D Numerical Simulations of Single Event Upset of an SRAM Cell ", *IEEE TNS*, Vol. 40, No. 6, 1993, pp.1795-1803.

[7] Roche *et al.*, "SEU response of an entire SRAM cell", *IEEE TNS*, Vol. 45, No. 6,1998, pp.2534-43

[8] P. Hazucha *et al.*, "Measurements and analysis of SER-tolerant latch", *IEEE JSSC*, Vol. 39, No. 9, 2004, pp.1536-43

[9] P. Roche *et al.* "Determination of key parameters for SEU occurrence using 3-D full cell SRAM simulations", *IEEE TNS*, Vol. 46, No. 6, 1999, pp.1354

[10] V. Reddy, A. T. Krishnan *et al.*, " Impact of negative bias temperature instability on digital circuit reliability", *2004 IRPS Proceedings*.

[11] Axeness *et al.* "Single event upset in irradiated 16 K CMOS SRAMs", *IEEE TNS*, Vol. 35, No. 6, 1998, pp.1602

[12] Cadence White Paper, "Reliability Simulation in Integrated Circuit Design"