Manufacturing Process Variations and Dependability - A Contrarian View

Janak H. Patel
University of Illinois at Urbana-Champaign, USA
jhpatel@uiuc.edu

Semiconductor Trends

The focus of this talk is the discussion of future CMOS technology and its impact on dependability. Main stream CMOS devices are already in the nanotechnology dimensions and continue to shrink following Moore's law. A CMOS transistor in today's microprocessors has gate oxide thickness of about 6 atoms. As the scaling down of the physical dimensions of transistors continues, defect density, transient error rates and reliability become serious concerns. One can get some idea of defect density and reliability from *ITRS*, a public document. *The International Technology Roadmap for Semiconductors (ITRS)* is a document showing the main trends in the semiconductor industry spanning across 15 years into the future and is available at *www.itrs.net*. This document is the result of a consensus of semiconductor experts from Europe, Japan, Korea, Taiwan and United States. Using some of the ITRS data and other experimental data, this talk projects the impact of shrinking CMOS technology on hard faults, age related reliability, and transient errors from manufacturing variability. It concludes that there should be no concern for dependability with the scaling of CMOS.

Hard Faults

Semiconductor manufacturing processes may introduce permanent defects in a chip during one or more of hundreds of process steps. It is important that the testing be as thorough as possible to uncover defective chips before they are shipped out. Defect Density, defined as number of electrical defects/m^2 of wafer area is an important parameter in computing yield as well as test escapes. One must keep the defect density low for economics as well as quality. It so happens that the process engineers have managed to keep the defect density in microprocessors to about 1395 defects/m^2. For the next 15 years they continue to project the same defect density. A typical microprocessor silicon area remains about 500mm^2 for the next several years, but the number of transistors per chip doubles every 2 to 3 years. This means per transistor defect rate continues to decrease not increase! If test coverage of chips stays constant, we continue to get the same quality. For these reasons hard faults from manufacturing process is not a great concern for dependability.

Age Related Faults

Semiconductor chips have well known age related faults that manufacturers already account for in the design to achieve a specified life time of a chip. Some of the known effects are: Oxide breakdown, charge trapping in gate oxide, metal migration, thermal fluctuation related weakening of interconnect and dielectric. Semiconductor manufacturers can accurately model, analyze and experimentally measure the age dependent defects and compensate for these in the design rules. ITRS projects short term reliability goals of 50 to 2000 failed parts per million in the first year of operation of a chip (early failures due to latent defects) and the long term reliability goal of 10 to 100 FITS (failures in billion device-hours). This goal remains constant over time and since the number of transistors increase over time, failure rate per transistor must decrease over time!

Process Variations

Semiconductor manufacturing process involves many process steps and each is a source of some nonuniformity. For example, oxide thickness, doping density, diffusion depth, and sheet resistance affect a transistor's threshold voltage (V_T). It is estimated that V_T varies about 100% across a modern chip. Since V_T affects transistor switching delay, logic delays across the chip vary a great deal. This results in varying speed chips from the same wafer. The variance in operational speed of chips is a concern from dependability. What if the test for speed is not perfect passes a slow chip as fast? If only very infrequent logic operations need the fast paths in a chip then the chip will operate correctly most of the time except on rare occasions. The result may seem like a transient error even if it is repeatable in theory. In practice, such an error is not easily reproduced since the exact electrical and thermal environment may not be repeatable. This error is however not inevitable. Recall that it is less a consequence of unknown process variations, than an imperfect timing test. Process variations must be kept under control for a predictable device, and manufacturers will strive for that. By simply improving the test quality one can reduce timing errors. As we move forward in time, it is clear that CMOS technology will remain as robust and dependable as has been in the past and there is no concern for future.