Nanoelectronic Architectures: Reliable Computation on Defective Devices

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Scaling beyond CMOS

Moore's law – exponential scaling down of transistors

- State-of-the-art device: Si based CMOS
  - Provided several decades of scaling: ~ 45nm currently
  - Expected to continue for the next several years: – beyond 22nm
  - Asymptotic end around year 2019: – approaching 6nm
- Physical limits of CMOS
  - Quantum mechanics, fabrication limitations, …

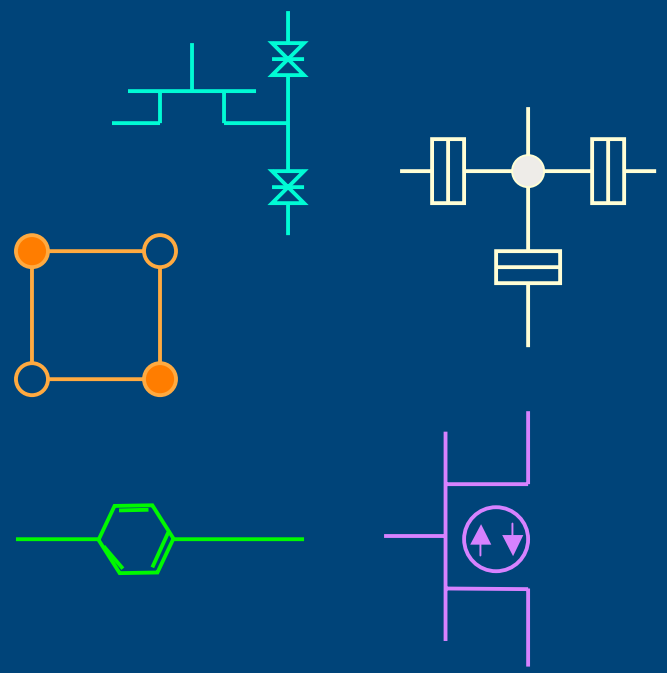
Substantially extending the roadmap beyond CMOS:

- **New nano scale materials, devices**
  - **Near term: heterogeneous integration with CMOS**
  - **Long term: nano architectures**

Nanoelectronic device candidates

- *Micro*electronic devices → *nano*electronic devices
  - New means of processing / representing / storing information
  - Nano system innovations

- Emerging technologies
  - Carbon Nanotube (CNT)
  - Resonant Tunneling Devices (RTD)
  - Single Electron Transistor (SET)
  - Quantum Cellular Automata (QCA)
  - Molecular Electronics (Molecular)
  - Spin transistor (Spin)



- Promising device candidates
  - ✓ Logic & Memory

Nano devices: fundamental differences

- ***Different means of physical basis***
  - ***Info storage mechanism:***
    - Capacitor charge, interlocked state of logic gate vs. charge on floating gate, gate insulator, magnetization, etc
  - ***State variables:***
    - Voltage level vs. molecular state, spin orientation, phase state, etc
  - ***Logic device:***
    - 3 terminal FET vs. 1D structure, 2 terminal transistor, etc

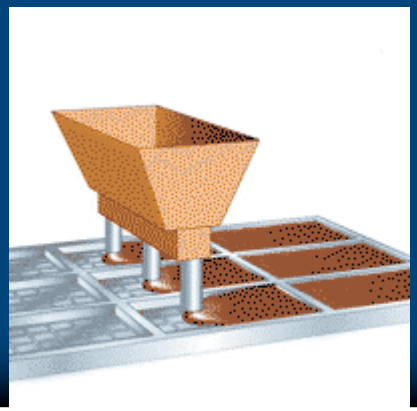
⇨Implication on logic gates / architecture

- **➢New basic logic gates**
  - **Majority gate, XOR gate, Multi-Valued logic, …**
- **➢New supported logic architectures**
  - **Crossbar, Cellular nonlinear network (CNN), bio-inspired neuro-functions, …**

Nano– Opportunities vs Challenges

- ☺ advantages
  - ✓ Abundant HW resources
  - ✓ High speed
  - ✓ Low power

- Challenges
  - **Reliability**
    - **Defect**
    - **Transient fault**
  - Interconnect
    - Nano-nano
    - Nano-CMOS
  - Fabrication
    - Bottom-up vs. top-down



Fabrication & interconnect challenges

- **Fabrication**

  - **Traditional Top-down lithography fabrication reaching physical limits**
    - **Loss of accuracy**
    - **Expensive**
  - **Bottom-up fabrication**
    - **Self-assembly process**

⇨ Fabrication implications:

- Lead to large # of defects
- Result in regular structures
- Require reconfigurability
  - ✓ build arbitrary circuits
  - ✓ bypass defects

- **Interconnect**

  - **Geometrical challenge of accessing nano scale devices**
    - Speed
    - Bandwidth

Interconnect limitation:

- Localized interconnect
- Expensive global communications

Unreliability challenge

Extremely small scale ⇨ unreliability of nano devices

- Fabrication limitation:
  - random location / orientation of nanotubes / nanowire growth
- Low noise / error immunity
  - stray charge influence
  - random charge hopping, crosstalk
- Single Event Upsets
  - cosmic rays, noise, temperature fluctuations, …

- Expected behavior
  - Permanent defects from manufacturing phase
  - In-service occurring defects
  - Semi-permanent errors
  - Transient errors

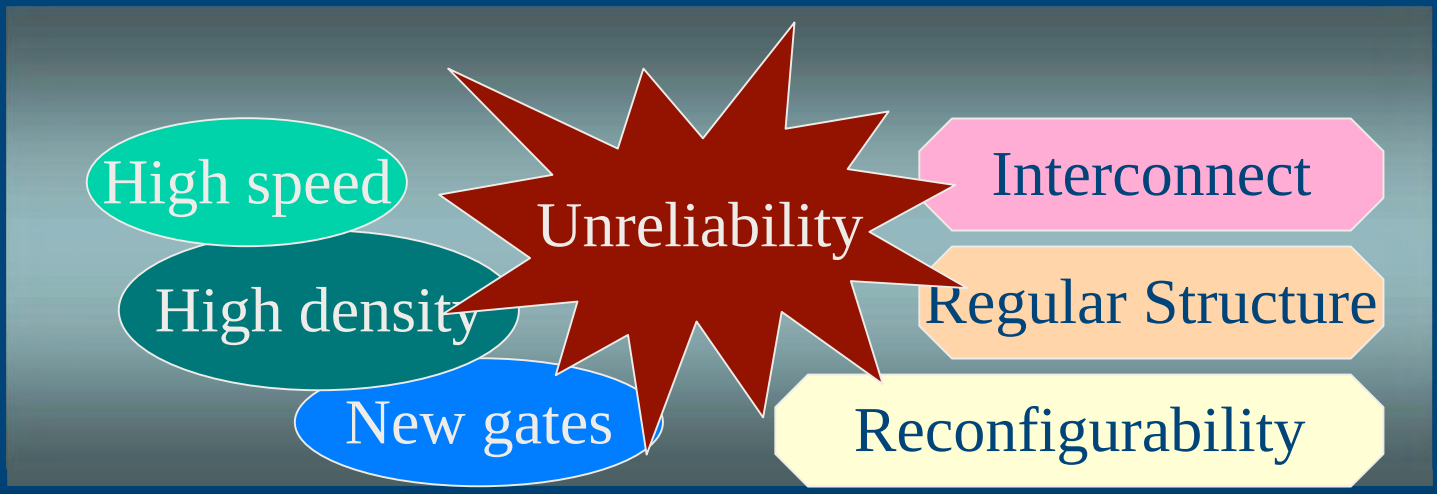
- Two forms of reliability challenges
  - **Manufacturing defects:** offline detect & repair
  - **Dynamic fault occurrences:** online fault tolerance

Specifically: new characteristics

- **Device density boost**
- **Novel basic gates**
- **Regularity of layout**
- **Reconfigurability**
- **Interconnect limitations**

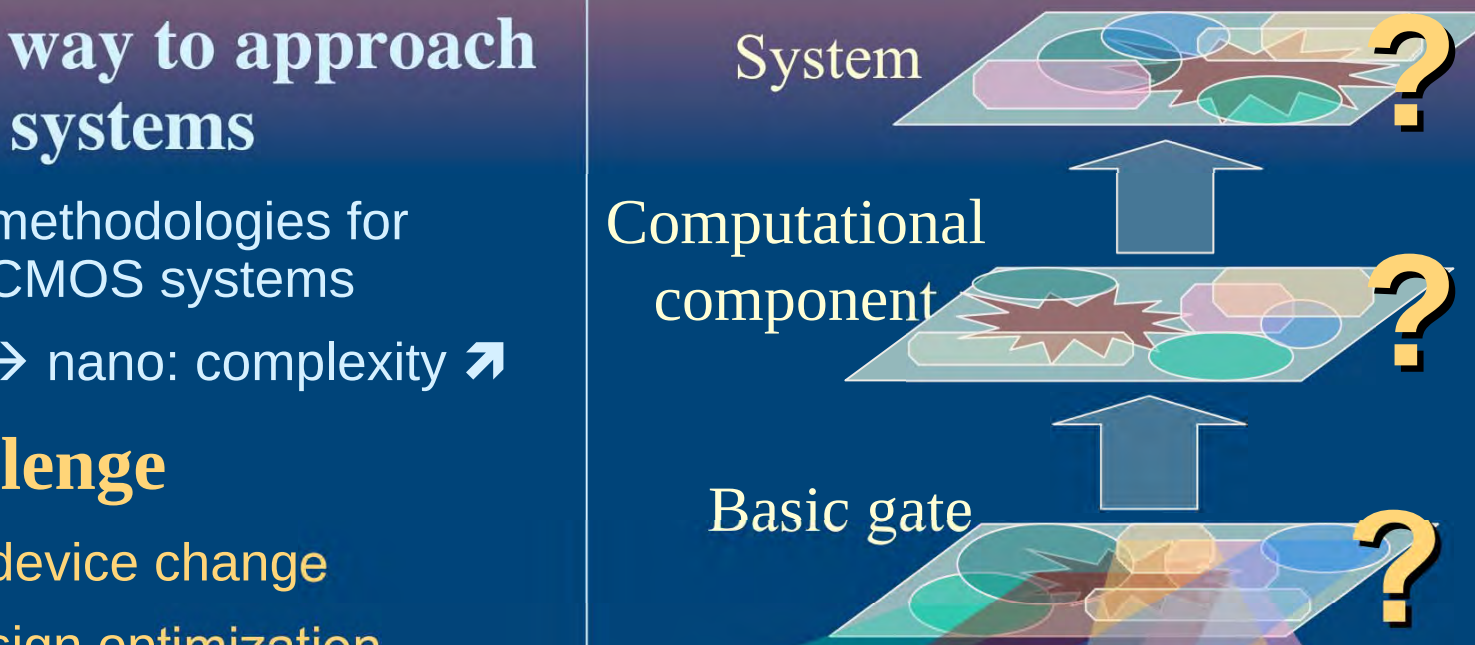
- → Resource & redundancy exploitable
- → Supporting novel FT strategies
- → Reducing complexity involved in diagnosis
- → Flexibility
- → Topology concern

Nanoelectronic environment



Hierarchical system construction

- **The only way to approach complex systems**
  - Mature methodologies for current CMOS systems
  - CMOS → nano: complexity ↗
- **New challenge**
  - Drastic device change
  - New design optimization considerations



Nano-scale devices

High speed

High density

New gates

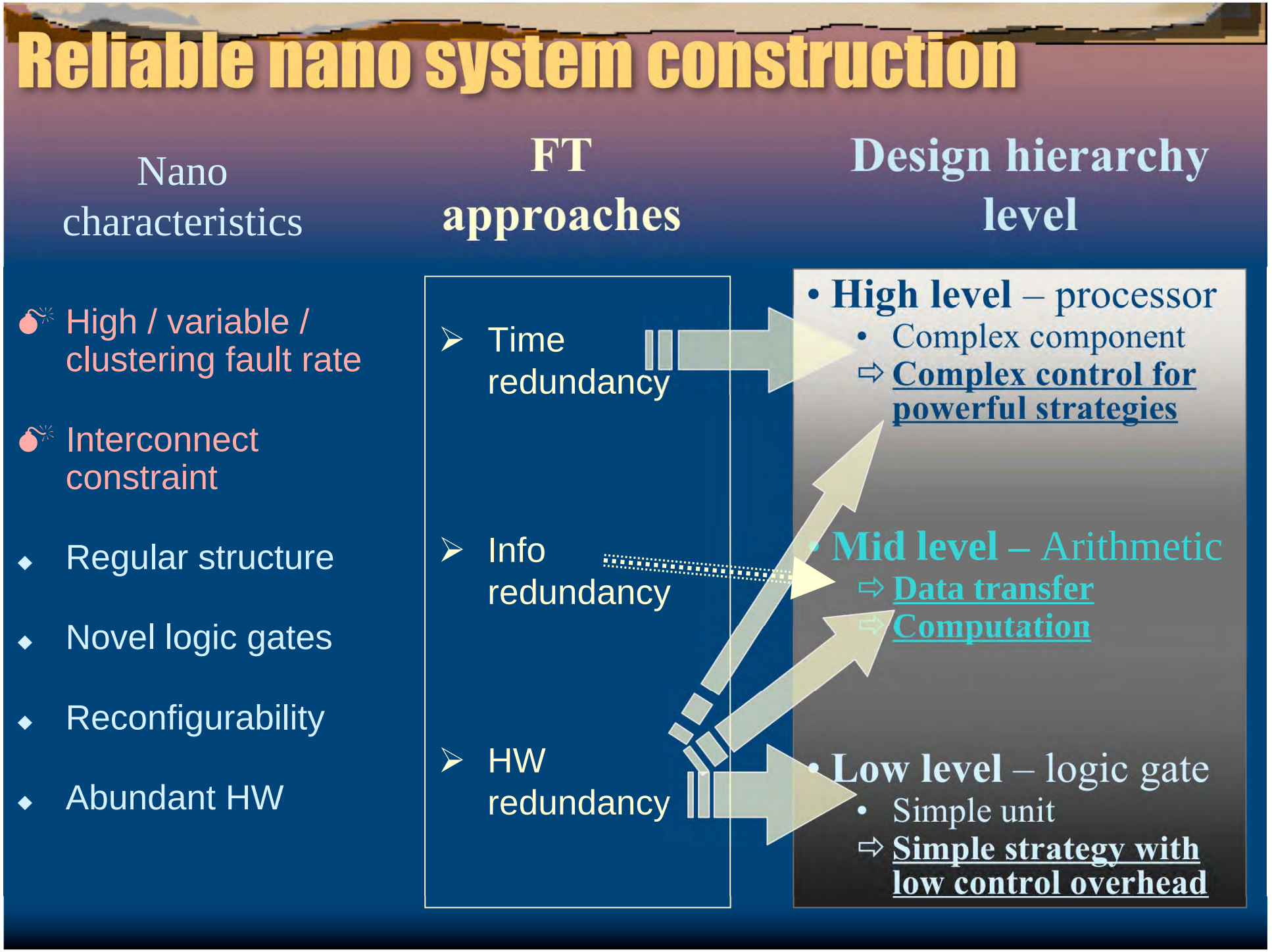
Unreliability

Interconnect

Regular Structure

Reconfigurability

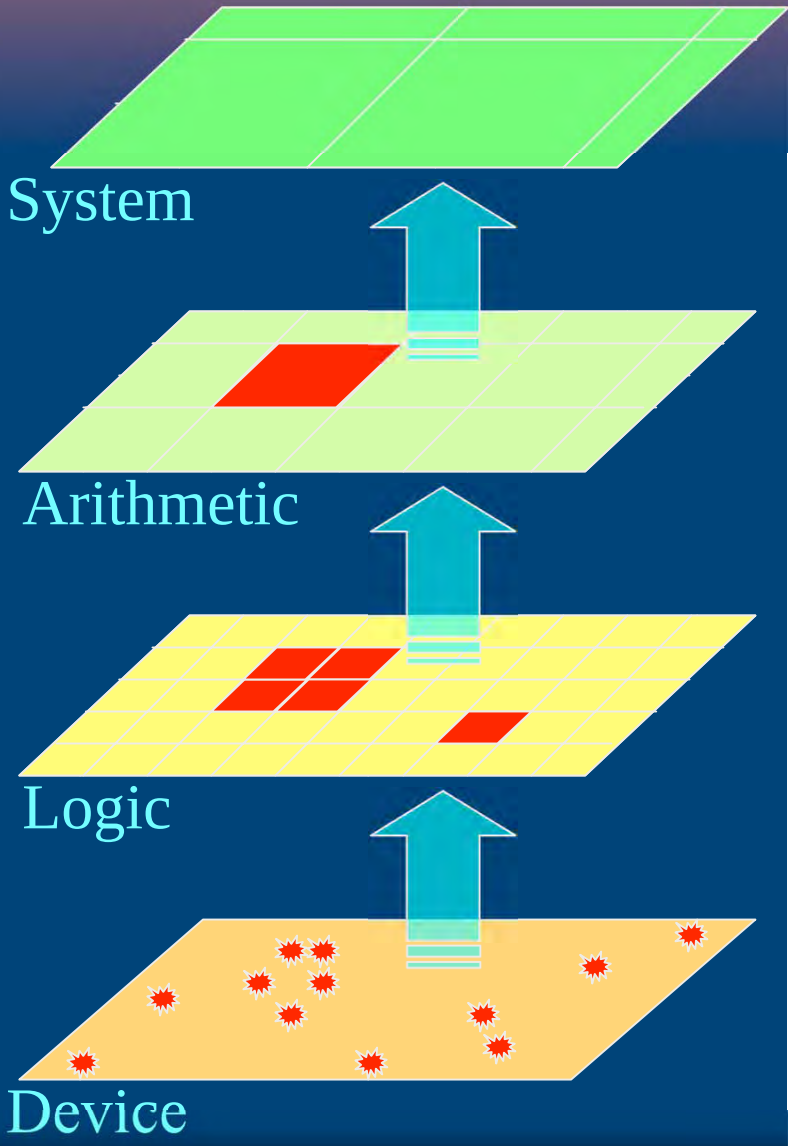
Reliable nano system construction



Hierarchical Fault Tolerance

- For clustered fault behavior
  - Superscaling effects in nano
- Can utilize various F.T. schemes
  - Applicable F.T. schemes vary at different levels

- Hierarchical F.T.
  - ✓ High fault rates – faults filtered through levels
  - ✓ Clustering of faults – upper level can use more global resources
  - ✓ Variable fault rates – flexible



Hierarchical FT in Nano system

Processor architecture

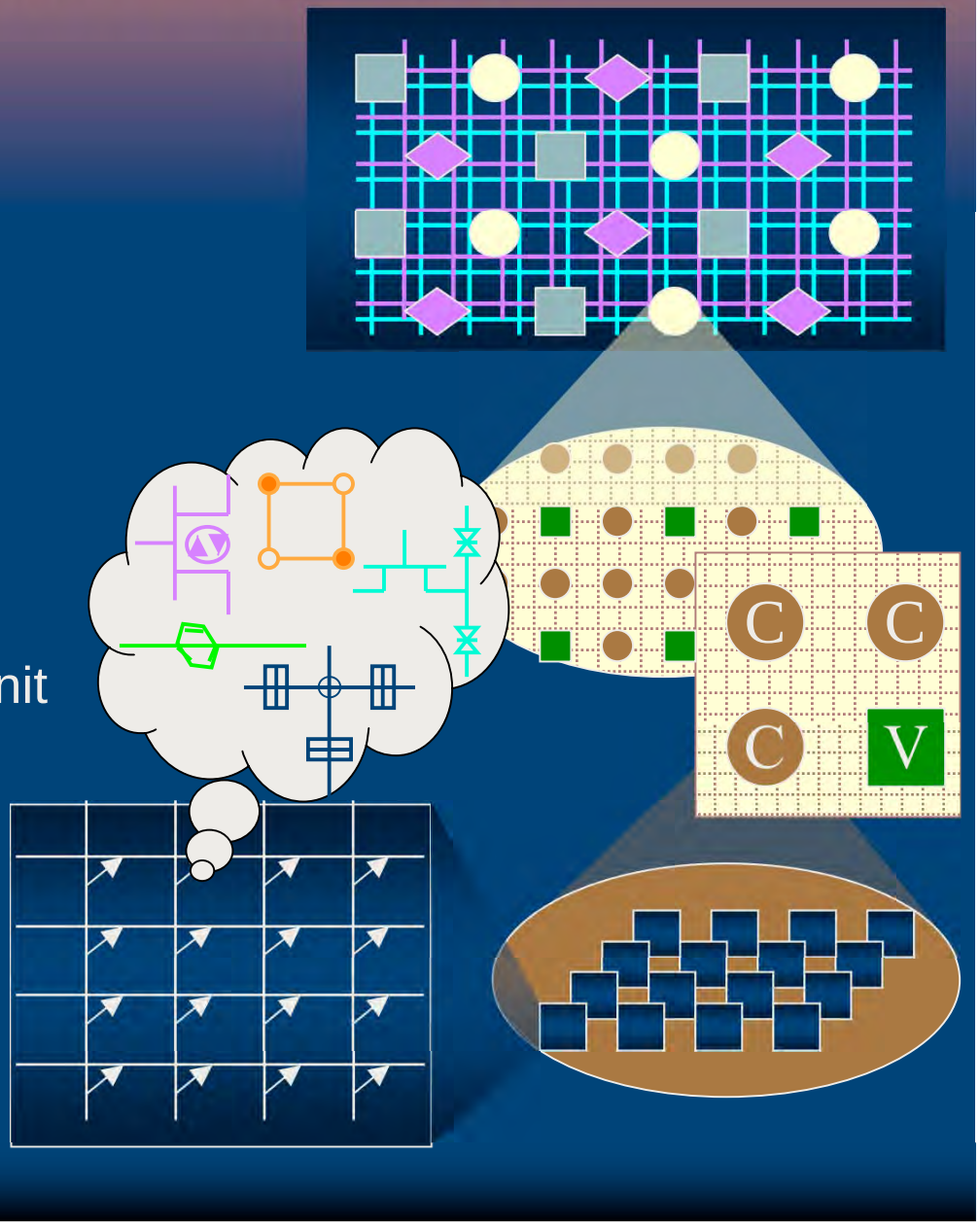
- FT computational model
  - HW, performance, F.T. capability
- Topology consideration
  - Distributed control

Arithmetic component

- Memory / data transfer
  - Coding based FT
- Arithmetic / logic computation unit
  - NMR based fault masking
  - Reconfiguration based online repair

Logic gate

- Defect aware logic synthesis
- HW redundancy based FT



Nano system: order out of disorder

- Reliability
  - Goal: reliable computation
  - Challenge: unreliable HW
  - Feasibility: given enough redundancy
    - *von Neumann: computations may be done reliably with a high probability, even based on gates with certain failure probability – given enough HW redundancy.*
- Nanoelectronic systems
  - Goal: extending Moore's law beyond CMOS scale
  - Foreseeable severe challenges
  - Eventually deliverable – *given the involvement of active research*