FPGA Hardware Implementation of Statically-Derived Application-Aware Error Detectors

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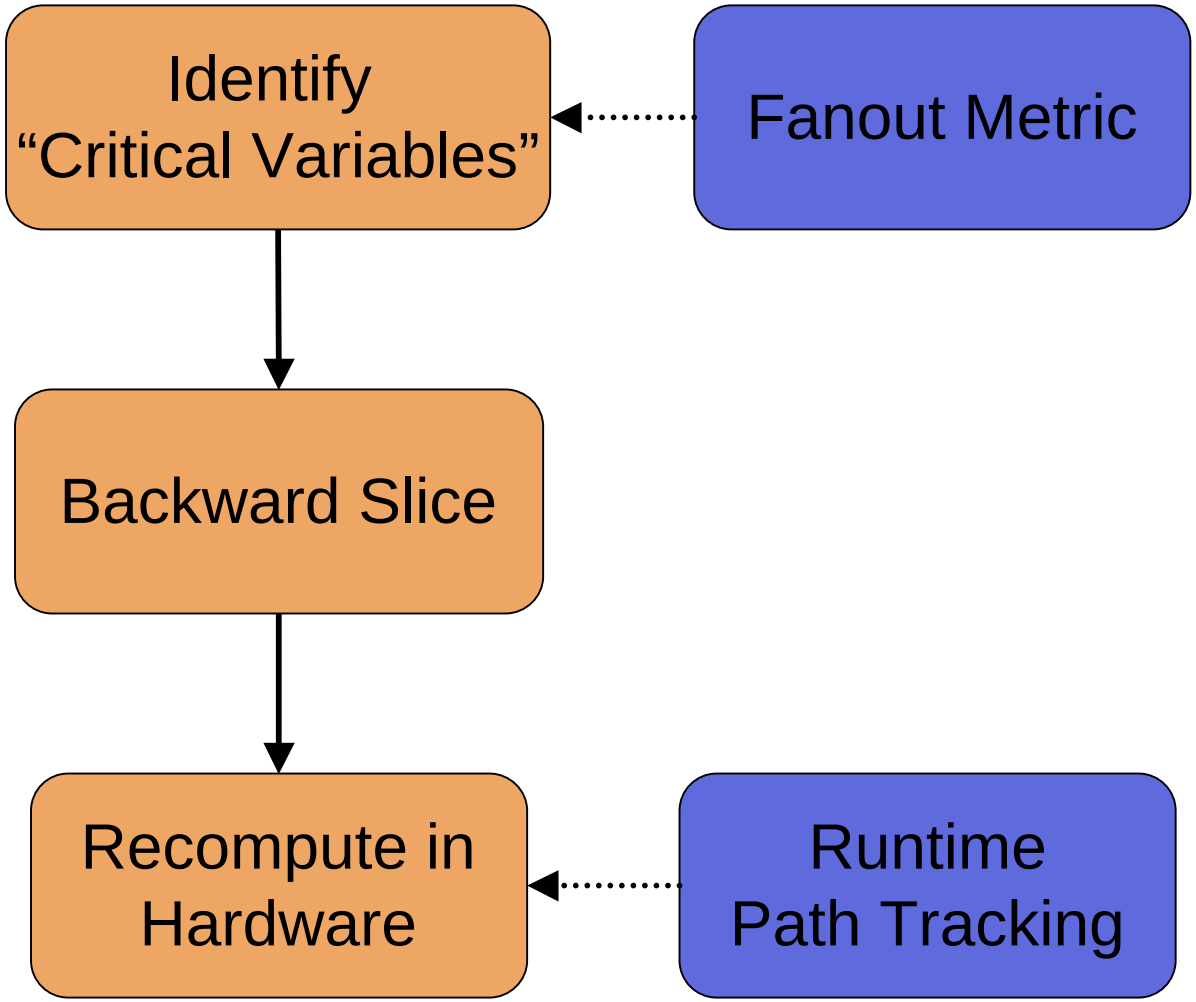
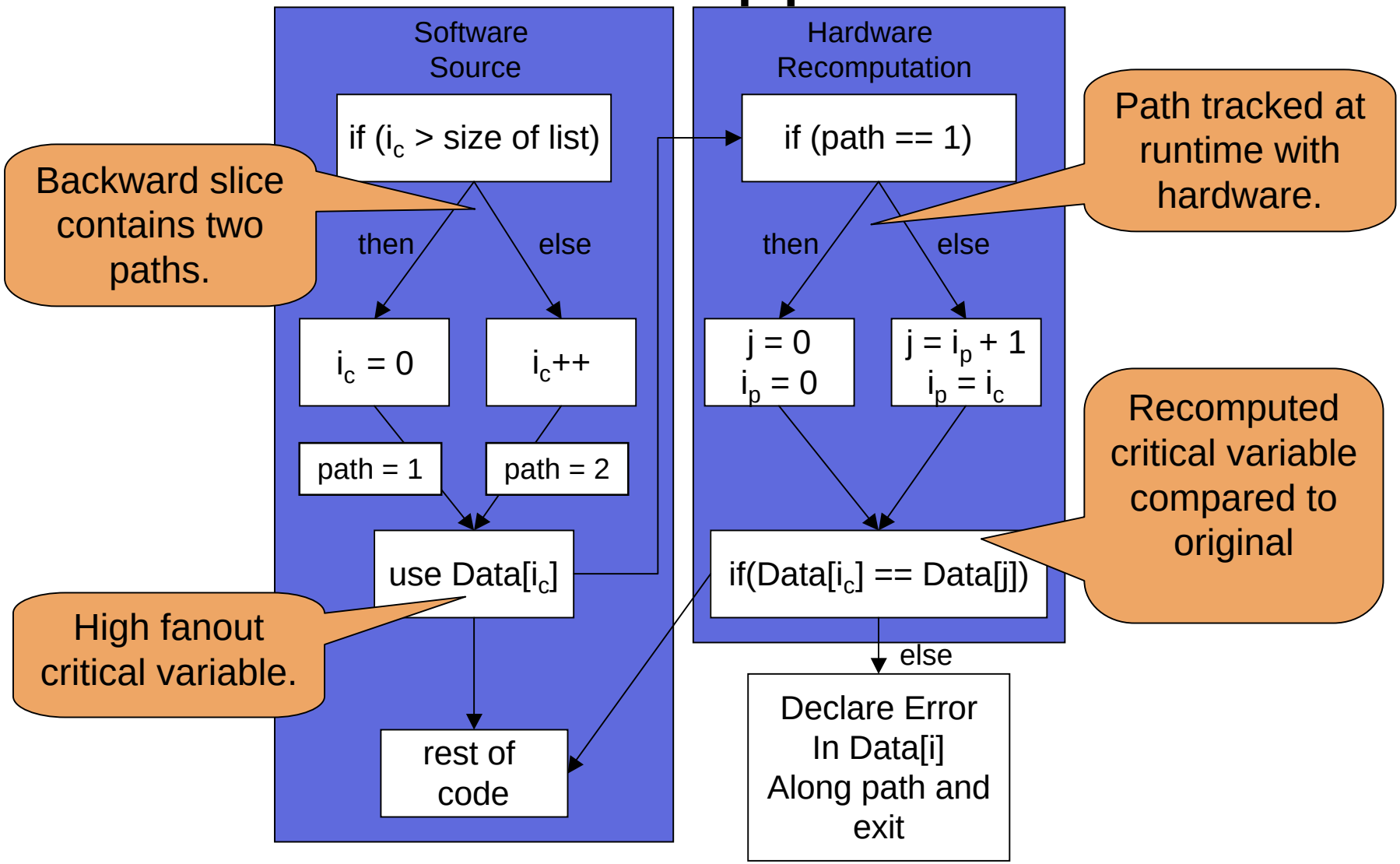
Motivation

- Nano-regime new types/severity of errors.
- Traditional solutions expensive.
- One size fits all approach not appropriate.
- Low cost and high coverage.
- Application-aware techniques.
- Hardware implementation.

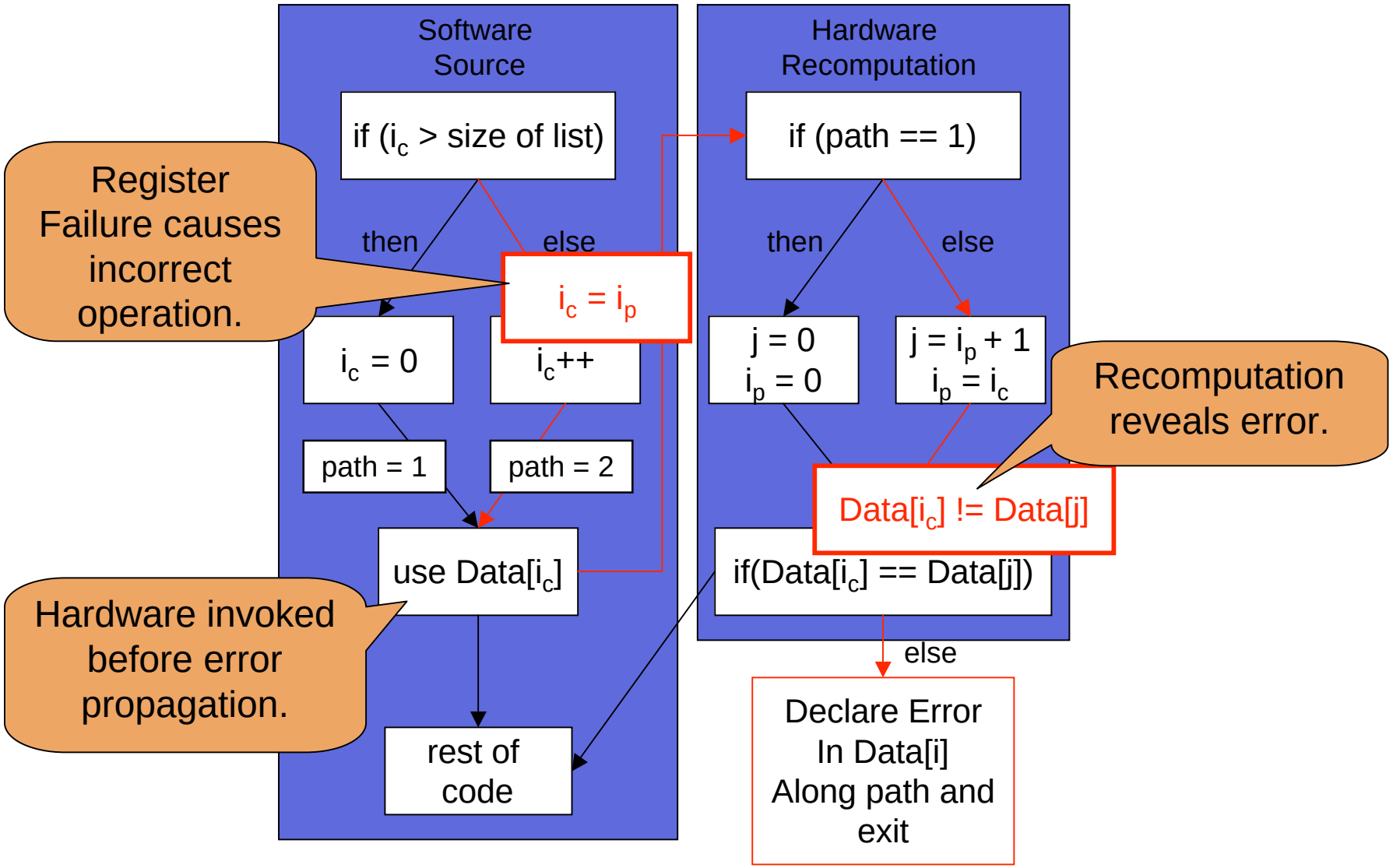
Technique


Identify
“Critical Variables”
Fanout Metric
Backward Slice
Recompute in
Hardware
Runtime
Path Tracking

Derivation of Detectors: Bubblesort Application

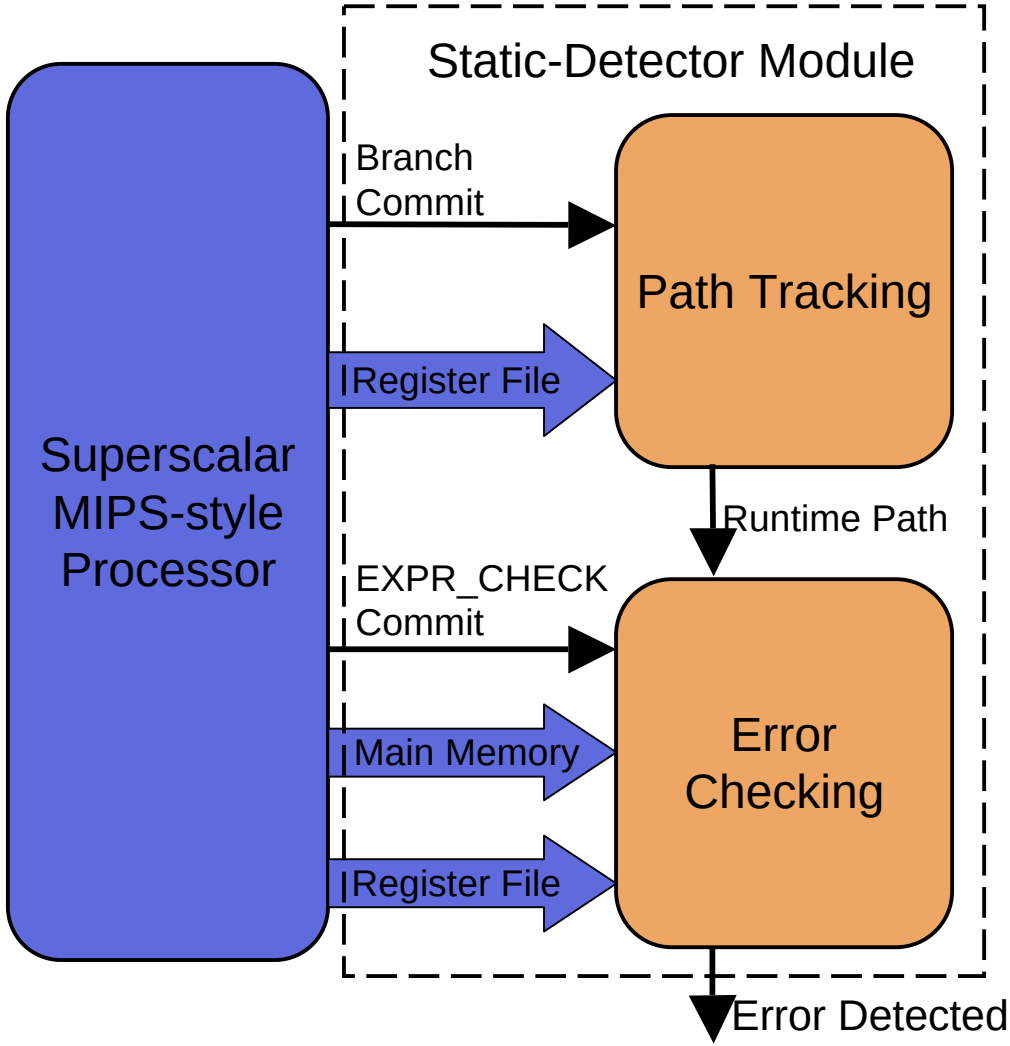


Detection of Error



Hardware Implementation

- Static Detector Module (SDM) provides:
  - Recomputation
  - Checking
- SDM Sub-modules:
  - Path Tracking
  - Error Checking
- Commit unit access.
- Register file access.
- Direct memory access.



Performance Evaluation - Setup

- Software executes on superscalar DLX.
- dlxcc generates dlx assembly.
- VHDL simulations of the system (processor + checking) in ModelSim 6.2.
- Hardware synthesis for Xilinx Virtex-2 Pro FPGA with Xilinx ISE 7.1 toolflow.
- Simulation results validated against hardware.

Performance Evaluation

Performance	Cycles	Performance Overhead
No Instrumentation	30,067	-
SW Static-Detector Module	136,607	354%
HW Static-Detector Module	57,411	91%
Static-Detector Module w/DMA	**30,688**	**2%**

Synthesis	Slices	Max Frequency
DLX	12,262	76 MHz
DLX + Static-Detector Module	12,533	77 MHz

Significant performance savings over software duplications.
Path tracking provided with minimal overhead.
DMA significantly increases checking performance.
Minimal area overhead
Maximum clock frequency not affected.

Conclusions and Future Work

- Significant performance savings.
- Low area overhead.
- Diversity in hardware computation units.
- Future Work:
  - Expansion to larger benchmarks.
  - Performance and resource feedback for detector optimization.