Time Redundancy Processor with a Tolerance to Transient Faults Caused by Electromagnetic Waves

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Outline

1. Background
2. Purpose
3. Transient fault modeling
4. Time redundancy processor
5. Experimental results
6. Conclusions

Background

- Recent semiconductor manufacturing
  - higher integration with DSM
  - lower power consumption
  - higher operating frequency

- Problems
  - degradation of tolerance of devices
  - serious influences of transient faults
    - soft error, crosstalk, electro-magnetic (EM) pulse, etc.

Transient faults

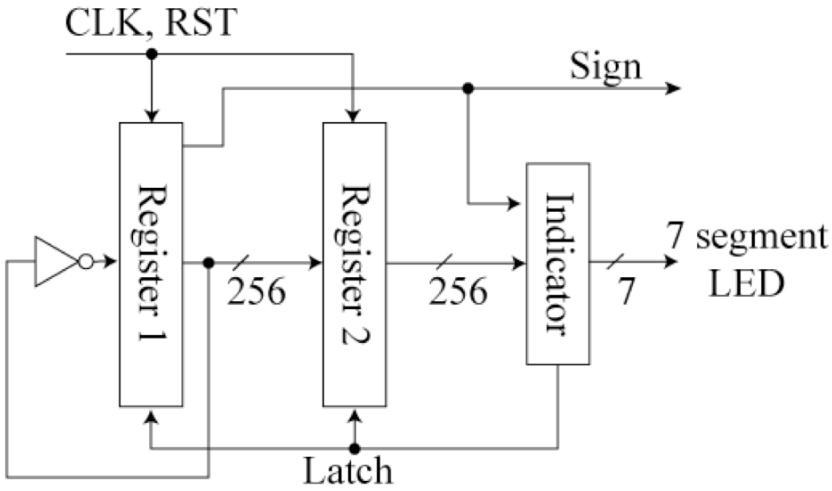
- Caused by EM pulse, cosmic ray neutron, etc
- No damage on hardware itself
- Induce malfunctions of systems
- Generation mechanism:
  - Single event upset (SEU)
  - Single event transient (SET)
- few countermeasures against widely-affecting multi-bit error

Purpose

- Discuss processor with tolerance against transient faults
- Assume widely-occurring transient faults
  - EM wave caused by capacitor discharge
  - Effects of EM waves:
    experiments → establish fault model
- Design time redundancy processor
- Experiments for transient fault injection

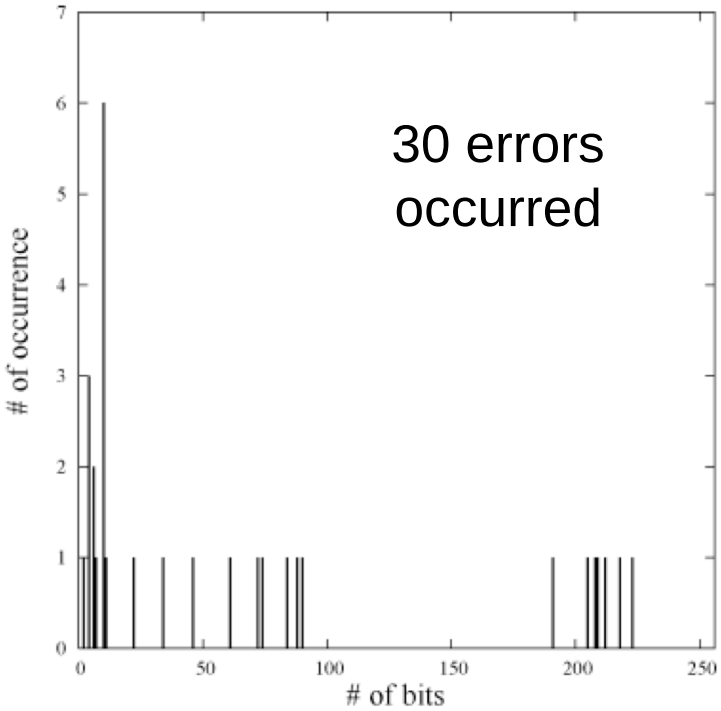
Establishing fault model

- FPGA: Xilinx Spartan Ⅱ
（XCS200-PQ208）
- Fault injection：
by capacitor discharge
- Capacitor capacity: 6800 uF
- Clock signal:
72 kHz generated by a
function generator
- Voltage of capacitor charge:
10 V
- # of trials: 200

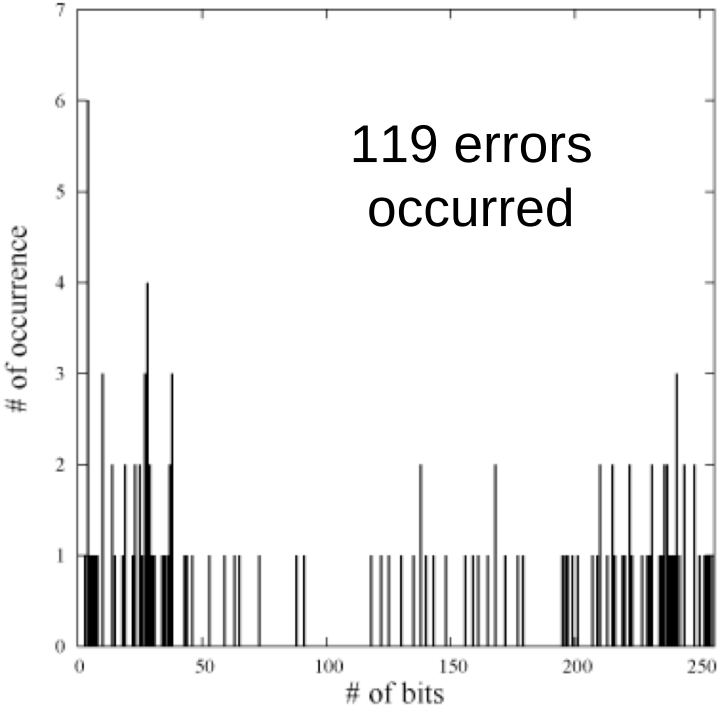


Experimental results (1)

distribution of erroneous bits caused by one capacitor discharge



0→1 error



1→0 error

confirm larger-scale impacts than soft errors

Experimental results (2)

Capacitor discharge with no clock input

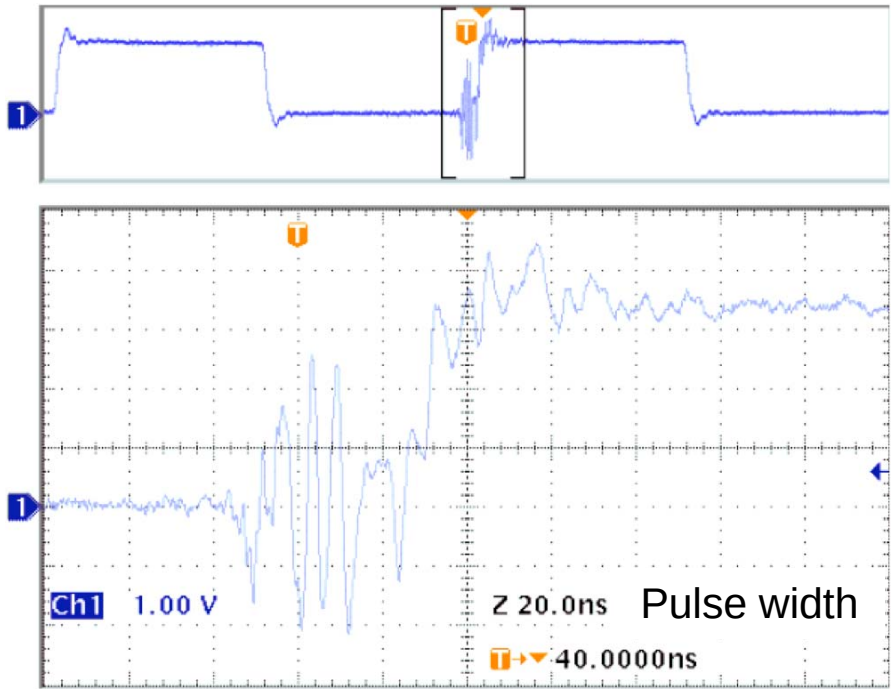
- no flip observed
- configuration of FPGA not affected

Transient fault caused by capacitor discharge

- instantaneous pulse for clock signal line
  - FPGA does not have oscillator
- FF capture incorrect value at incorrect timing

Fault model

1. Transient fault does not affect the internal signal line in the chip
2. The transient fault affects only the external clock signal line.
3. The duration of the transient fault is no more than two clock cycles.



Time redundancy processor

Overview

- Execute each state twice
  - assume not the same fault effect on the results
- Compare calculation results
  - introduce buffers partially

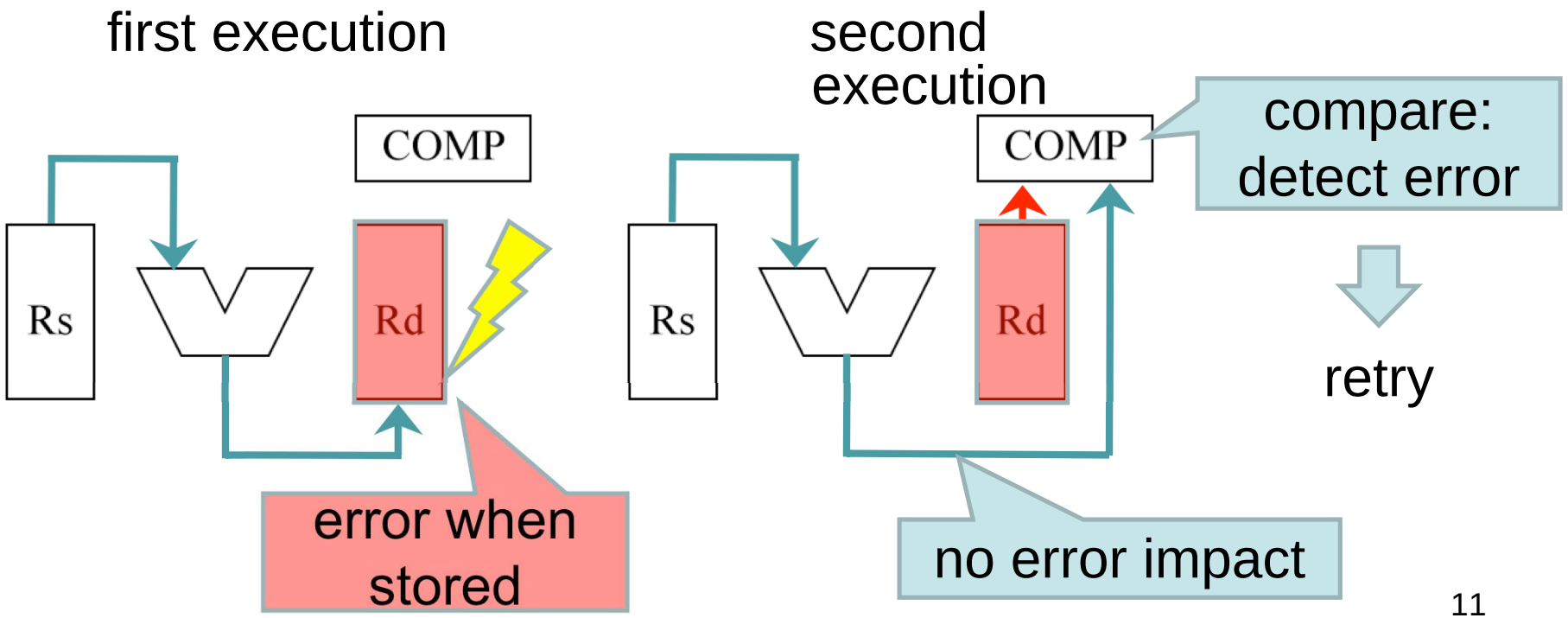
  ⇨ faults can be detected

- retry faulty execution
  - effect of transient fault = recoverable

  ⇨ fault effect is overwritten

Example of error detection

- Calculate from Rs → store to Rd



Implementation of time redundancy processor

Design specification of processor core：

- implement subset of instruction set ofH8/300 CPU by Renesas technology Inc.

Result of logic synthesis

processor	CS ratio	FF ratio	LUT ratio
normal	1	1	1
time redundancy	1.63	1.58	1.65

(CS: Chip Slice, LUT:Look Up Table)

FPGA: Xilinx VIRTEX-E（XCV300E-6PQ240C）

Synthesizer tool: Xilinx ISE web pack 7.1i

Experiments for transient fault injection

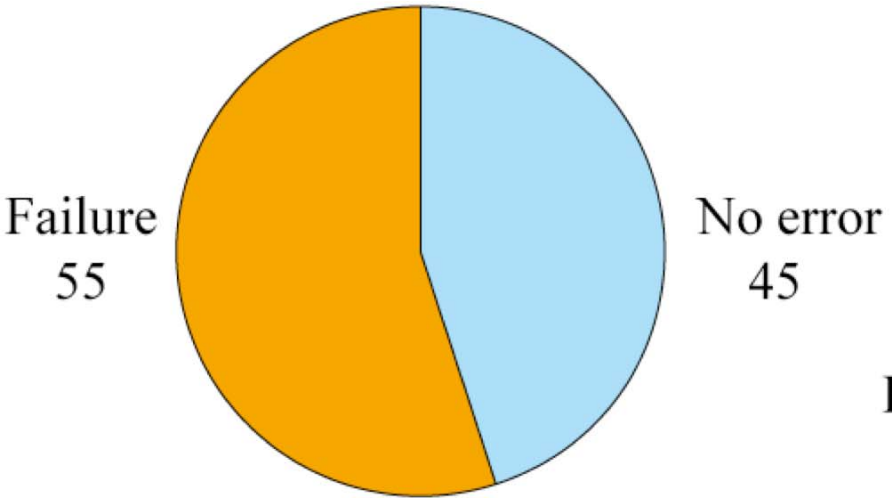
Inject transient faults for each processor

- check if error detected and state recovered

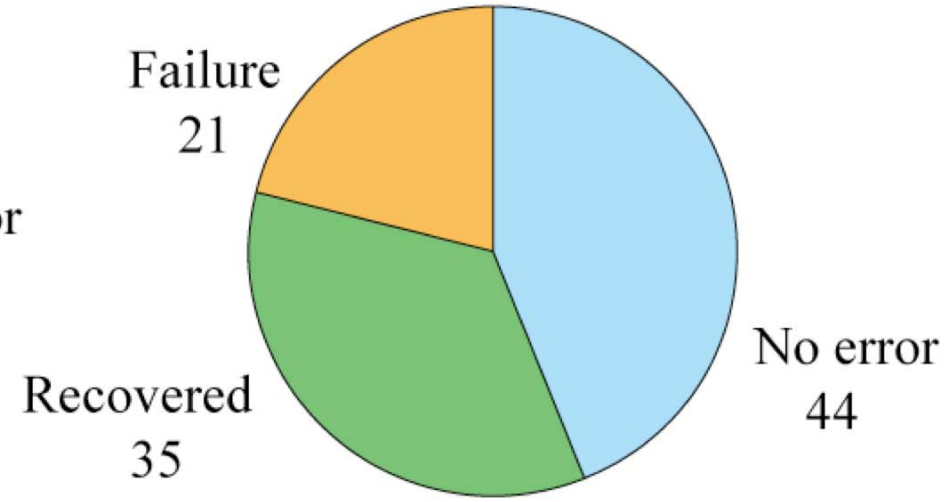
Conditions for experiments

- Capacitor capacity : 6800uF
- Clock signal : 100KHz by a function generator
- Voltage of capacitor : 10V
- # of trials : 100
- Executed instruction : inter-register data transfer

Experimental results (3)



detail for normal processor



detail for time redundancy processor

time redundancy processor

- higher probability of correct operation
- recovery rate: 62%
  - recovery from detected error

Conclusions

- Examined influences EM waves by capacitor discharge
  → establish fault modeling
- Design/implement time redundancy processor
- Experiment of transient error injection
  → improved probability of correct operation, but perfect tolerance not achieved