Manufacturing Process Variations and Dependability
A Contrarian View

Janak H. Patel

Department of Electrical and Computer Engineering

University of Illinois at Urbana-Champaign

Semiconductor Trends

- **Technology Projections from ITRS**
  - 15 Years in to future
  - CMOS will continue to dominate
  - Some of the concerns of scaling
    - Manufacturing Defects
    - Age dependent degradation
    - Process Variations

Trends in Circuit Technology

- **Supply Voltage is Decreasing to save Power**
  - Reduces Signal to Noise Ratio
- **Device Threshold is Decreasing to maintain or increase performance**
  - Increases Sub-threshold Leakage Currents
- **Wires are getting taller and closer**
  - Increases Coupling Capacitance
  - Increases Crosstalk Noise
- **Statistical designs vs. Worst Case assumptions**
- **Manufacturing Test is getting harder**
  - Some timing defects go undetected

Manufacturing Defects

- **Defect Density**
  - Number of Electrical Defects/m^2 chip area
  - Defect Density has a direct impact on the Yield and hence the profitability of a manufacturing line
  - Since testing for defects is an imperfect process, defect density also impacts quality
  - ITRS goal for the next Five years is
    - Maintain defect density constant at 1395 defects/m^2
  - Since the number of transistors double every 2-3 years per unit area, the defects/transistor must halve every 2-3 years!!
- **Hard Faults: Not a serious concern for dependability**

Age Dependent Faults

- **Known Sources of Degradations**
  - Gate oxide breakdown, Charge trapping in oxide, metal migration, structural weakening of dielectric and interconnect from thermal fluctuations
  - These effects are accurately predictable from physical model and lab measurements
  - ITRS projects
    - Short term goals: 50 to 2000 failed parts/million
    - Long term goals:

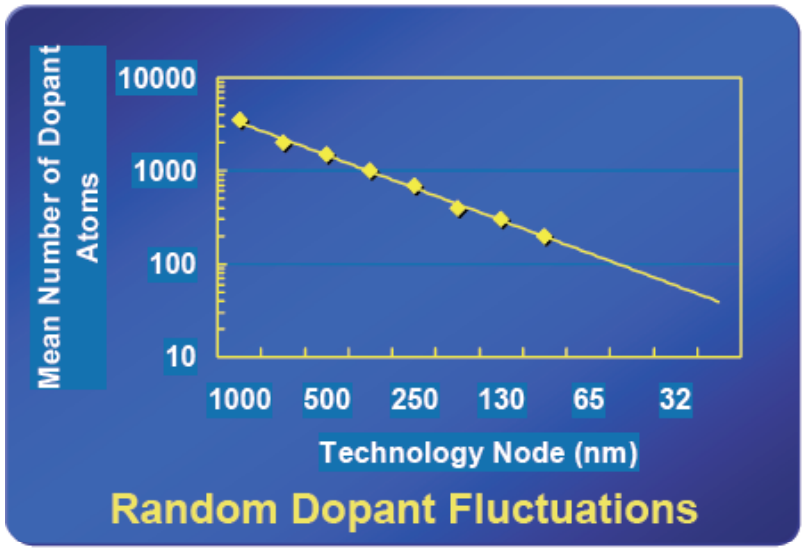
      10 to 100 FITS (failures/billion device-hours)
- **Failures per/transistor must decrease!**

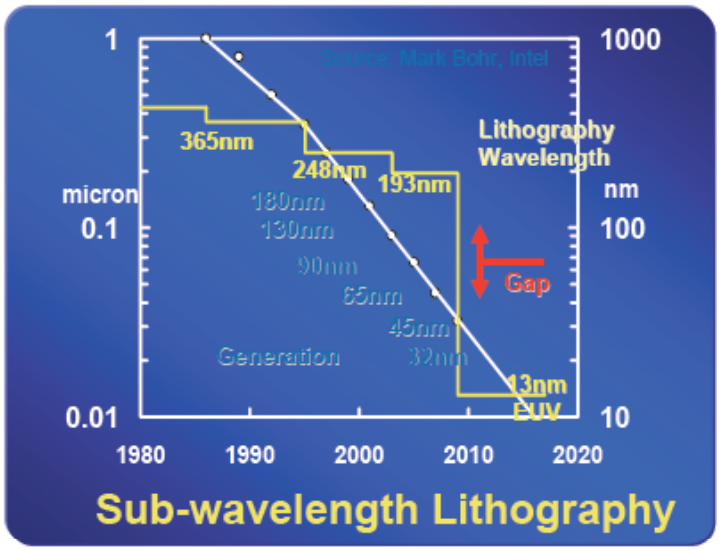
Process Variations

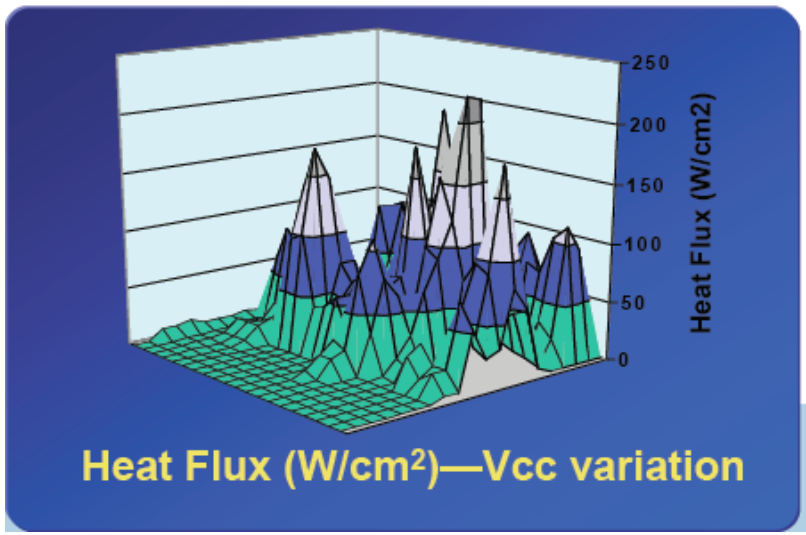
- **Sources of Variations**
  - Gate Oxide thickness
  - Doping density
  - Device geometry, Lithography in nanometer region
  - Transistor Threshold V_T
    - Sub threshold current, leakage, power, frequency
- **Range of Variations**
  - 100% V_T variation across a modern chip
  - 30% speed variation across a wafer
  - 100% leakage (static power) variation in a wafer

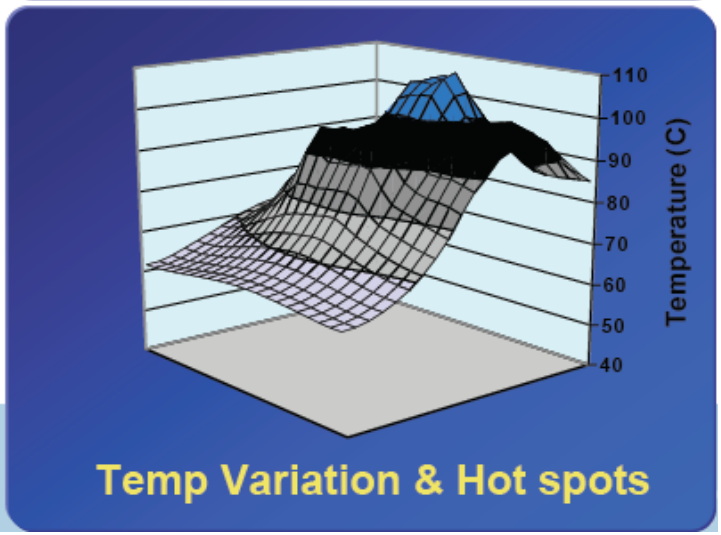
Sources of Variations

(from Shekhar Borkar, Intel)

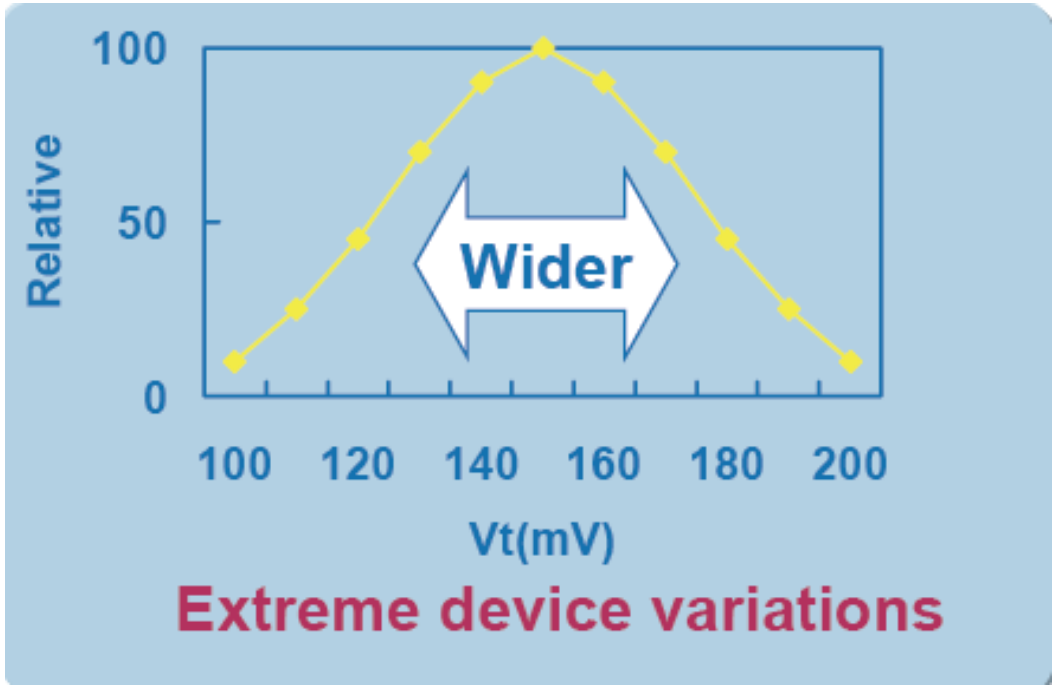






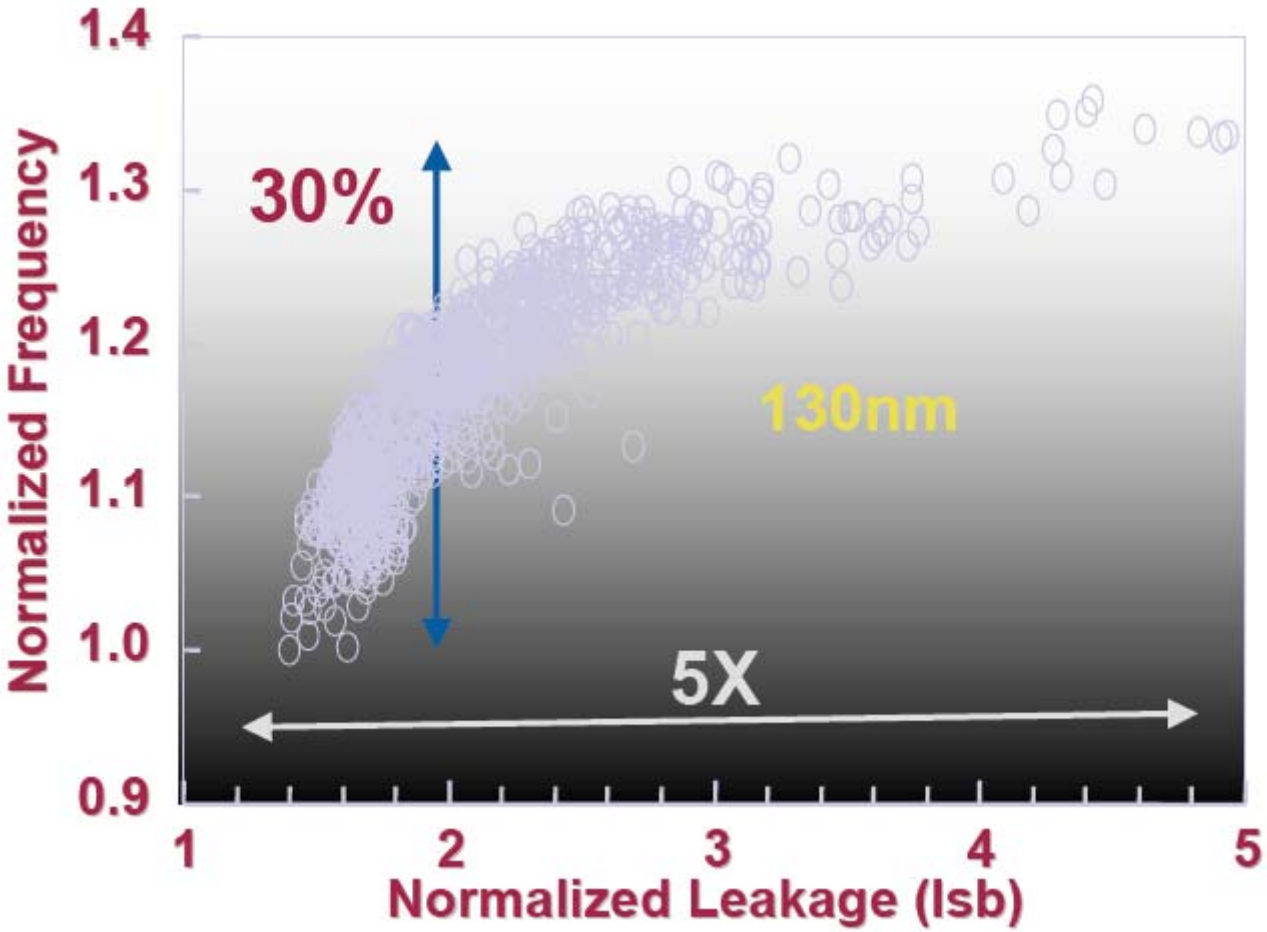


Transistor Threshold V_t

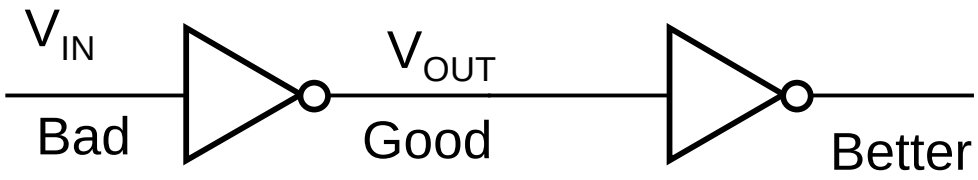


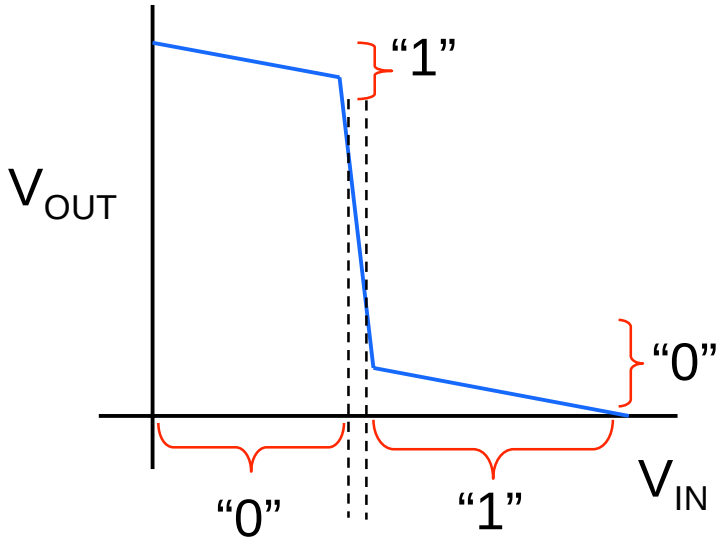
Static Variations today

(source: Shekhar Borkar, Intel)



Inherent Robustness of Gates

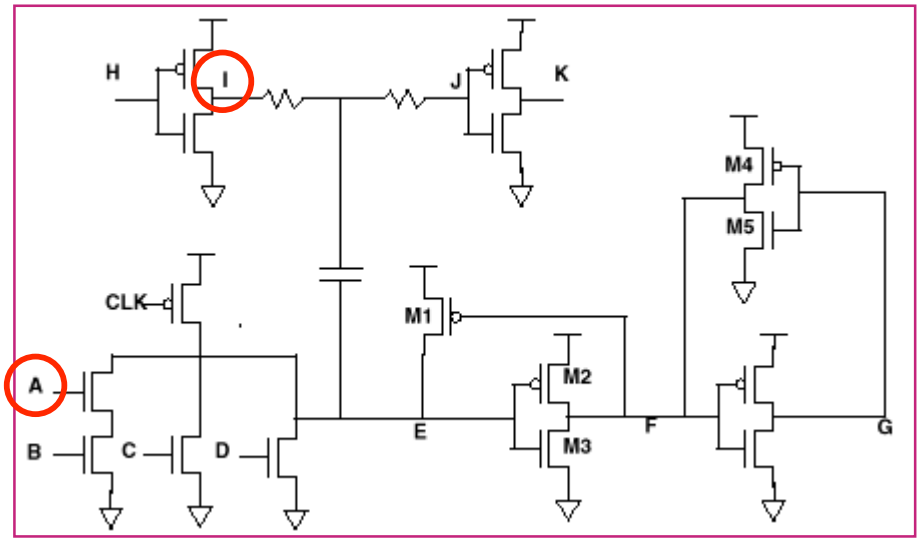


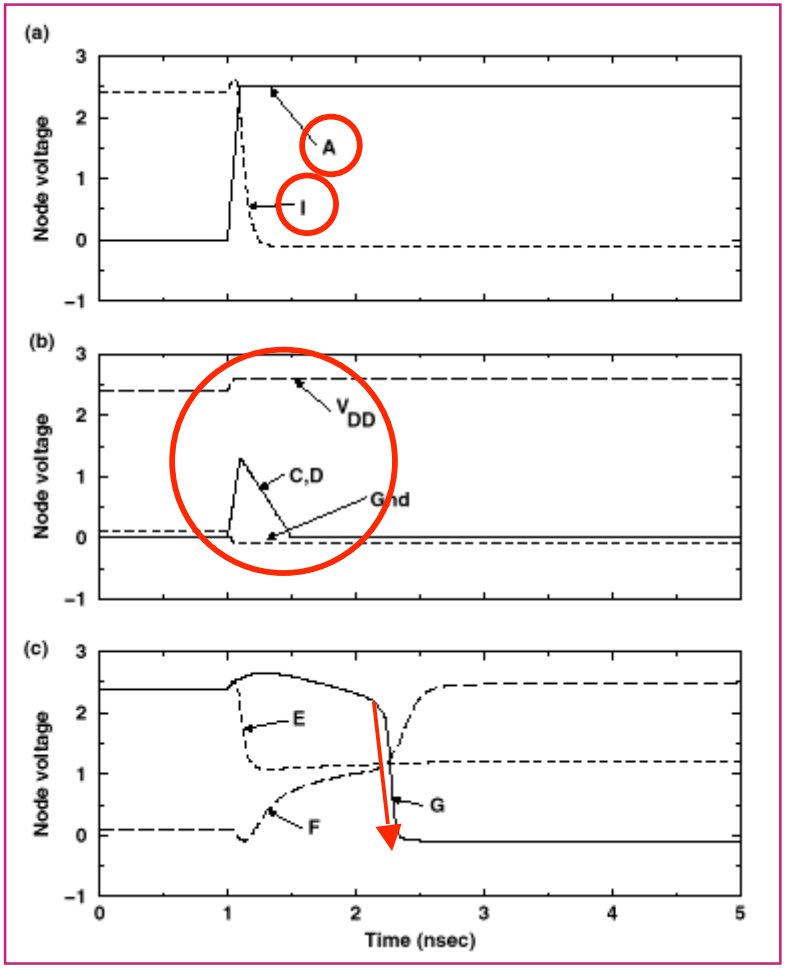


Voltage Transfer Curve

Regeneration Property:
Every Logic Gate improves its input signal quality

Example: Circuit Simulation of A Bit Flip due to Noise





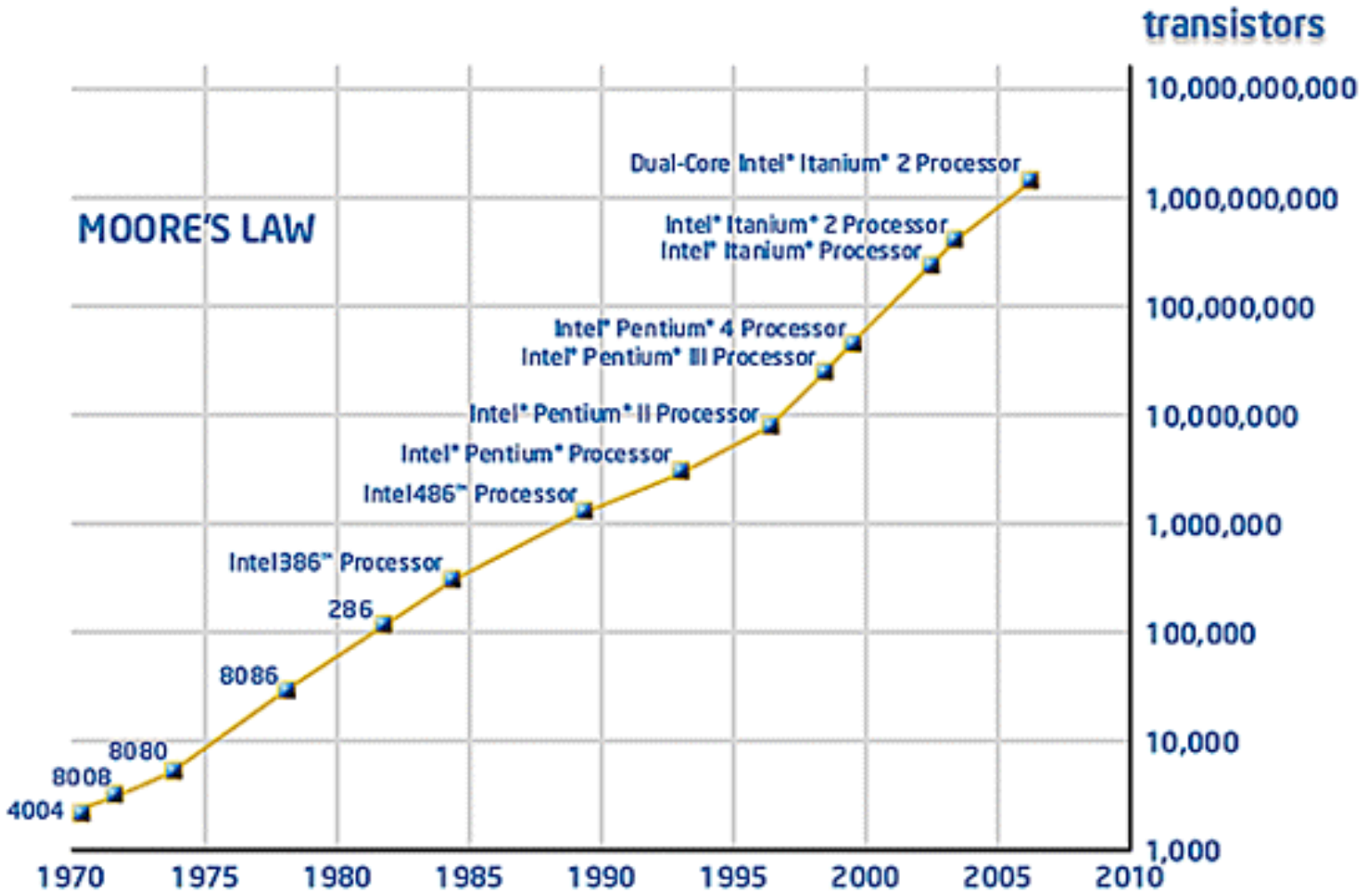
(a) Driver output **I** is switching as is node **A**.
(b) Coupling noise appears on inputs **C** and **D** along with power-supply noise on the voltage rails.
(c) The dynamic node **E** falls, switching the output inverter of the domino gate **F** and the latch output **G.**

Source: Kenneth L. Shepard, "Design methodologies for noise in digital integrated circuits," 35th Design Automation Conf. pp. 94-99, 1998. © 1998 ACM

A Thought Experiment

- **Let us suppose process variations in future are so large as to have some transistors very slow**
  - Let us say 0.1% of all transistors are very slow
  - If we exercise the microprocessor with extremely large work load – lots of computations, lots of switching activity, large temperature variations, we should see some errors
  - 0.1% of one Billion Transistors is 1 Million!
  - 0.01% of one Billion is 100k
- **Hypothesis**
  - 100k slow transistors must cause massive failures!

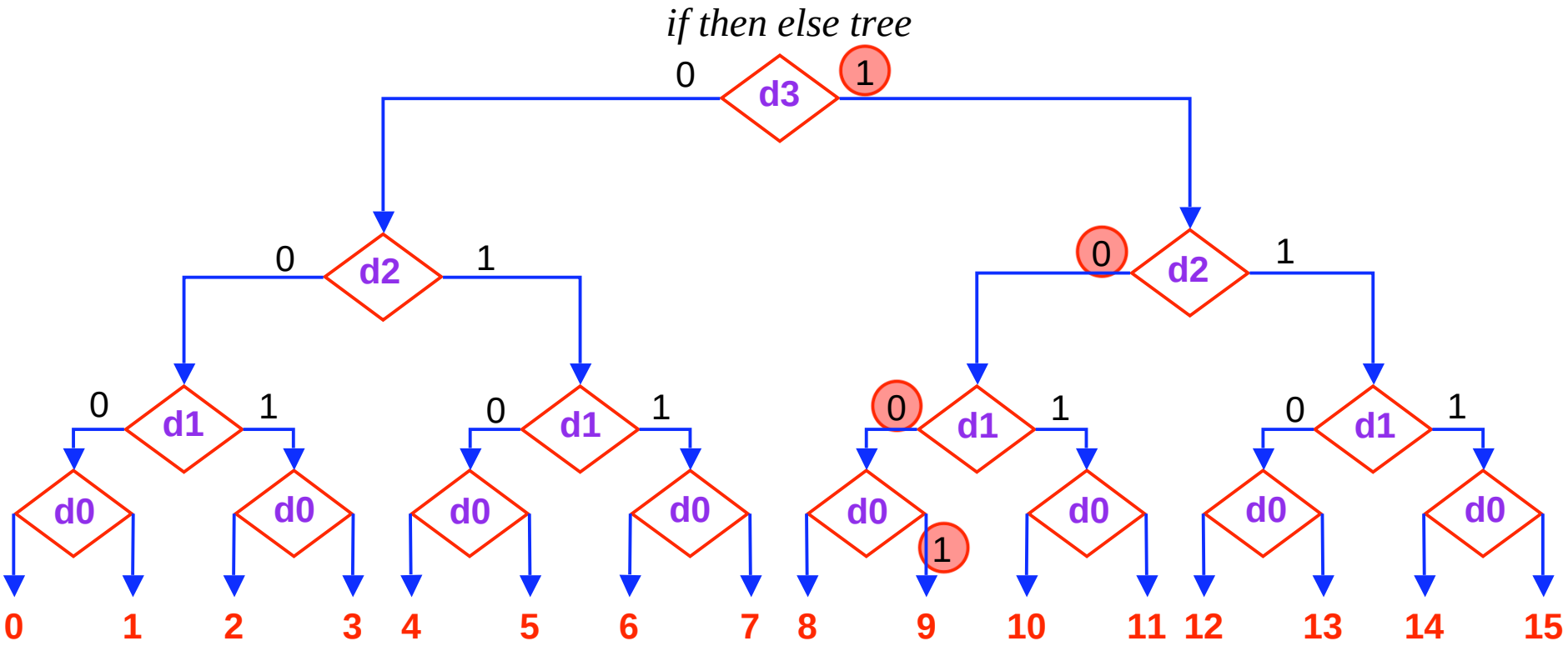
Moore's Law


transistors
MOORE'S LAW
Dual-Core Intel® Itanium® 2 Processor
Intel® Itanium® 2 Processor
Intel® Itanium® Processor
Intel® Pentium® 4 Processor
Intel® Pentium® III Processor
Intel® Pentium® II Processor
Intel® Pentium® Processor
Intel486™ Processor
Intel386™ Processor
286
8086
8080
8008
4004
10,000,000,000
1,000,000,000
100,000,000
10,000,000
1,000,000
100,000
10,000
1,000
1970
1975
1980
1985
1990
1995
2000
2005
2010

Exercising a Microprocessor

- **For each ALU Operation (e.g. ADD, SUB, AND, XOR, …) several operations with known operands and known results are placed in a tight loop**
- **Try to maximize the execution rate of each operation**
- **Try to maximize the logic switching rate**
  - High switching causes IR drop in power bus
- **Try to utilize all functional units**
- **Exercise pipeline control logic**
  - Independent and Dependent Operation

Exercising Branch Prediction Unit



Integer $d_3d_2d_1d_0$ = 1001 = 9

Experimentation with PowerPC 750

Routine	Operations per loop	Number of loops	Total Operations	Approx. Running Time	**Approx. Operations Per Second**
Register Unit	40	8,000,000	320,000,000	6.34 s	**50.47×10^6**
Instruction Fetch Unit	32	8,000,000	256,000,000	92.04 s	**2.78×10^6**
Integer Addition	40	8,000,000	320,000,000	9.35 s	**34.22×10^6**
Integer Subtraction	40	8,000,000	320,000,000	9.12 s	**35.09×10^6**
Integer Multiplication	58	8,000,000	464,000,000	18.21 s	**25.48×10^6**
Integer Division	50	8,000,000	400,000,000	33.72 s	**11.86×10^6**
Logical AND	20	8,000,000	160,000,000	0.71 s	**225.35×10^6**
Logical OR	20	8,000,000	160,000,000	0.64 s	**250.00×10^6**
Logical XOR	20	8,000,000	160,000,000	0.71 s	**225.35×10^6**
Integer Unit 2	40 adds & multiplies	8,000,000	640,000,000	48.75 s	**13.13×10^6**
Floating Point Add	20	8,000,000	160,000,000	0.82 s	**195.12×10^6**
Floating Point Subtract	20	8,000,000	160,000,000	0.82 s	**195.12×10^6**
Floating Point Multiply	20	8,000,000	160,000,000	0.83 s	**192.77×10^6**
Floating Point Divide	20	8,000,000	160,000,000	0.82 s	**195.12×10^6**
Branch Processing Unit	7	8,000,000	56,000,000	6.09 s	**9.20×10^6**
Load/Store Unit	320 loads, 192 stores	80,000	40,960,000	13.24 s	**3.09×10^6**
Data Cache	2	3,300,000	6,600,000	15.97 s	**0.41×10^6**

Experimental Set-UP

- **A Single-Board-Computer (SBC)**
  - WindRiver SBC750
  - Motorola PowerPC 750 Microprocessor
  - 233MHz, 2.5V Power Supply
  - A Host Computer
  - WindRiver debugging software
  - HyperTerminal Software for serial communication
  - A Hewlett-Packard E3631A Power Supply
    - Digital control in units of 1/100th Volt changes
  - A Blow-Drier to raise the temperature

Results of Lowering Supply Voltage

Board No.	No. Tests	Error Generated at Supply Voltage	Control Flow Errors Detected	
			System Hangs	Program Crashed
1	45	1.99 V – 2.10 V	31	14
2	35	2.00 V – 2.08 V	26	9
3	25	2.10 V – 2.29 V	18	7
4	25	2.08 V – 2.20 V	17	8

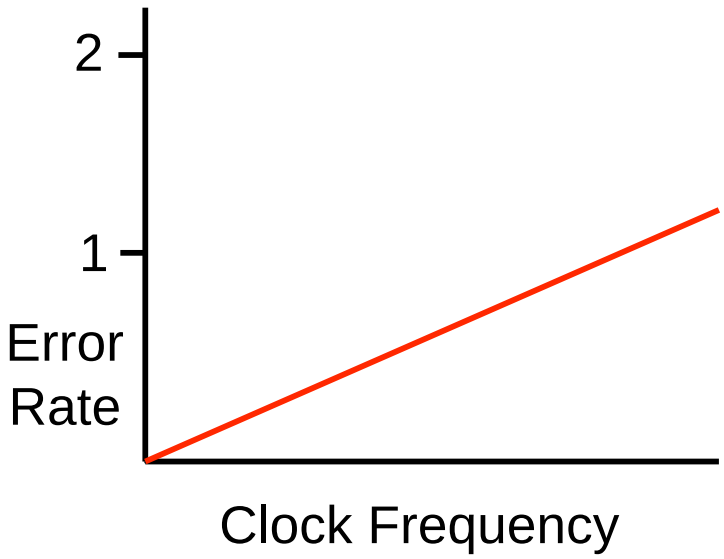
Nominal Supply Voltage of 2.5 V is reduced in steps of 1/100th Volt

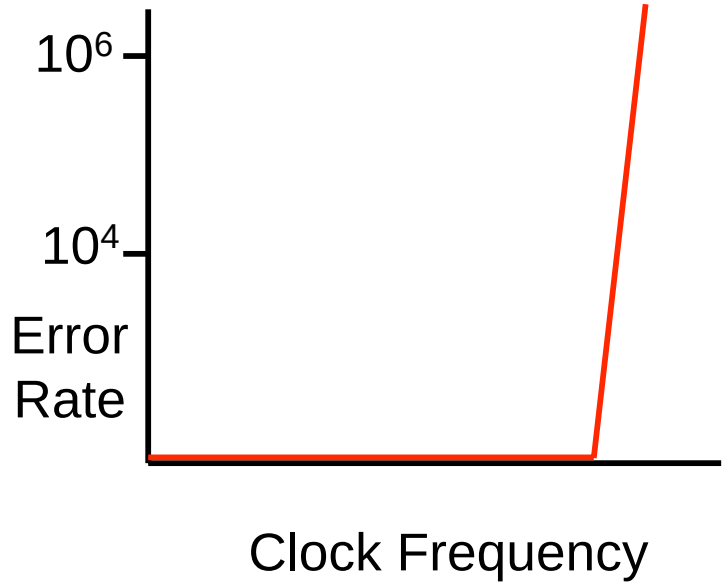
No Data Error was ever Observed at user visible Registers!

Some Remarks on Experiment

- **Possible explanation for the crashes**
  - Control errors are always catastrophic
  - Most Critical Paths are in Control Logic
  - Control Logic fails before ALU datapath
- **Alternative explanation**
  - A large number of transistors affected simultaneously
  - An exponential number of logic paths affected
  - Massive failure in control and data

Outcome of Process Variations





Final Remarks

- **CMOS technology is robust now and will continue to be so for the future**
  - Process Variation related errors must be massive
  - No industry can survive with massive failures
  - Process variations must remain bounded
- **Where does dependability come in?**
  - Perhaps in yield improvement for multi-core microprocessors
  - Perhaps in relaxing design rules for cost and power reduction
  - Early Diagnosis for Yield Leaning


OUT & BACK
RUGGED 7.6
CLEAR LAKE
RUGGED 3
0.0
0.MI
CLEAR POND TRAIL
WARNING!
USE
BIKE TRAIL ONLY!
1201


OUT & BACK TRAIL
RUGGED 7.6 MILE
CLEAR LAKE TRAIL
RUGGED 3 MILE
FOOT RACE
HIKING TRAIL
CLEAR POND TRAIL
WARNING!
BIKERS USE
BIKE TRAIL ONLY!
SIBERIAN EXPRESS
1150
SIBERIAN EXPRESS
866


EXPRESS


SIBERIAN EXPRESS
867


ILLINOIS
1867
UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN
ROUND BARNS
IMAGE: KALEV LEETARU
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