Workshop on
Dependable and Secure
Nanocomputing

Organizers:
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LAAS-CNRS
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UIUC
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TIMA

Thursday June 28, 2007
Nanometric Hardware Technologies

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Increased Performance & New Applications

*but*...

Challenges wrt Dependability and Security

Transient Faults in Operation

[SEUs, power disturbances,...]

Chips with Massively Defective Devices

[low fabrication yield, unpredictability,...]

Hardware Vulnerabilities and Security Threats

[side channel attacks,...]
Motivation and Aims of the Workshop

- **Special Focus on Hardware Issues**
  - Analyze the current status
  - Report on recent advances
  - Forecast the trends

- **Solutions at stake feature many facets**
  - Semiconductor technology
  - Device and chip architecting
  - Basic software
  - High speed communication and networking protocols
  - Resilience techniques
  - Verification and testing
  - Risk assessment
  - …
SRAM FPGA Technology and Automotive Systems

- **Basic Assumptions**
  - Location: Denver, CO, USA ≈ 5,000 feet
  - Technology: 22μm SRAM-based FPGA 1M-gates
  - Prediction (SpaceRad 4.5): $1.05 \times 10^{-4}$ upsets* / day

- **A fleet of 500,000 vehicles, each featuring an airbag control system using this technology**
  - Continuous operation ≈ 52.5 upsets / day
  - *Thus an upset every 27.4 minutes!*
  - Assuming 1 h use per day ≈ 2 upsets / day

* These are firm errors that will persist until the SRAM FPGA is reloaded (normally by power cycling or forcing reconfiguration)

Program Committee

Jacob A. Abraham  University of Texas, Austin, USA
Jacques Collet  LAAS-CNRS, Toulouse, France
Jiri Gaisler  Gaisler Research, Gothenburg, Sweden
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Takashi Nanya  University of Tokyo, Japan
Rubin A. Parekhji  Texas Instruments, Bangalore, India
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Pia Sanda, IBM  Poughkeepsie, NY, USA
Shiuhyung W. Shieh  Nat. Chiao Tung Univ. Hsinchu, Taiwan
Matteo Sonza Reorda  Politecnico di Torino, Italy
Alex Yakovlev, Vivian Zhu  University of Newcastle upon Tyne, UK
Texas Instruments, Dallas, TX, USA
Program Set-up

- 14 submissions
  - Academia: 7
  - Industry: 7

- Selection of contributions by the PC
  - Short presentations
  - Poster presentations

- Invited talks

- Panel
Program-at-a-glance

9h20-10h30 — Invited Talks  
Sudhakar Reddy
Emerging Accidental Faults and Malicious Threats
• Janak Patel, Jean-Jacques Quisquater

11h-13h — Paper Presentations  
Lorena Anghel
From Transient Faults to Architectural Design Issues
• Environmental and Power-Induced Disturbances
• On-Line Testing and Chip-level Configurability

14h-15h30 — Panel  
Johan Karlsson
Emerging Hardware Technologies
and Related Dependability & Security Challenges
• Jacob Abraham, Helena Handschuh, Takashi Nanya, Alex Orailoglu

Coffee Breaks — Poster Presentations
Program-at-a-glance (Revised)

9h15-11h
Emerging Accidental Faults and Malicious Threats

- Invited Talk: Janak Patel
- Paper presentation (1): Cristian Constantinescu,

11h-13h — Paper Presentations (7)

- Palkesh Jain (Rubin Parekhji), Makoto Kimura, Jaume Abella, Rubin Parekhji, Jacques Collet, Peter Klemperer, Giorgio Di Natale

14h-15h30 — Panel
Emerging Hardware Technologies and Related Dependability & Security Challenges

- Jacob Abraham, Helena Handschuh, Takashi Nanya, Alex Orailoglu

Coffee Breaks — Poster Presentations