Development of Dependable Network-on-Chip Platform (3)

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Project summary

- 5.5 year National project (CREST)

- Goal
  - Platform for performing many and various tasks dependably, efficiently and adaptively
  - Demonstration in automotive control system area
Recent cars are equipped with many ECUs

- **Conventional ECU configuration**
Recent cars are equipped with many ECUs
- Centralized ECU approach
Recent cars are equipped with many ECUs
- Centralized ECU approach

Any ECU can access any sensors/actuators
ECUs efficiently used by balancing loads
Tasks continuously executed even if some ECUs become faulty
(i.e., faulty ECU does not result in malfunction of its specific functions)
Backgrounds

- Centralized ECU approach
  - NoC (Network-on-Chip) based
    - Some European projects
  - Multi-Chip NoC based [Yoneda, et al. PRDC2012]
    - Multiple NoCs are connected via off-chip links
      - On-chip networks seamlessly extended to multi-chip networks
    - Advantages
      - Cost-effective: small NoC chips are cheap, and various sizes of configuration are possible (without developing different sizes of NoCs)
      - Chip-level redundancy: tolerate a chip fault
Backgrounds

- Centralized ECU approach
  - NoC (Network-on-Chip) based
    - Some European projects
      - Recomp: Reduced certification costs for trusted multi-core platforms. [http://atc.ugr.es/recomp/](http://atc.ugr.es/recomp/)
      - Race: Robust and reliant automotive computing environment for future ecars. [http://projekt-race.de/](http://projekt-race.de/)
  - Multi-Chip NoC based [Yoneda, et al. PRDC2012]
    - Multiple NoCs are connected via off-chip links
      - On-chip networks seamlessly extended to multi-chip networks
    - Advantages
      - Cost-effective: small NoC chips are cheap, and various sizes of configuration are possible (without developing different sizes of NoCs)
      - Chip-level redundancy: tolerate a chip fault
Outcome

- **Hardware platform**
  - Multi-Chip NoC
    - Fully asynchronous on-chip network
    - Dependable, adaptive, deadlock-free routing
    - Efficient inter-chip communication technology

- **Dependable task execution**
  - Pair & Swap

- **Task allocation**
  - Redundant allocation, redundant scheduling

- **Demonstration of the proposed approach**
  - Practical automotive application
Fault tolerance in Routing level

- When a router goes faulty, a detour path will be taken

[Diagram showing a network with nodes and arrows indicating current position and destination, with annotations for detect the fault and modify the routing.]
Fault tolerance in **Routing level**

- Single chip/router/link fault can be tolerated in each cluster
Dependability in **Processor level**

- **Duplicated execution, comparison, and pair-reconfiguration**

  Compare Task A results

  Task A executed by this pair

  Compare Task B results

  Task B executed by this pair
Pair & Swap

- Duplicated execution, comparison, and pair-reconfiguration

Tasks are redundantly loaded in several cores
Task allocation

Simulink model

Atomic sub-function

Simulink model

Task graph generation

Embedded Coder

C code

Complier

Parameters

Multiplicities for scheduling and allocation

NoC model

Upper bound of failed nodes

Task graph

Multi-Task Scheduling and Allocation

Enumeration of failure patterns

Failure patterns

Scheduling and allocation result

Upper bound of failed nodes
Task allocation

Task graph

- UnitDelay
- Sum
- Sub
- Gain1
- Product
- Sat
- Voltage
- Gain2
- Gain3
- UnitDelay1
- Error
- Sum
- Gain
Task allocation

Task graph
Task allocation

Tasks are allocated to CPU cores redundantly

- p0
  - T1
  - T2
  - T3
  - T4
- p1
  - T1
  - T2
  - T3
  - T4
- p2
  - T1
  - T2
  - T3
  - T4
- p3
  - T1
  - T2
  - T3
  - T4
Task scheduling

Duplicated execution and comparison
Demonstration

- **Automotive Application**
  - Integrated attitude control system for a four-wheel drive car
    - Torque, brake, and steering control of 4 wheels performed by ECUs
  - Highly cooperative process needed by each ECU
    - Integrated Control ECU
    - 2 Electric Power Steering Control ECUs
    - Brake Control ECU
    - Battery Management ECU
Demonstration

- Automotive Application
  - Integrated attitude control system for a four-wheel drive car
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Demonstration

- Characteristics of this application
  - Stopping control is very dangerous
    - Higher availability is required
Experimental system

Base chip × 4

HILS (Hardware In the Loop Simulation) system

Base chip

Routers

H.W. accelerator

V850E CPU core

FPGA

PC

External IO

D/A・A/D・etc

Engine

Drivetrain

Vehicle Dynamics

Environment
Ongoing work

- **Evaluation kit**
  - Evaluation board
    - Dependable NoC platforms
      - 4 Multi-Chip ASICs
      - Vertex7(XC7VLX690T)
    - HILS interface
  - Pseudo HIL-plant models (executable on PC)
  - Redundant task allocation tool
    - Input: (Simplex) Simulink model for application
    - Output: Executable codes for redundant cores
Summary

- Provide a platform such that
  - Required dependability can be obtained by simply
    - connecting base-chips, and
    - allocating tasks redundantly
  - User just needs to prepare a simplex version of an application program