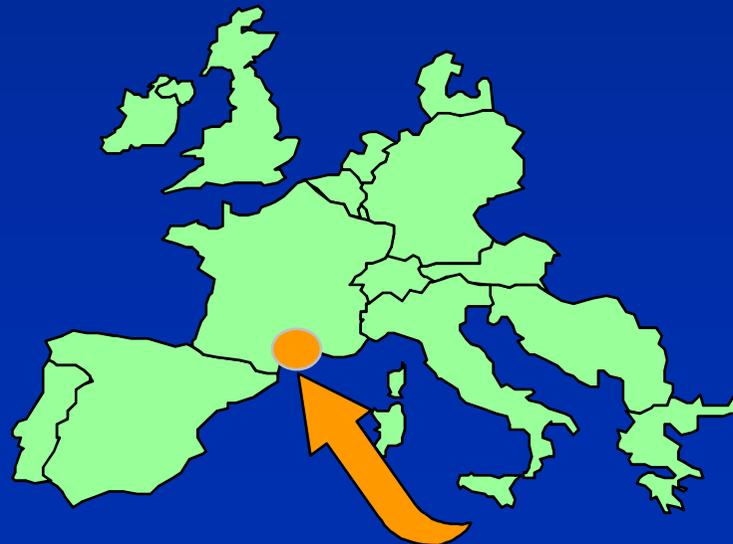


Testing for Realistic Defects in CMOS Technology: From a Deterministic to a Statistical View

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LIRMM - CNRS / University of Montpellier - FRANCE



Outline

□ Past

- 1. Classical FM

- 2. Defect with Realistic FM

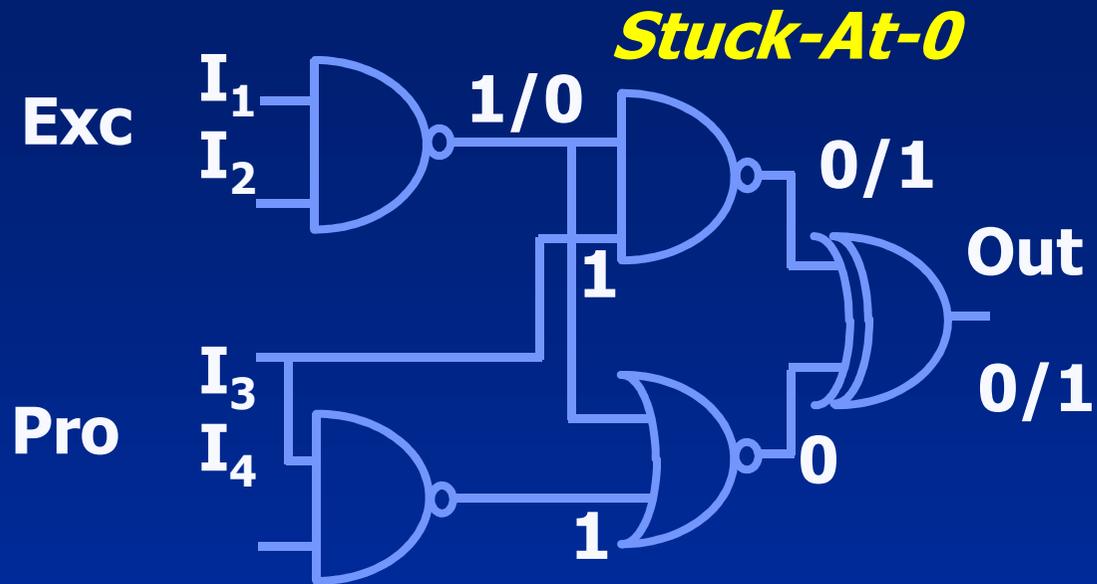
□ Today

- 3. Defect with Probabilistic DM

□ Future

- 4. Defect with Statistical Chip

1. Classical FM



Short

Open

Transistor

-

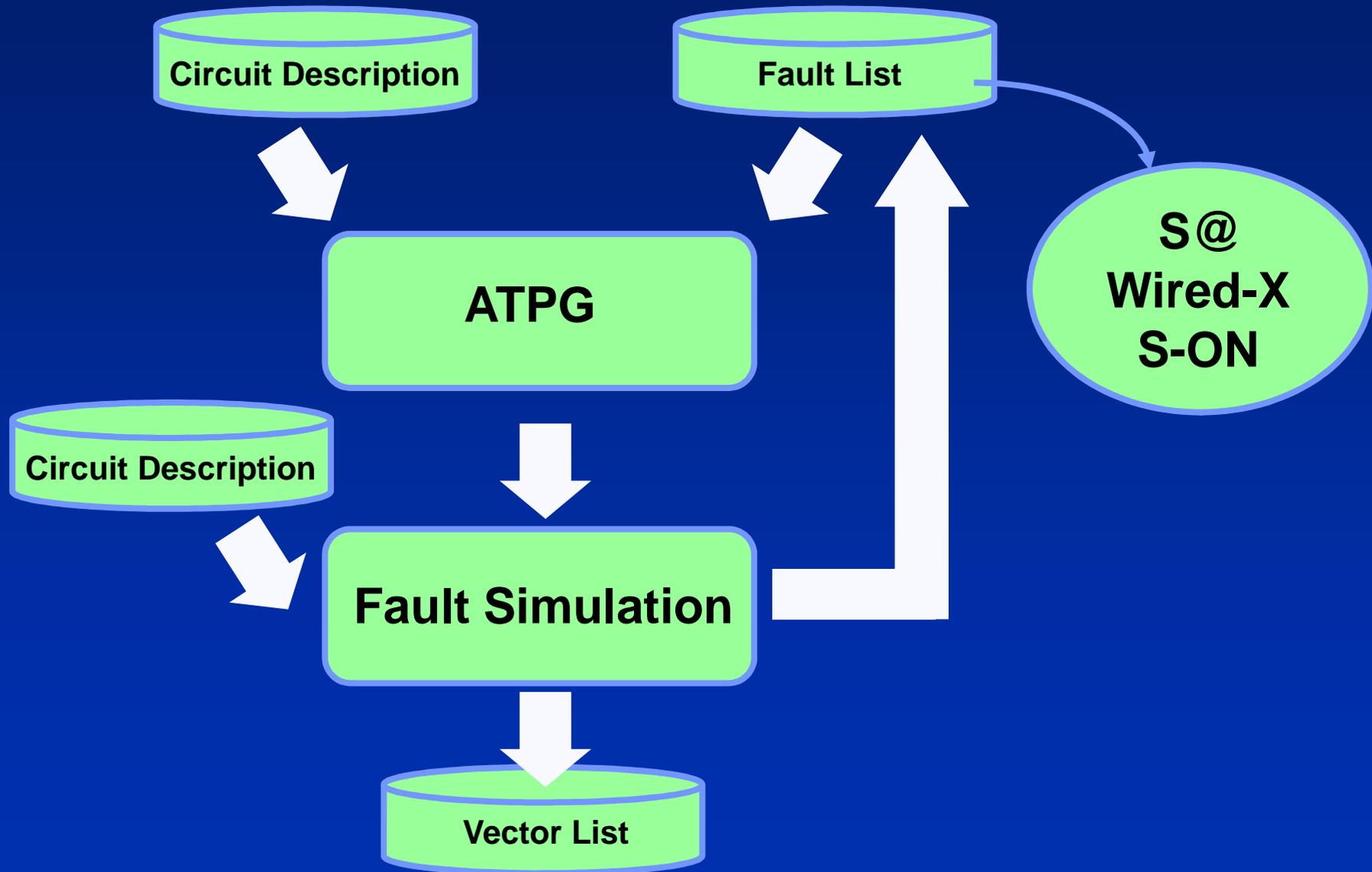
Stuck-Open

Interconnect

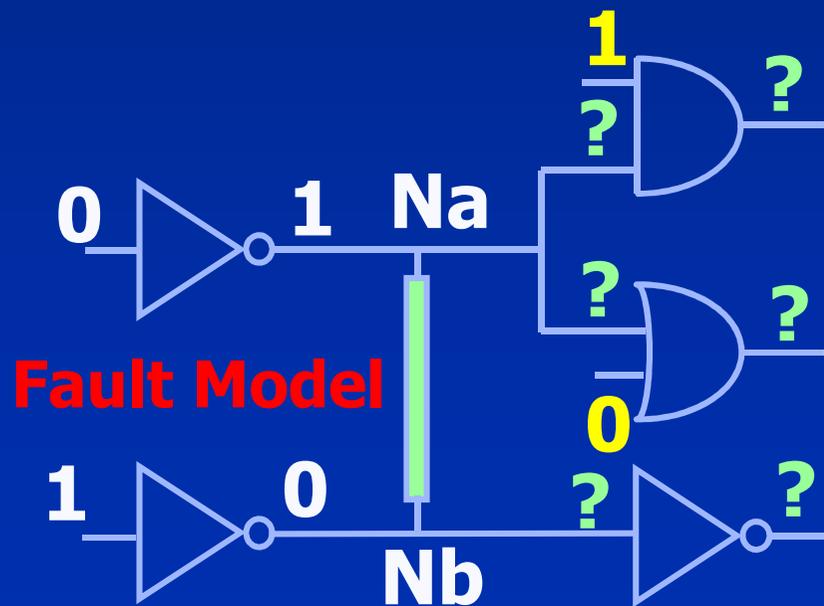
Wired-X

-

1. Classical FM

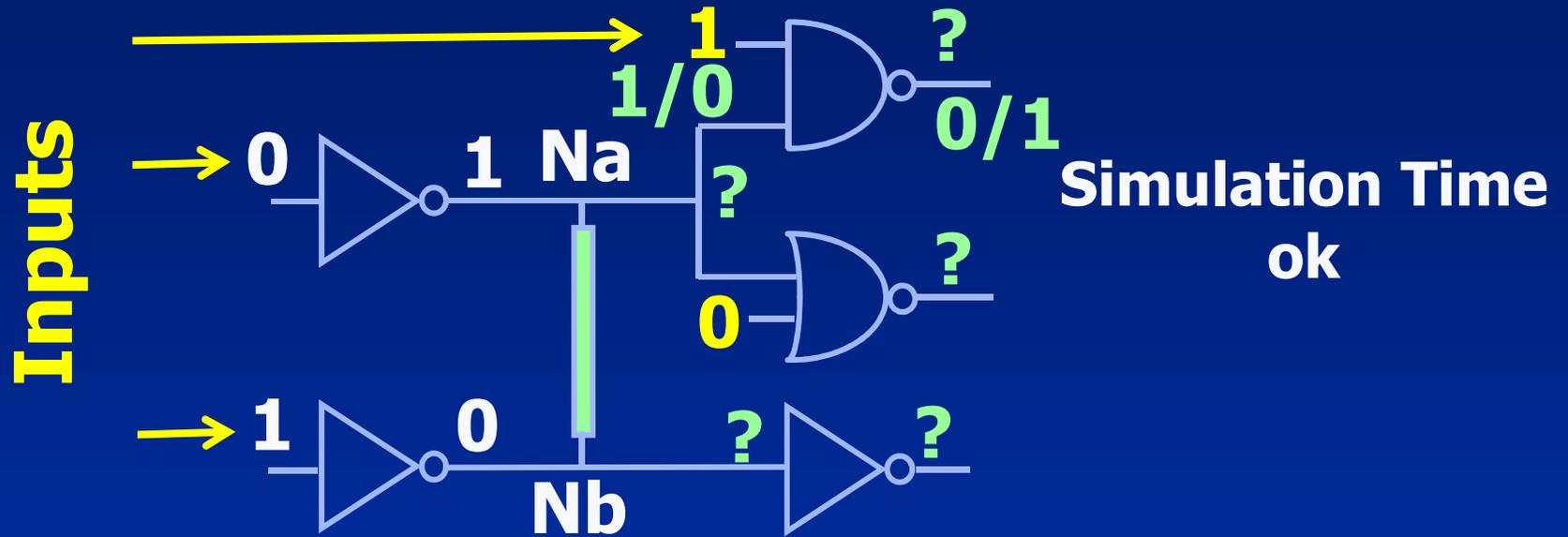


1. Classical FM



| Na | Nb | Na* | Nb* |
|----|----|-----|-----|
| 0 | 0 | 0 | 0 |
| 0 | 1 | ? | ? |
| 1 | 0 | ? | ? |
| 1 | 1 | 1 | 1 |

1. Classical FM



Wired-And

| Na | Nb | Na.Nb |
|----|----|-------|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Dominant

| Na | Nb | Na |
|----|----|----|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

Wired-Or

| Na | Nb | Na+Nb |
|----|----|-------|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

1. Classical FM

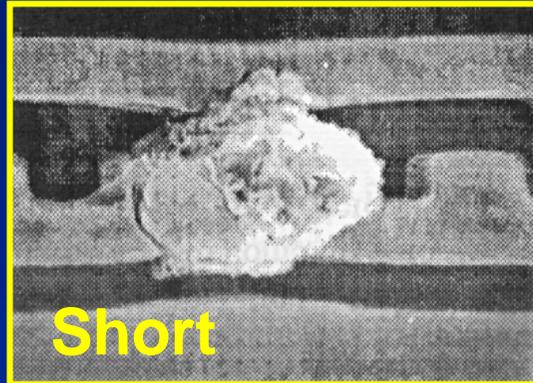
Classical Fault Model

Controlled

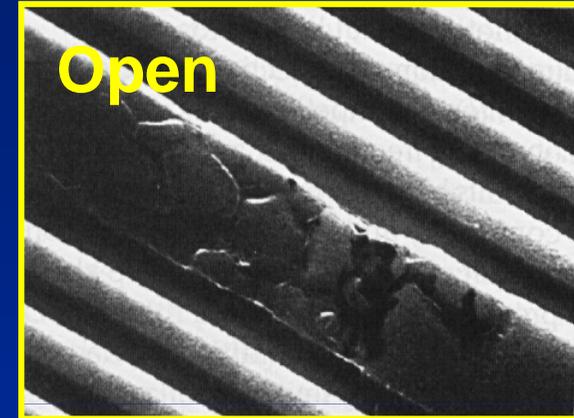


CFM

2. Defect with Realistic FM

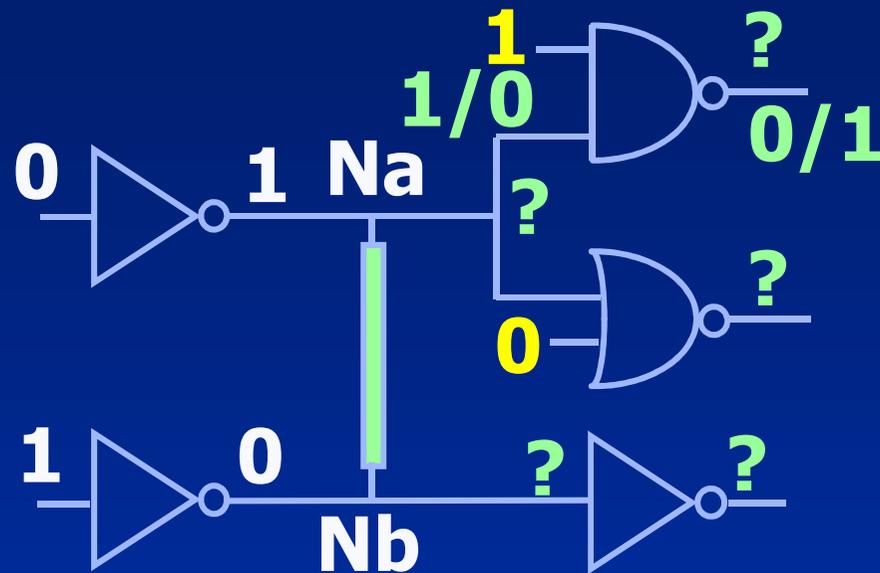


Defects



| | Short | Open |
|--------------|-------------------------|----------------------|
| Transistor | <i>Gate-Oxide-Short</i> | <i>Floating Gate</i> |
| Interconnect | <i>Short</i> | <i>Open</i> |

2. Defect with Realistic FM



Wired-And

| Na | Nb | Na.Nb |
|----|----|-------|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Dominant

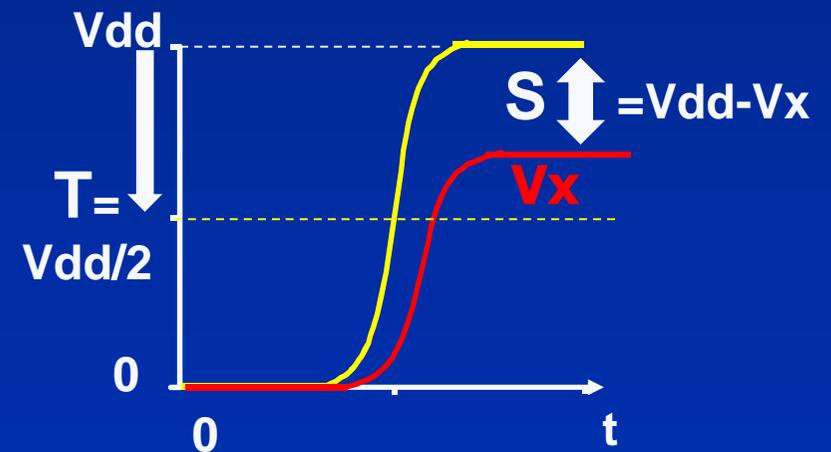
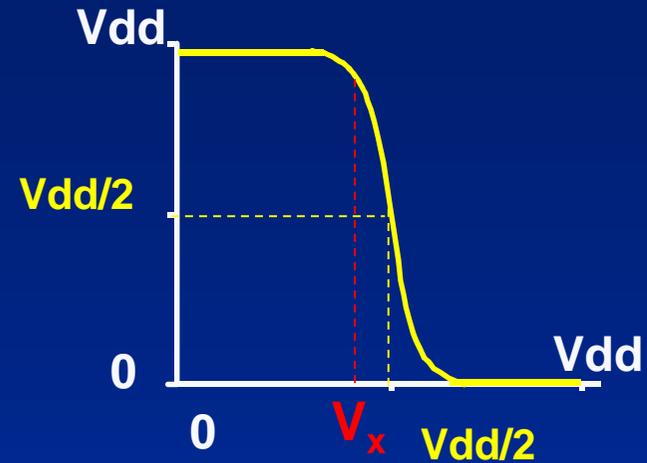
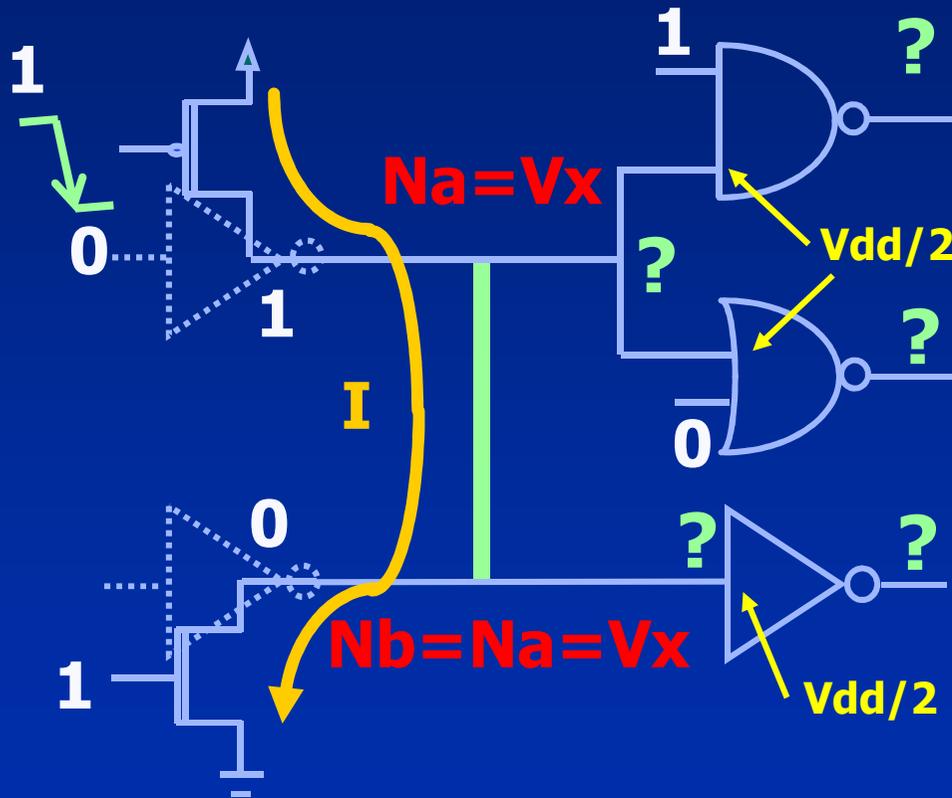
| Na | Nb | Na |
|----|----|----|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

Wired-Or

| Na | Nb | Na+Nb |
|----|----|-------|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

2. Defect with Realistic FM

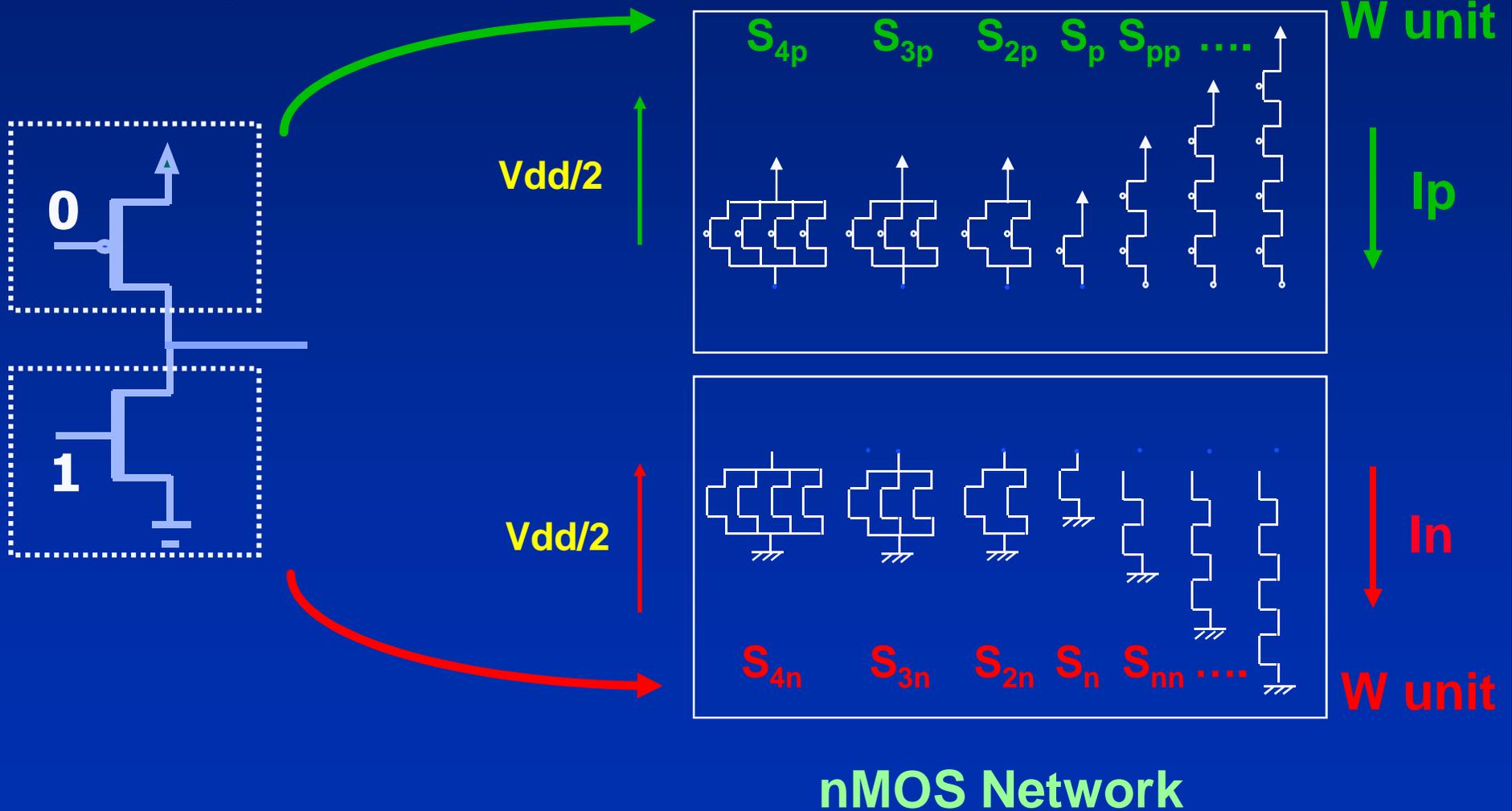
• Voting



Defect Detection: Size > Threshold

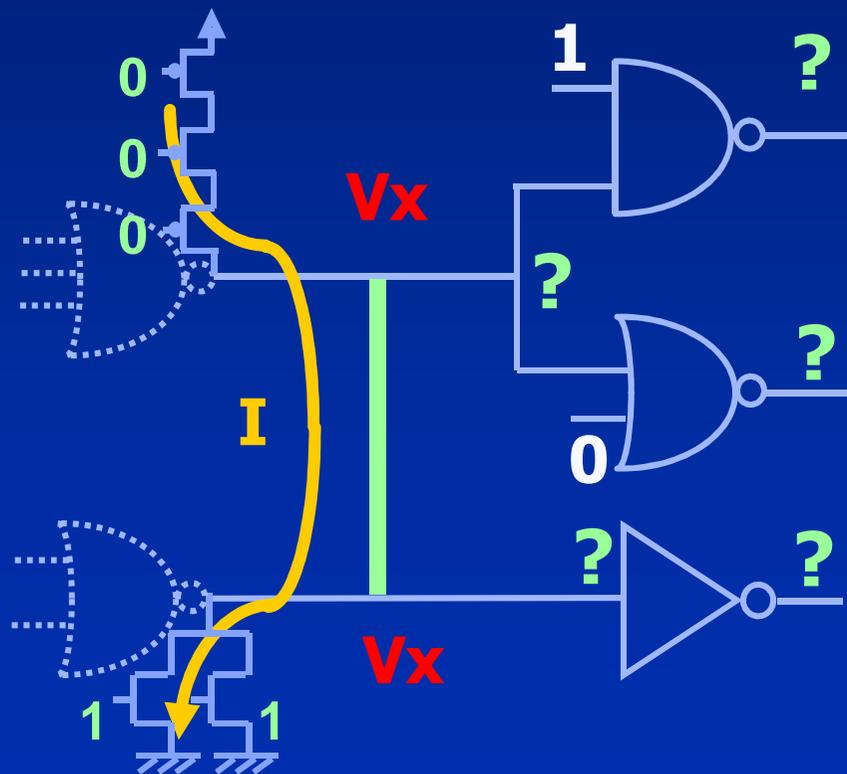
2. Defect with Realistic FM

- Voting



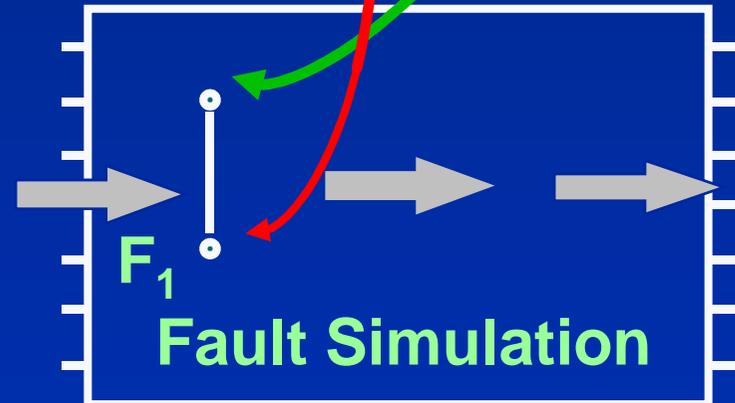
2. Defect with Realistic FM

- Voting



Pre-SPICE Table

| | | | | | |
|----------|----------|----------|-------|----------|-----------|
| S_{4p} | S_{3p} | S_{2p} | S_p | S_{pp} | S_{ppp} |
| S_{4n} | S_{3n} | S_{2n} | S_n | S_{nn} | S_{nnn} |



2. Defect with Realistic FM

Classical FM

Controlled

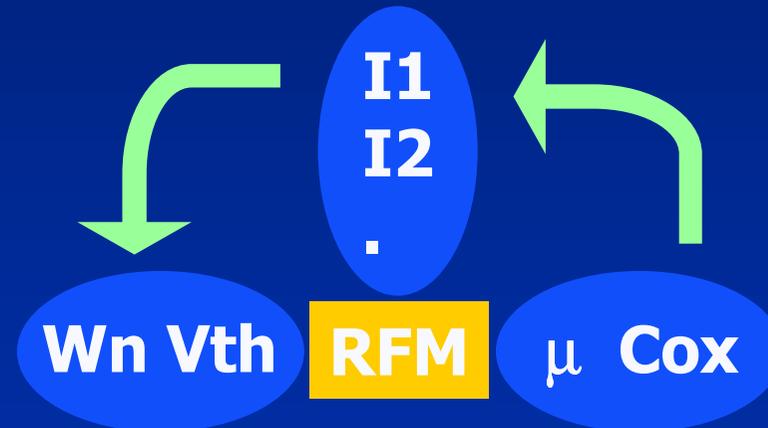


Size is Maximum

-

Realistic FM

Controlled

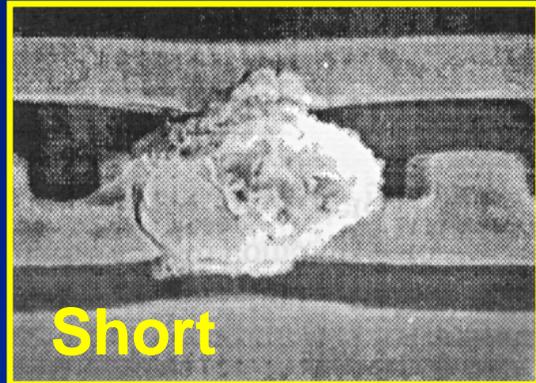


Induced

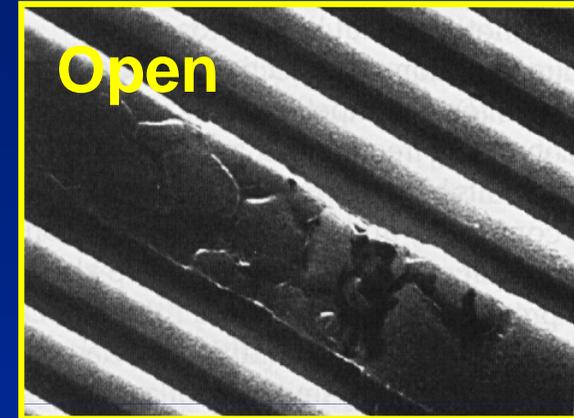
Imposed

Compute Size
Compare Threshold

3. Defect with Probabilistic FM



Defects



Short

Open

Transistor

Gate-Oxide-Short

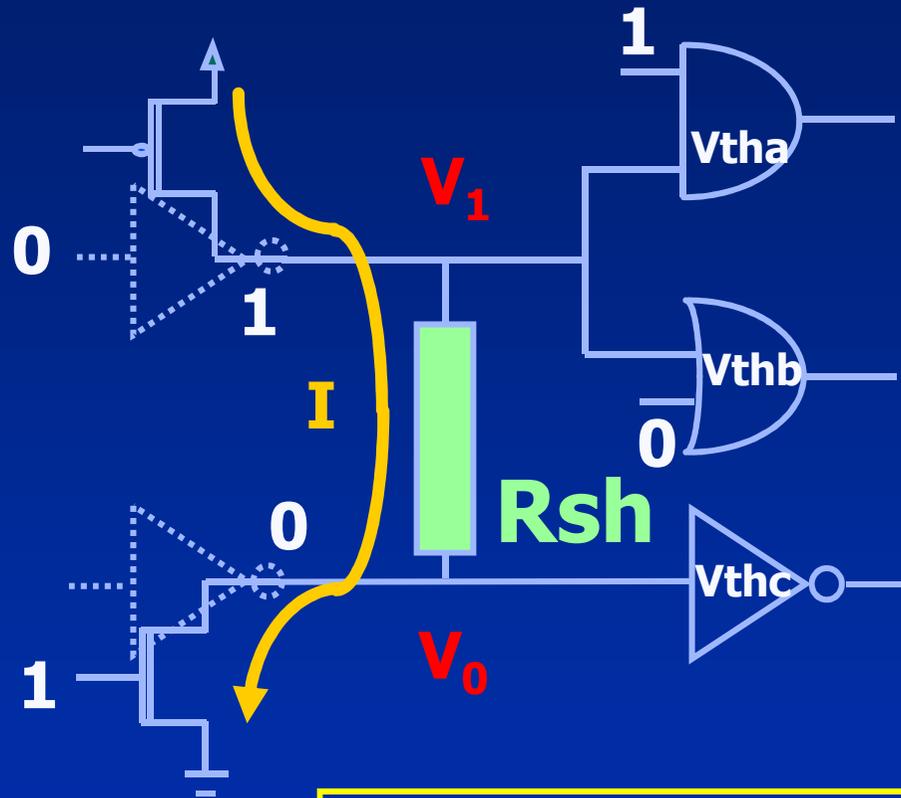
Floating Gate

Interconnect

Resistive Short

Resistive Open

3. Defect with Probabilistic FM



Defects are Unpredictable

?

$$V_x = F(R_{sh})$$

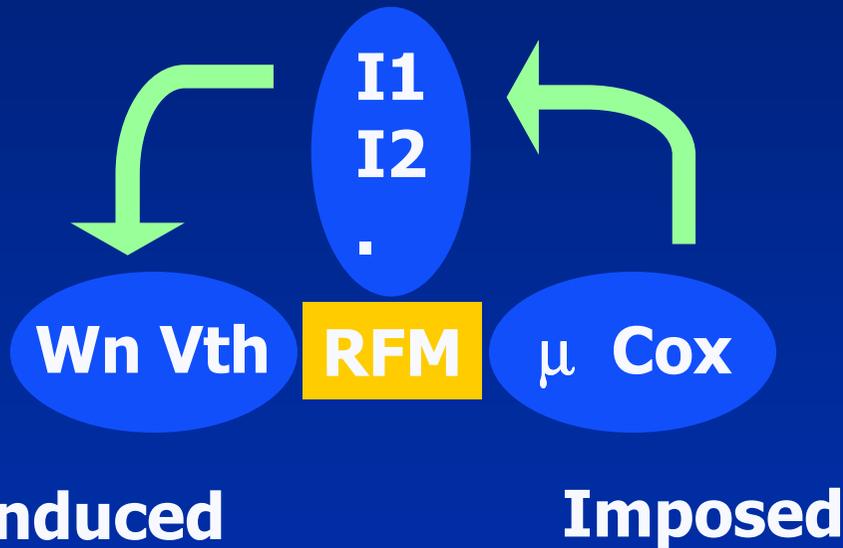
$\beta \quad V_{tp} \quad V_{tn} \quad C_{ox} \quad \mu_p \quad \mu_n \quad V_{dd}$

Topology
Technology

3. Defect with Probabilistic FM

Realistic FM

Controlled

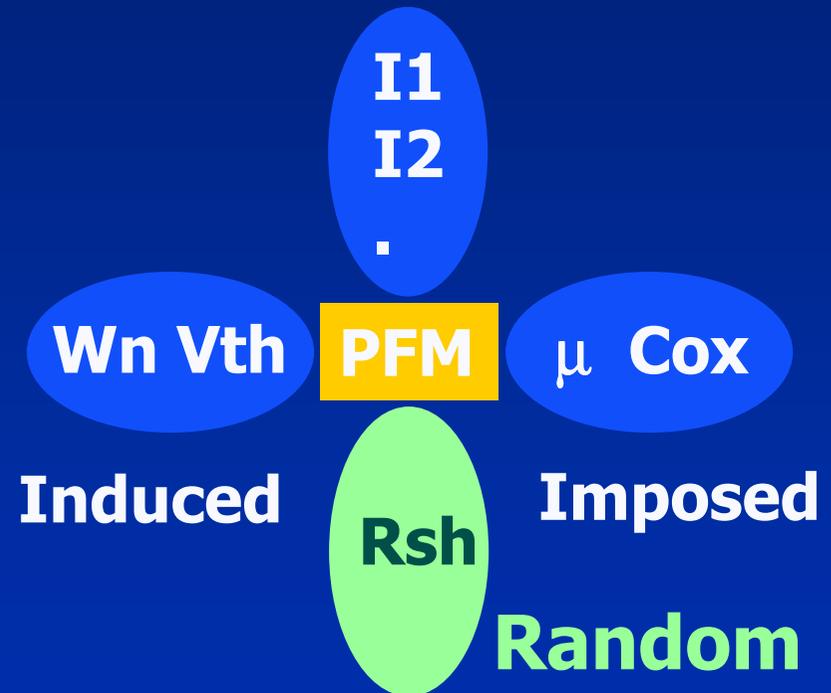


Compute Size
Compare Threshold

$R_{sh}=0$
 $R_{op}=\infty$

Probabilistic FM

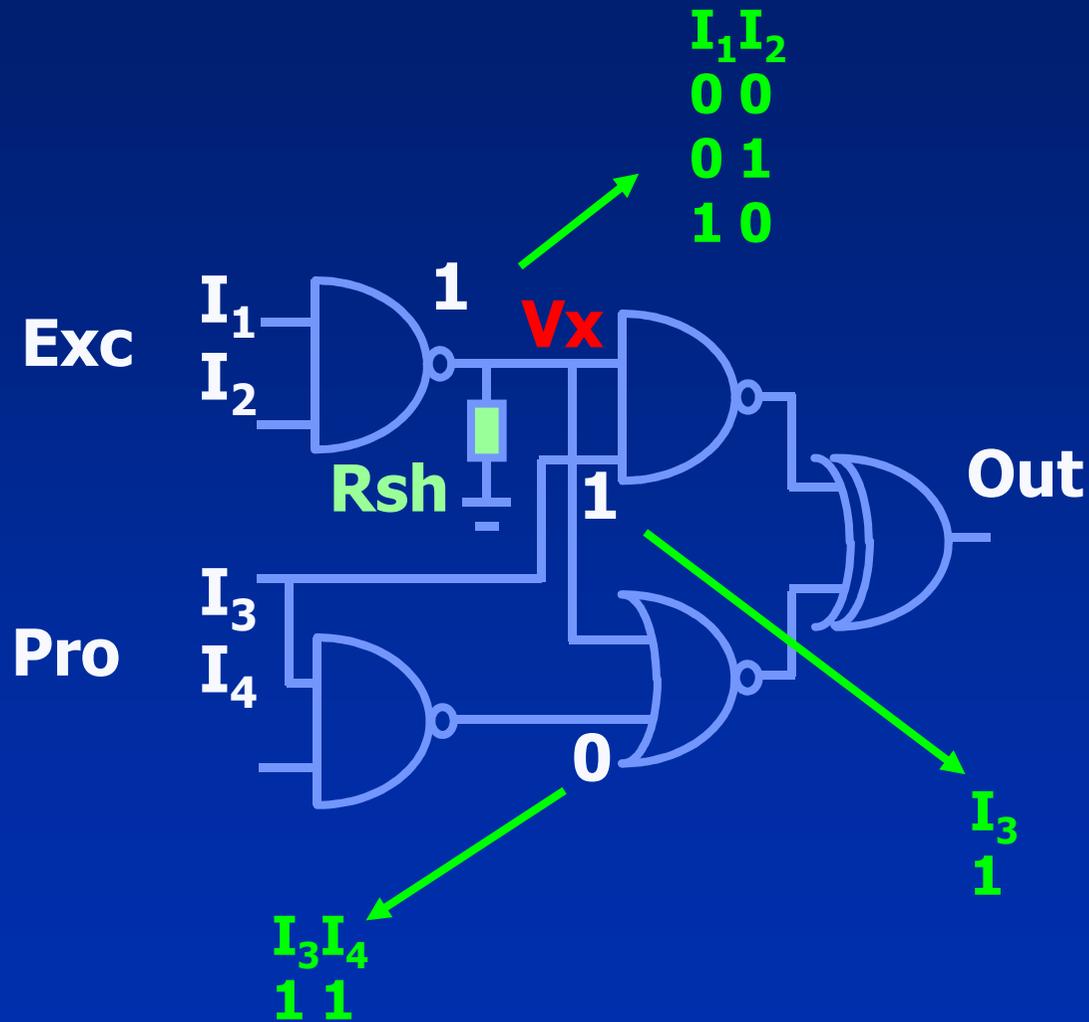
Controlled



Size (P) ?
Compare Threshold

$R_{sh}?$
 $R_{op}?$

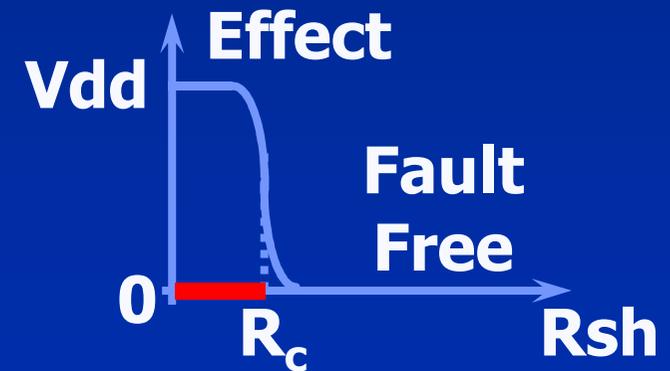
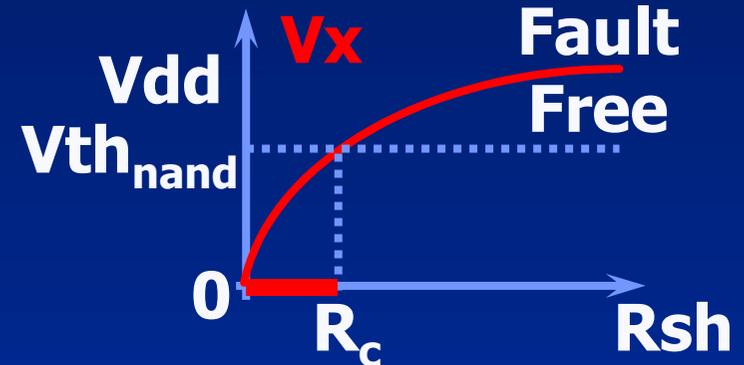
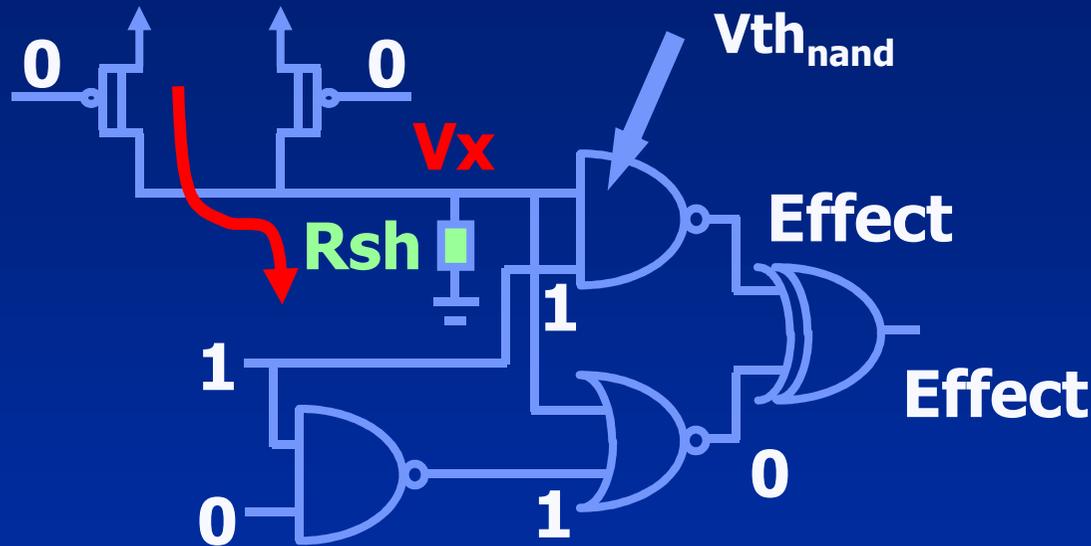
3. Defect with Probabilistic FM



| | $I_1 I_2$ | $I_3 I_4$ |
|-----|-----------|-----------|
| #0 | 0 0 | 0 0 |
| #1 | 0 0 | 0 1 |
| #2 | 0 0 | 1 0 |
| #3 | 0 0 | 1 1 |
| #4 | 0 1 | 0 0 |
| #5 | 0 1 | 0 1 |
| #6 | 0 1 | 1 0 |
| #7 | 0 1 | 1 1 |
| #8 | 1 0 | 0 0 |
| #9 | 1 0 | 0 1 |
| #10 | 1 0 | 1 0 |
| #11 | 1 0 | 1 1 |
| #12 | 1 1 | 0 0 |
| #13 | 1 1 | 0 1 |
| #14 | 1 1 | 1 0 |
| #15 | 1 1 | 1 1 |

3. Defect with Probabilistic FM

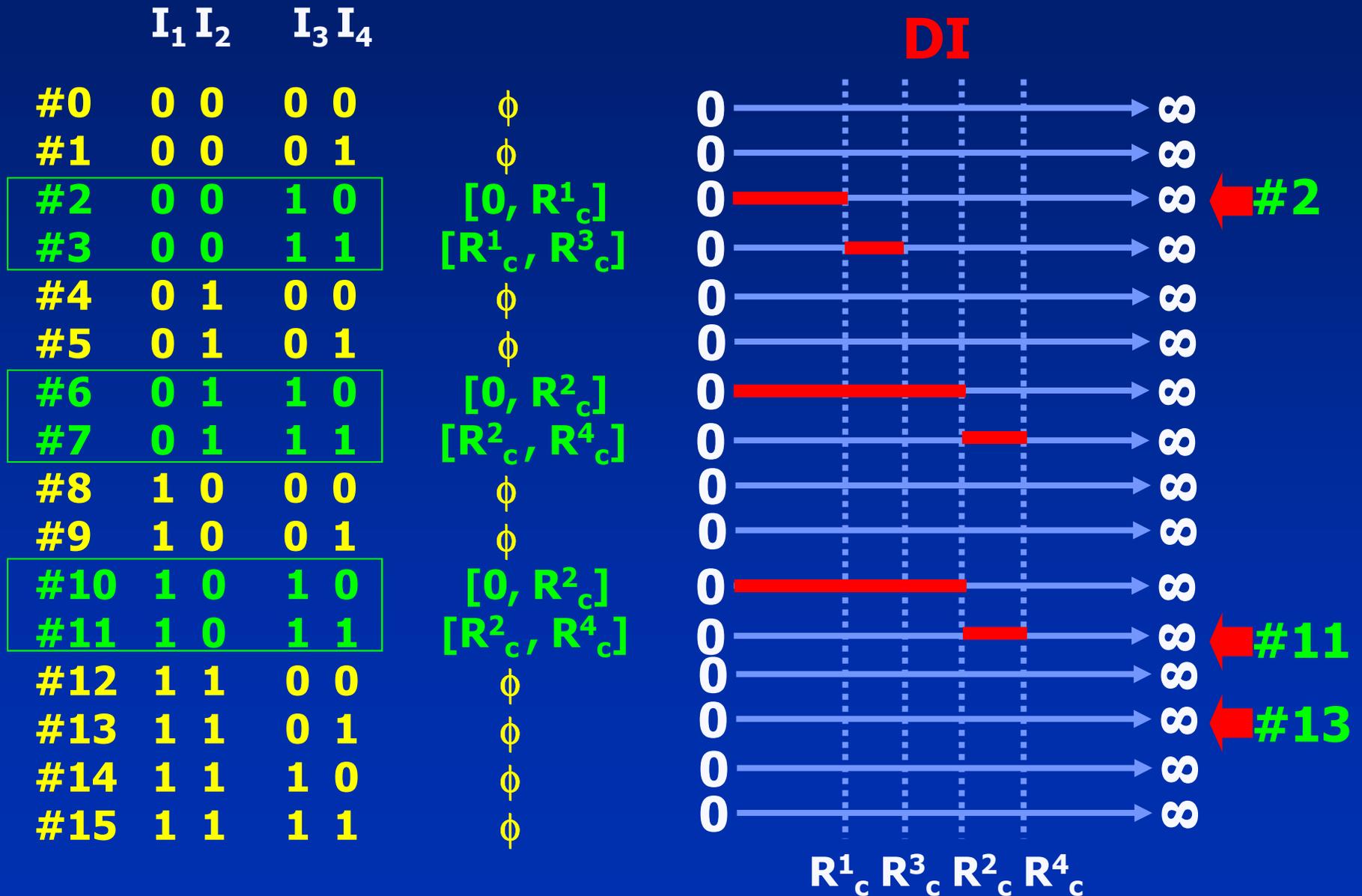
Vector #2



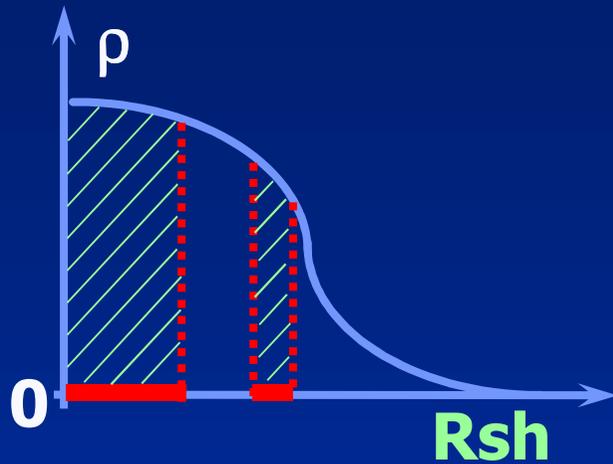
Defect is Detected
If $R_{sh} \in [0 , R_c]$

$$DI = [0 , R_c]$$

3. Defect with Probabilistic FM

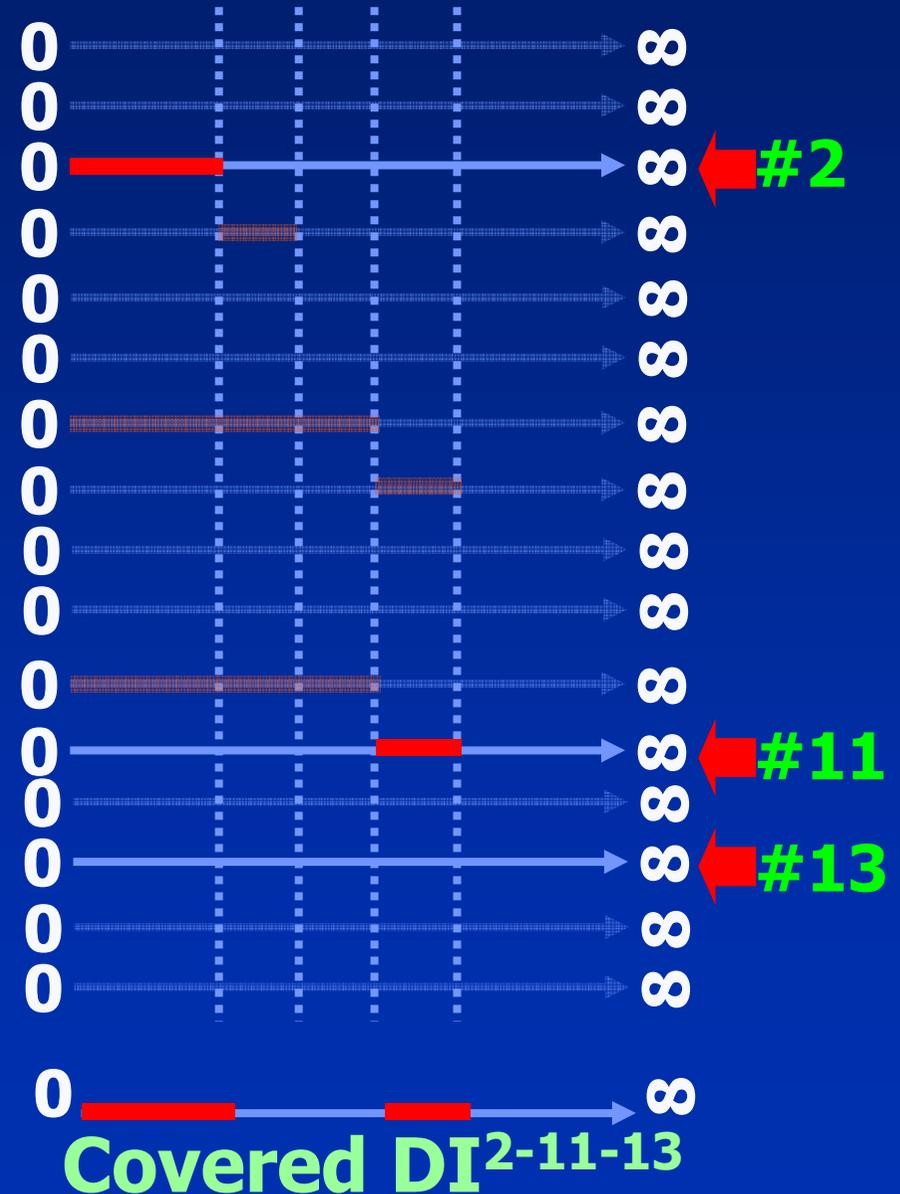


3. Defect with Probabilistic FM

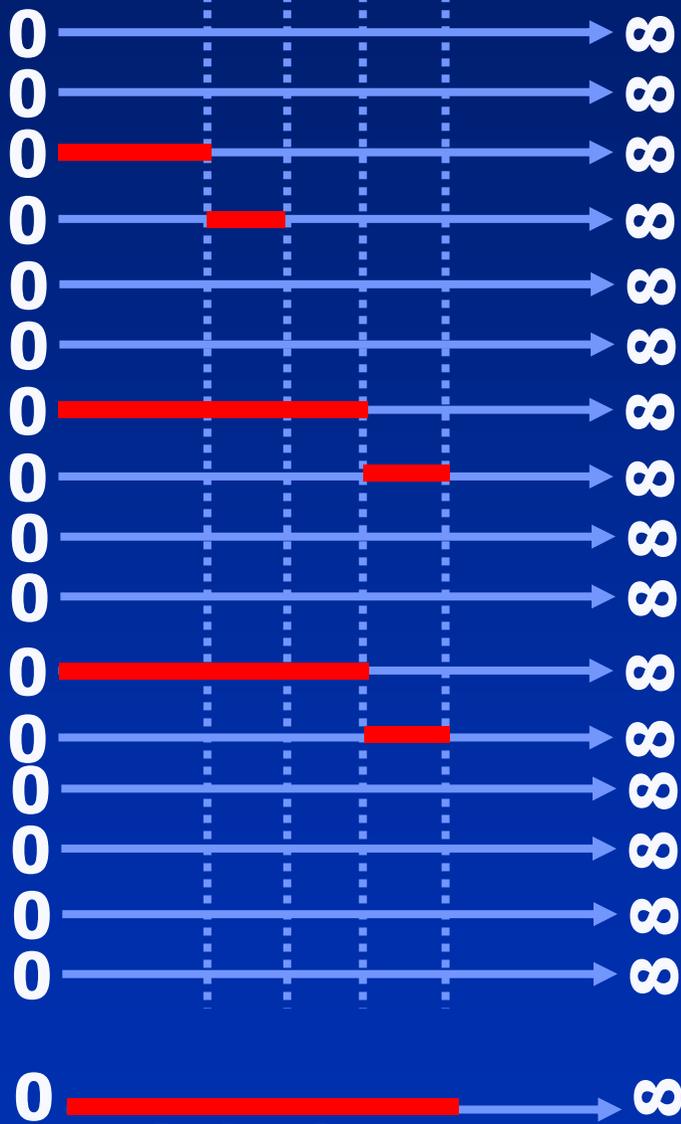


To know or not to know ?

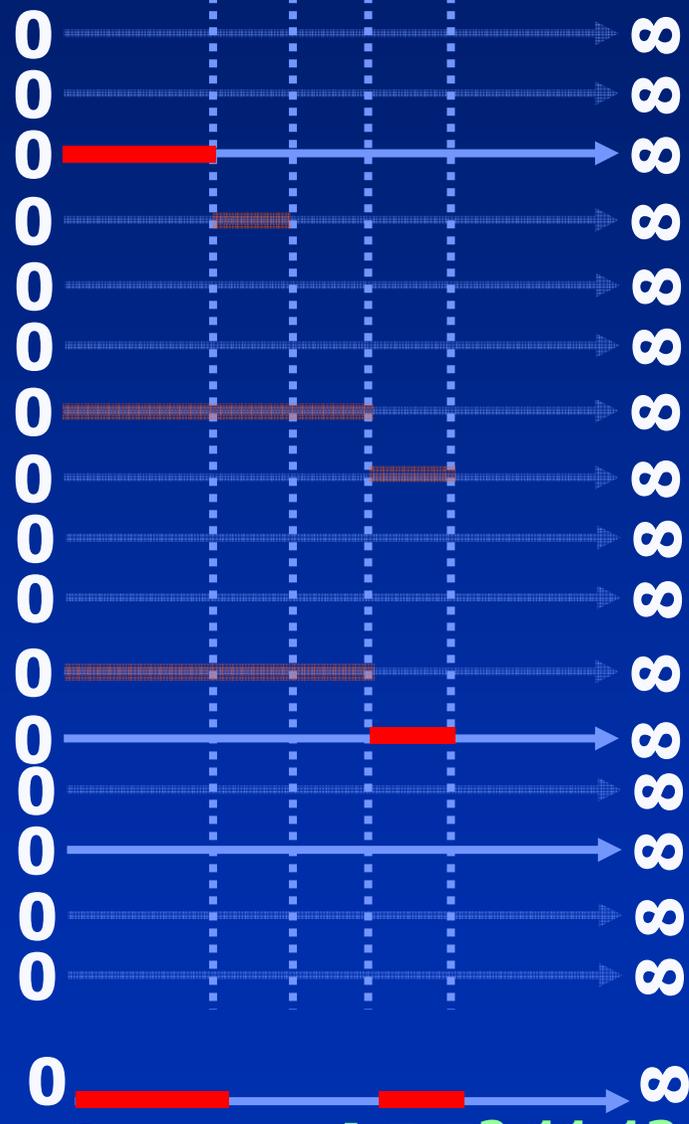
$$P_D = \int_{C-DI_D} \rho(Rsh) dRsh$$



3. Defect with Probabilistic FM



Global DI



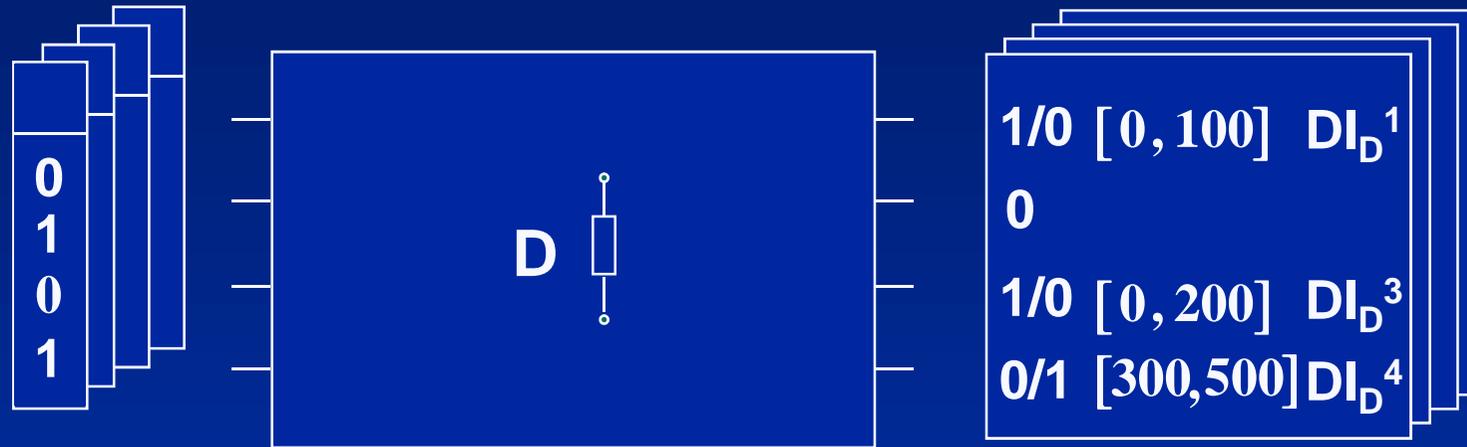
Covered DI²⁻¹¹⁻¹³

3. Defect with Probabilistic FM



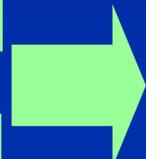
$$E_D = \frac{C-DI}{G-DI} = \frac{\int_{C-DI_D} \rho(Rsh) dRsh}{\int_{G-DI_D} \rho(Rsh) dRsh}$$

3. Defect with Probabilistic FM



$$C-DI_D = \bigcup_{V_i} \bigcup_{PO_i} DI_D$$

$$G-DI_D = \bigcup_{V_{2^n}} \bigcup_{PO_i} DI_D$$



$$E_D = \frac{\int_{C-DI_D} \rho(Rsh) dRsh}{\int_{G-DI_D} \rho(Rsh) dRsh}$$

3. Defect with Probabilistic FM

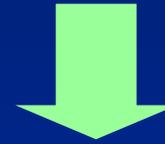
Classical FM
Realistic FM



$$FC = \frac{\sum E_F}{N_F}$$

$$E_F = \begin{cases} 0 \\ 1 \end{cases}$$

Probabilistic FM



$$FC = \frac{\sum E_D}{N_D}$$

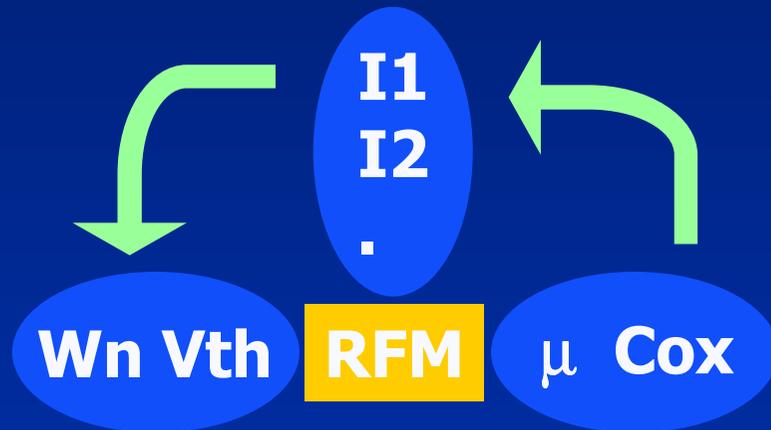
$$0 < E_D < 1$$

$$\frac{\int C-DI_D}{\int G-DI_D}$$

3. Defect with Probabilistic FM

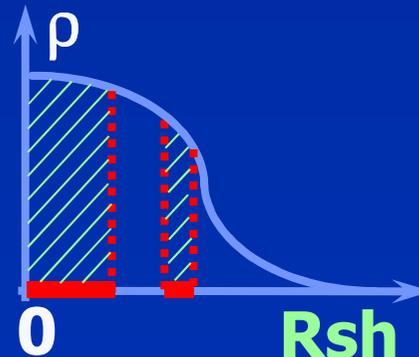
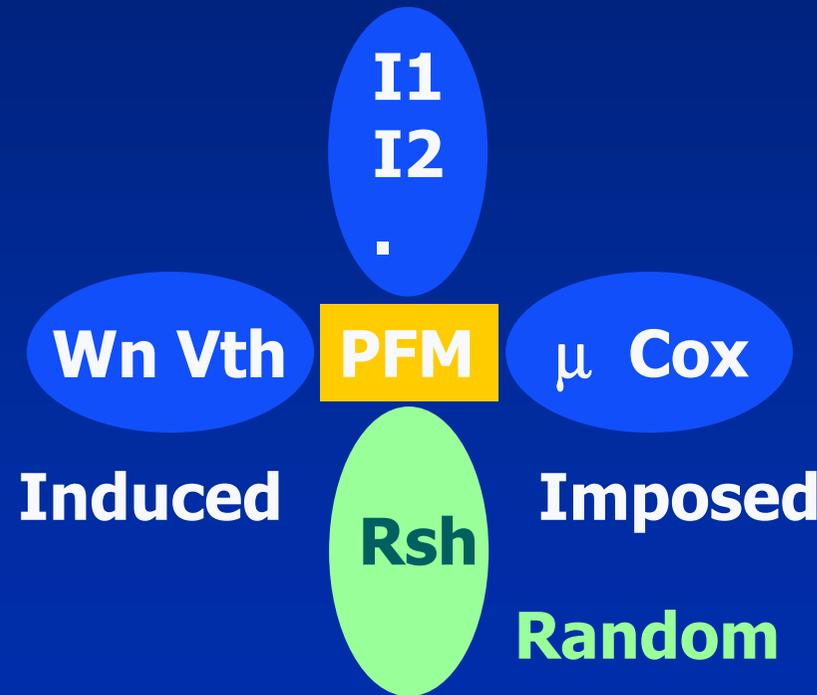
Realistic FM

Controlled



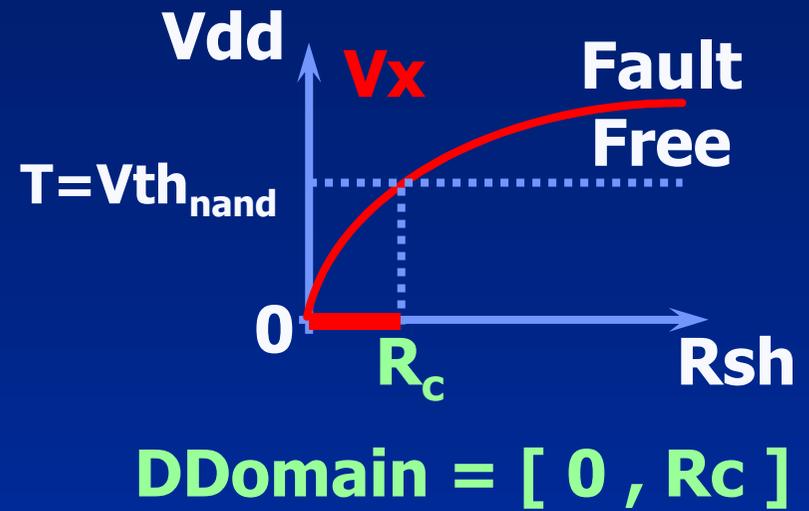
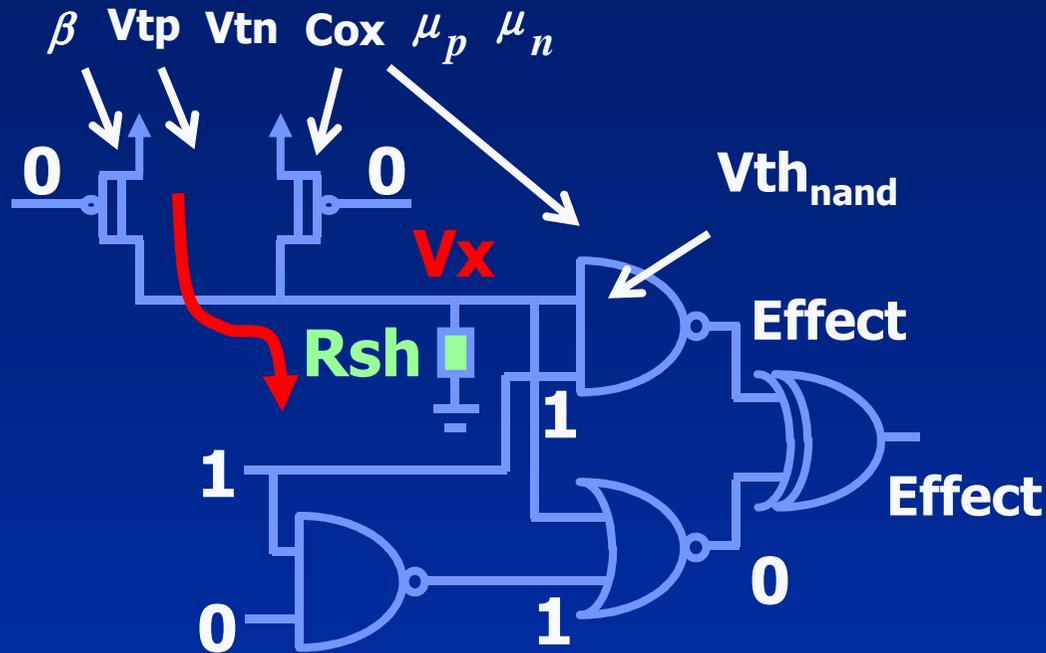
Probabilistic FM

Controlled

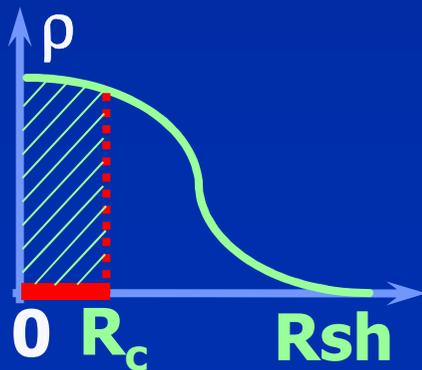


Size (P) => PDF
Threshold => DDomain

4. Defect with Statistical Chip



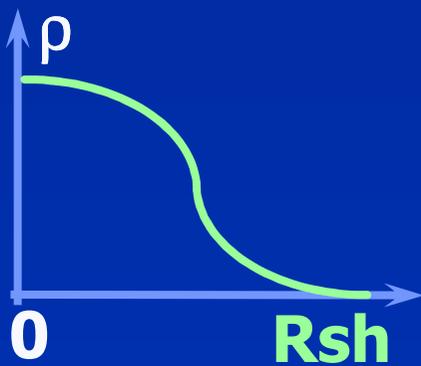
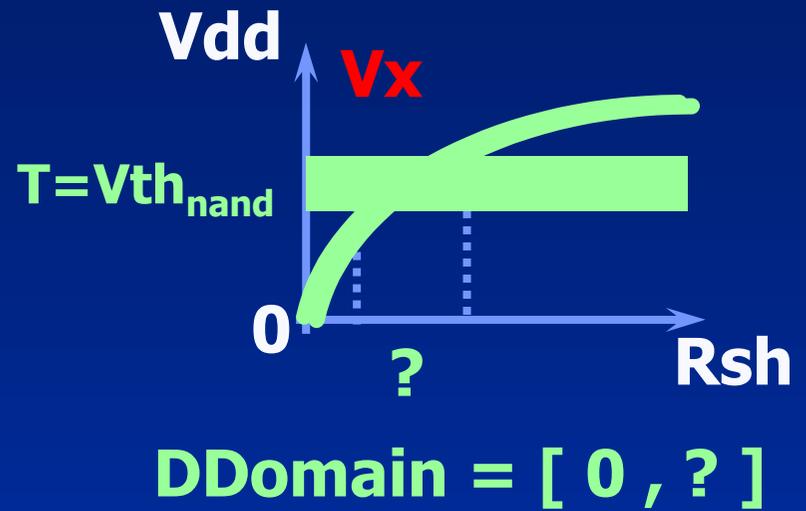
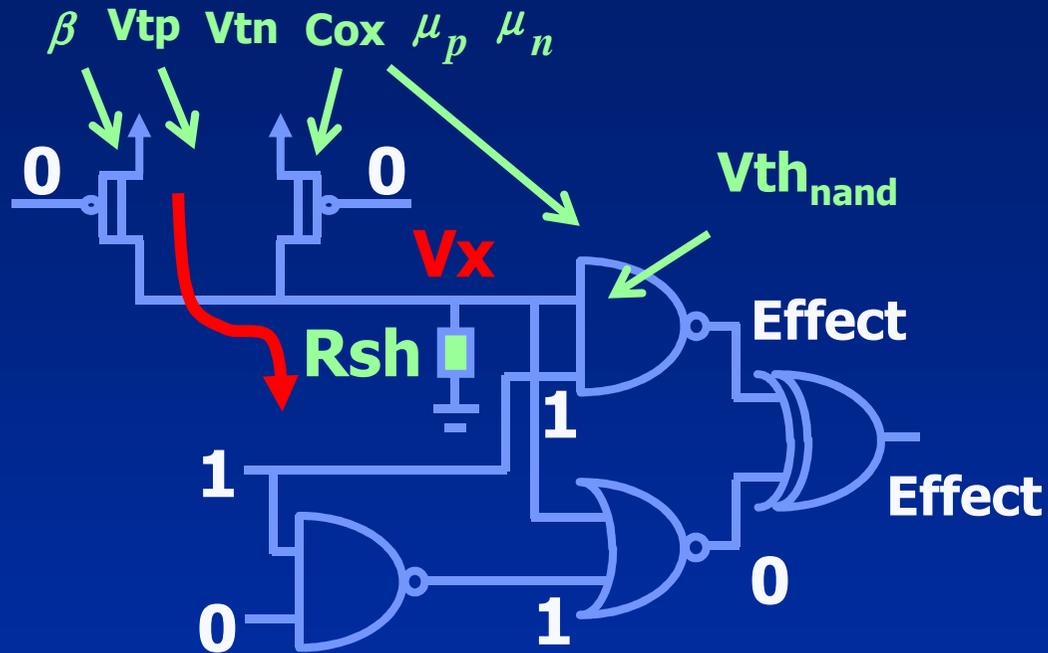
Size (P) \Rightarrow PDF
 Threshold \Rightarrow DDomain



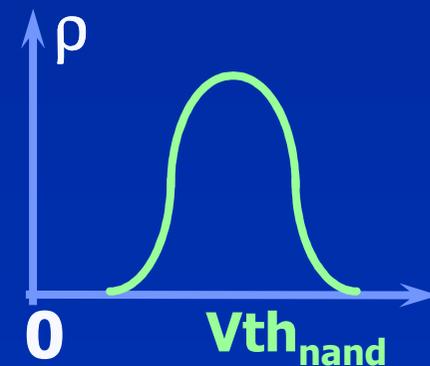
$$V_x = F(R_{sh})$$

β V_{tp} V_{tn} C_{ox} μ_p μ_n V_{dd}

4. Defect with Statistical Chip

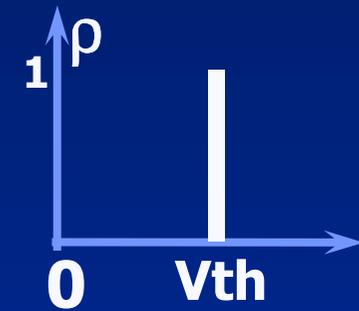
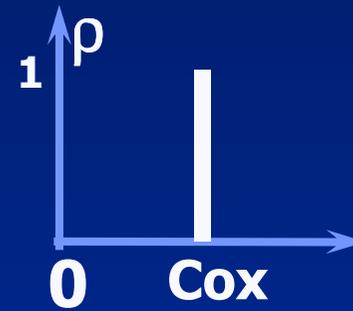
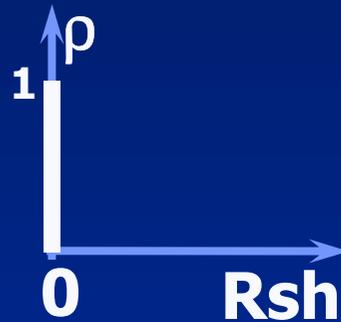


Size (P) \Rightarrow PDF
 Threshold \Rightarrow PDF

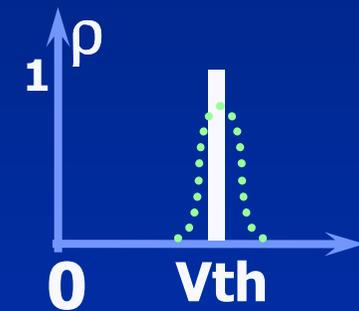
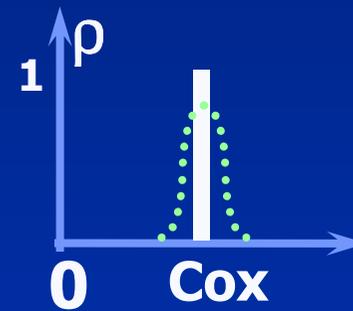
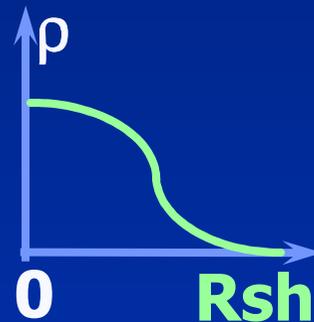


4. Defect with Statistical Chip

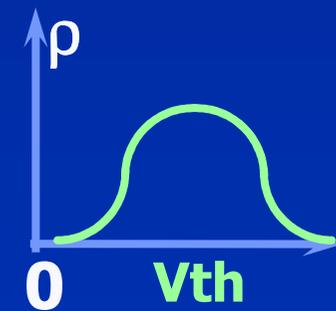
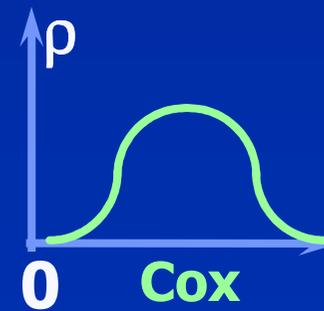
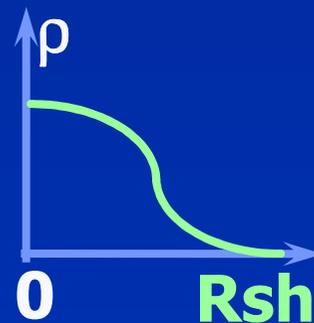
Realistic FM



Probabilistic FM



Statistical Chip



4. Defect with Statistical Chip

Probabilistic FM

Controlled

I1
I2
.

Wn Vth

PFM

μ Cox

Induced

Rsh

Imposed

Random

Size (P) => PDF
Threshold => DDomain

Statistical Chip

Controlled

I1
I2
.

Wn Vth

PFM

μ Cox

Rsh

Random

P(Size > Threshold)
Size (P1,P2,...)
Threshold(P1,P2,...)

Conclusion

□ Past

- 1. Classical FM → Chip Det / Fault Det
- 2. Realistic FM → Chip Det / Def Det

□ Today

- 3. Probabilistic FM → Chip Det / Def Stat

□ Future

- 4. Statistical Chip → Chip Stat / Def Stat