# Development of Dependable Network-on-Chip Platform (2)

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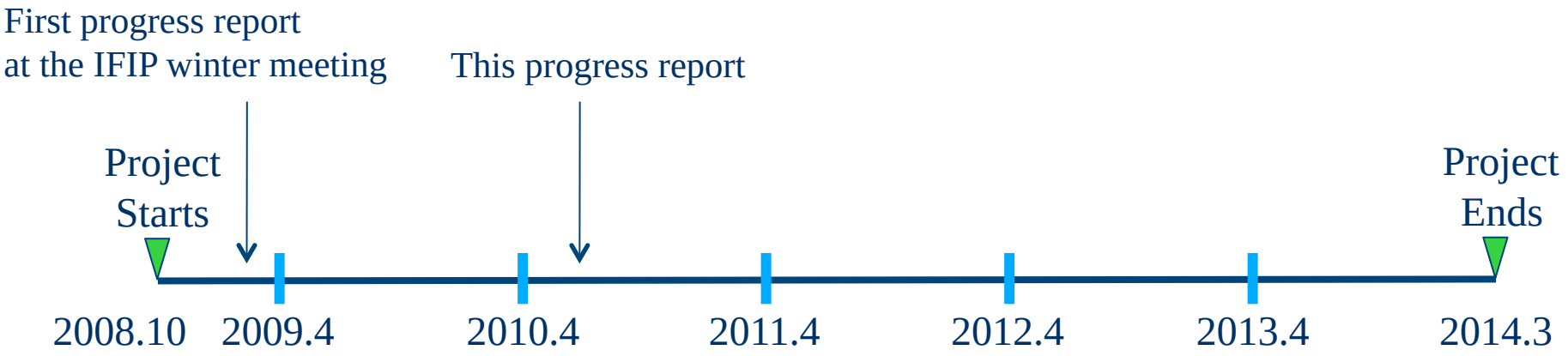
# Project summary

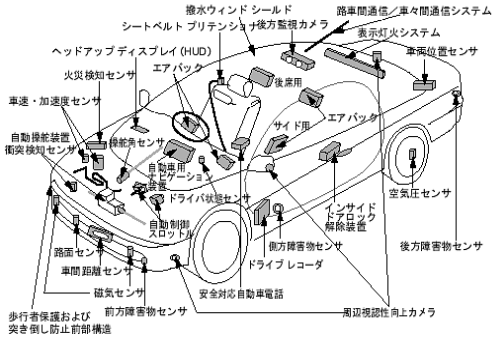
- 5.5 year National project (CREST)




- Goal
  - Platform for performing many and various tasks in one chip dependably, efficiently and adaptively
  - Demonstration in automotive control system area

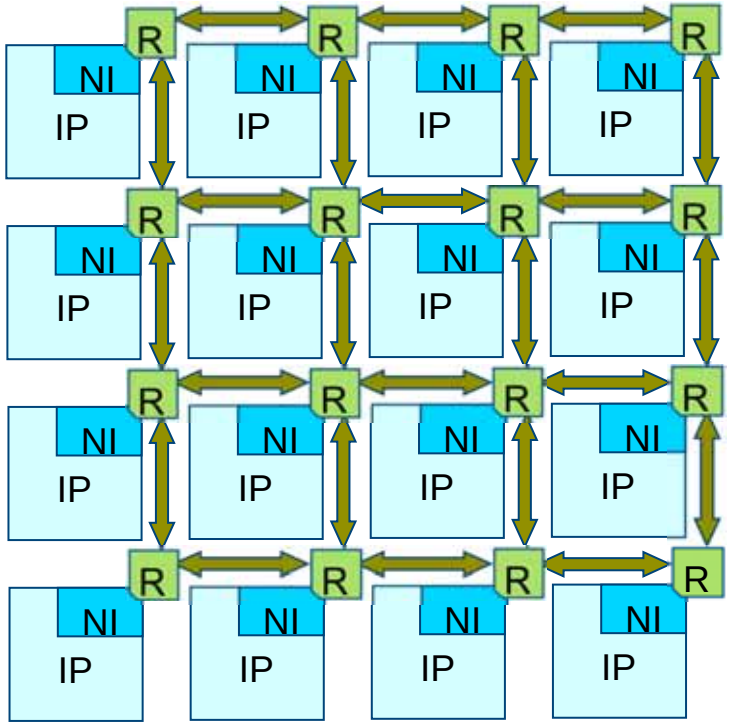
# Background

- Demands for integrating more and more cores into a chip
  - Eg. Automotive electronic systems
    - More than 50 ECUs are used in an automobile
    - Many problems in connecting them
    - New approach
      - Centralized architecture where many ECUs are contained in one chip



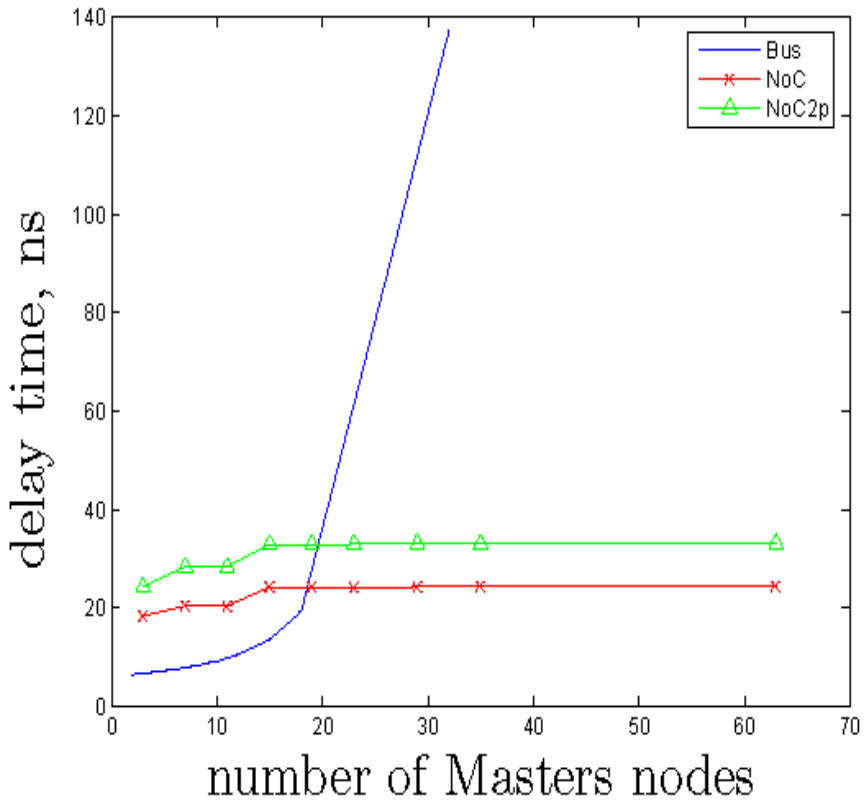
# Approach

- Network-on-Chip (NoC)




IP : CPU/accelerator core
NI: Network Interface
R: Router

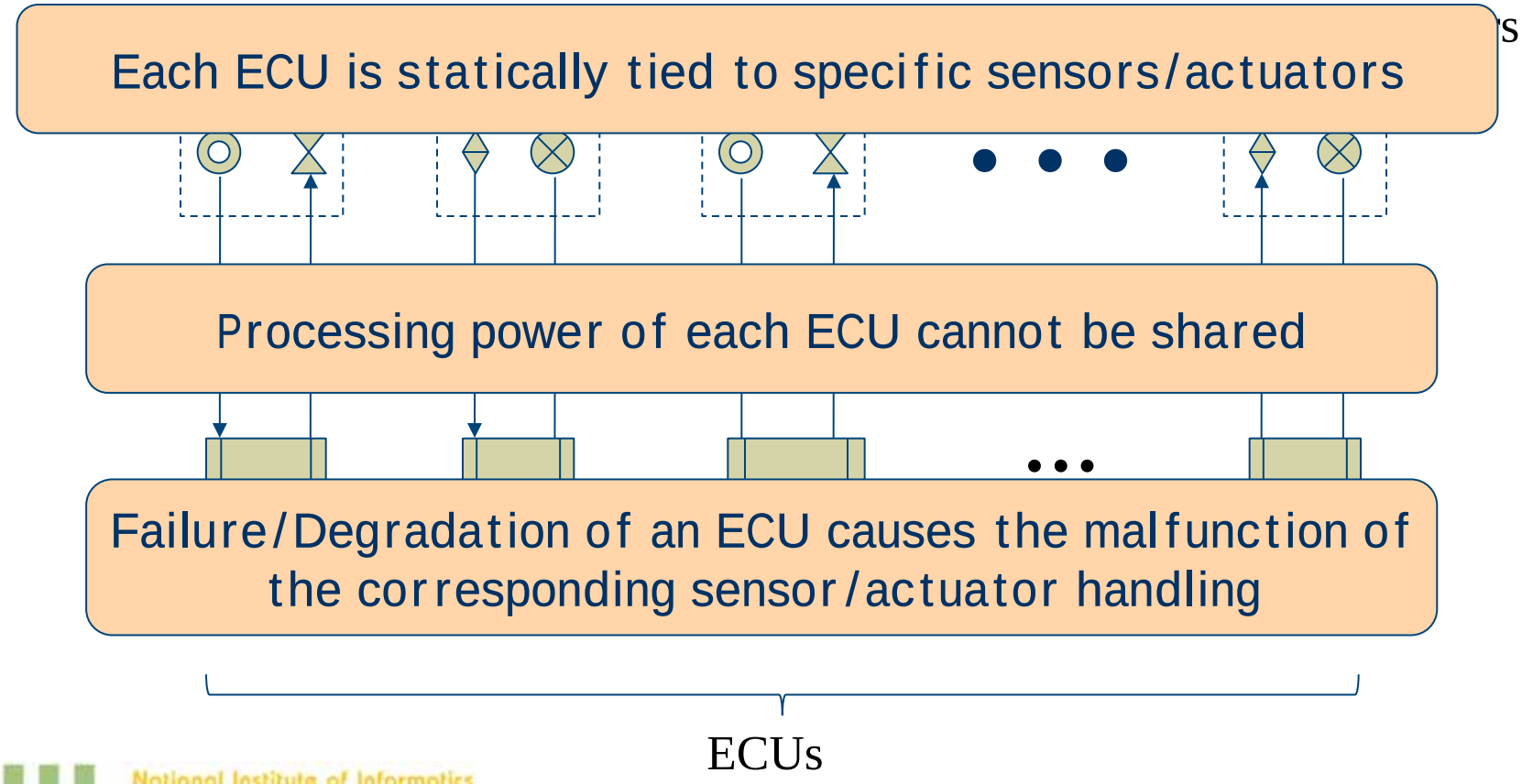
# Approach




*Asynchronous Network-on-Chip Communication Architecture Performance Analysis*
by
Bas Bijlsma and Rene van Leuken

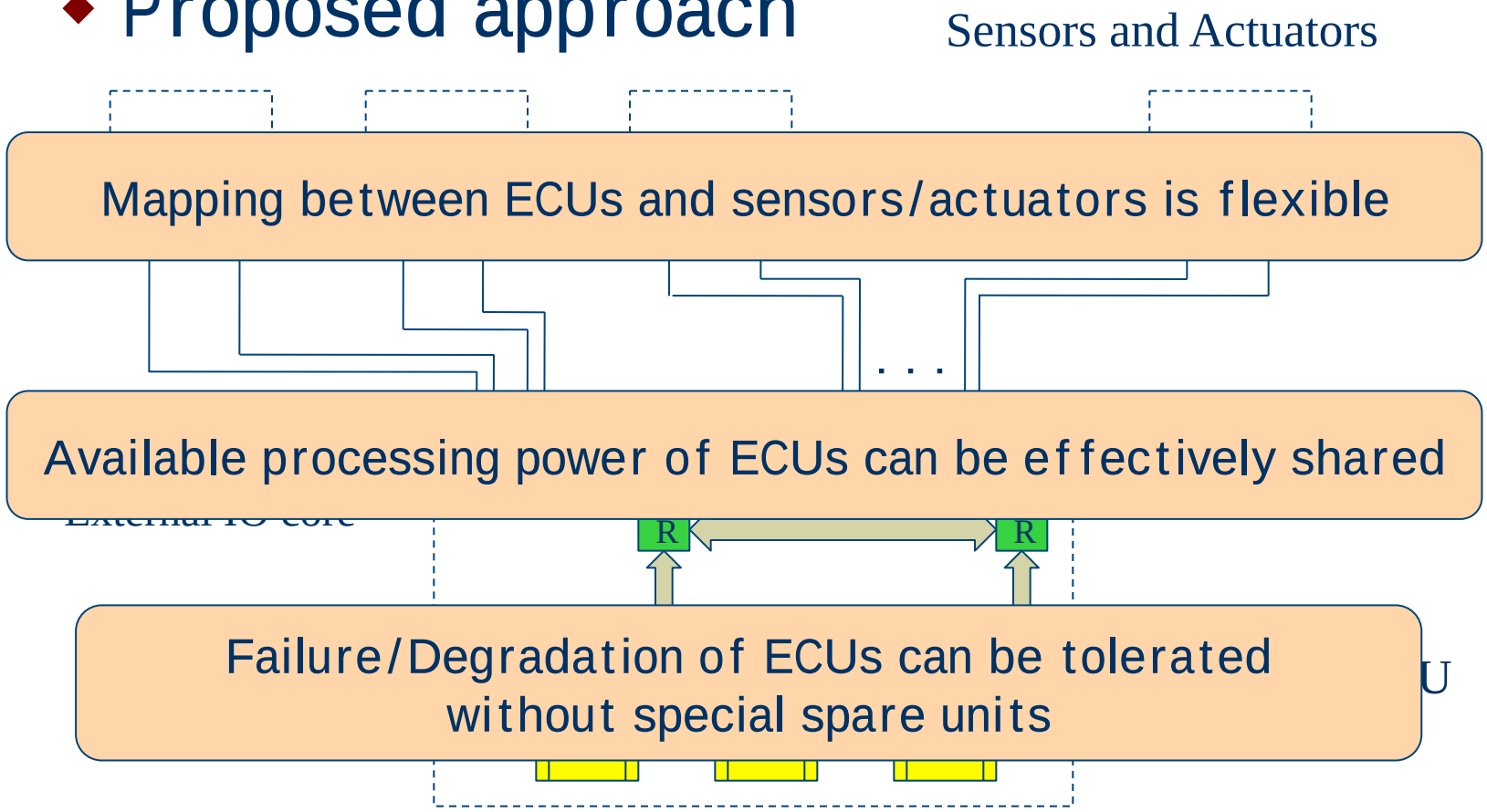
# Ideas

- Current implementation



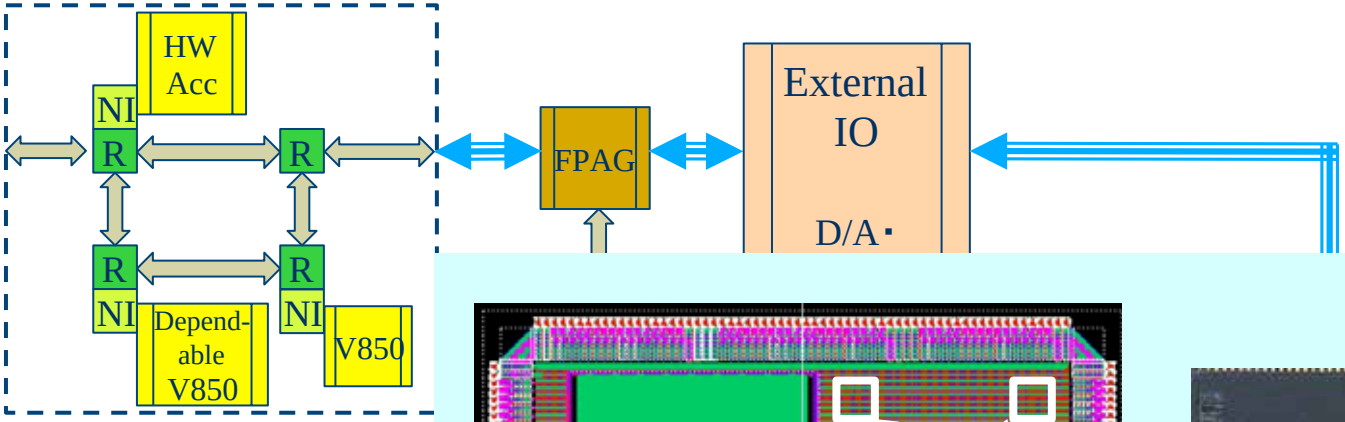
# Ideas

- Proposed approach

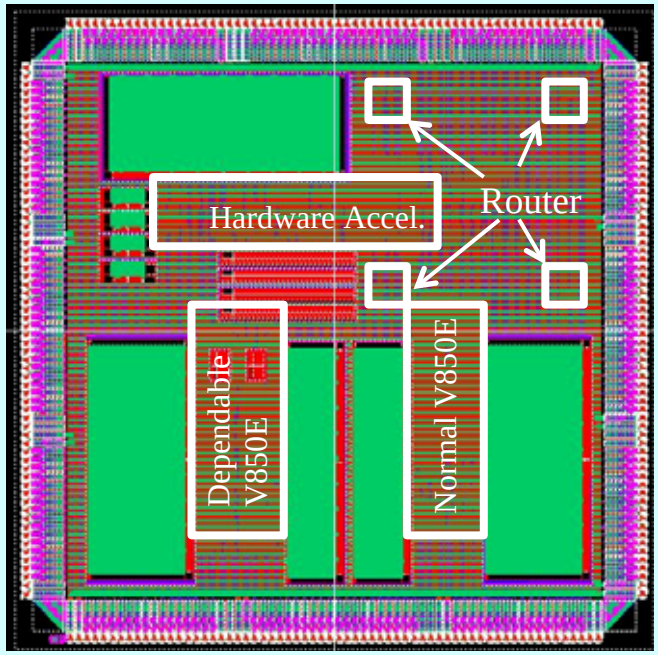


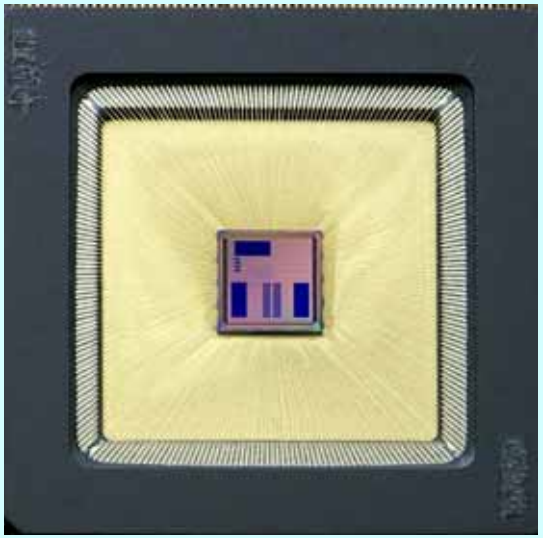
# First Stage Evaluation Model

LSI chip



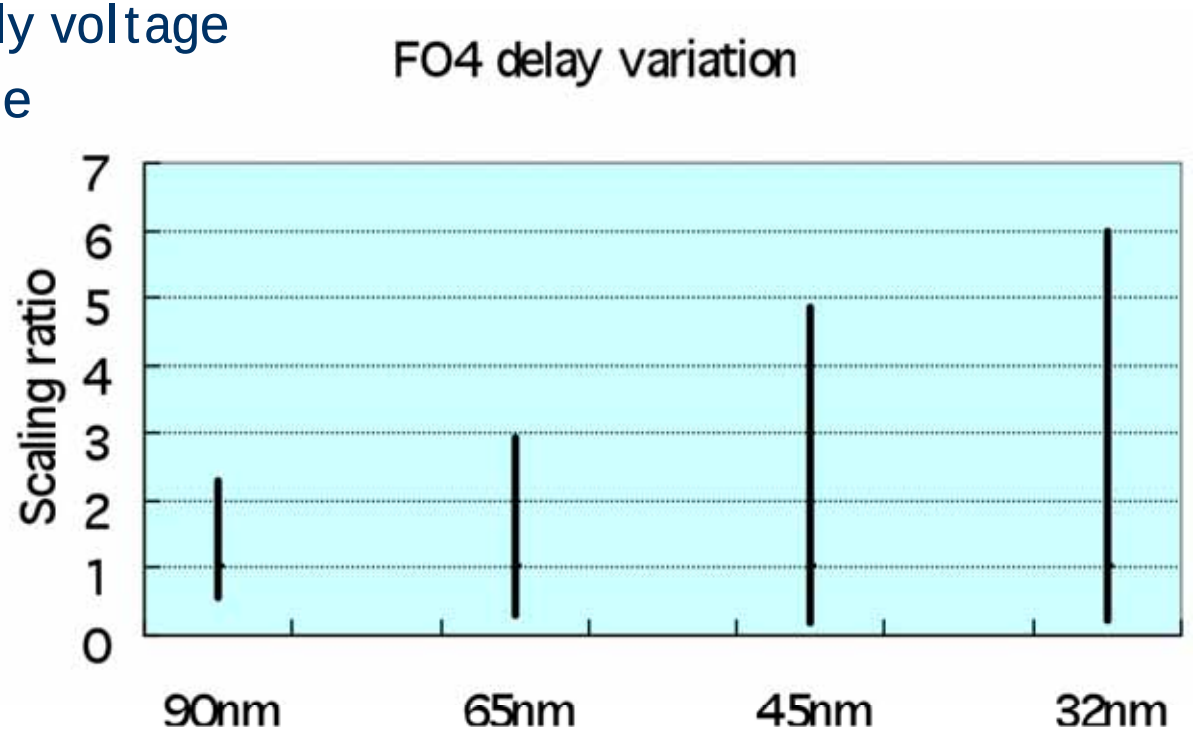

HILS (Hardwa
Loop-Simulati



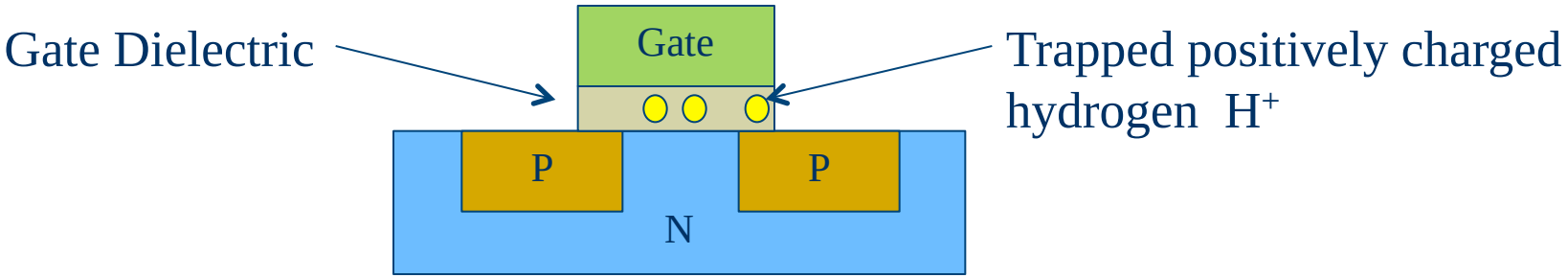
# Fault model focused

- Degradation (Delay fault)
  - Larger variations in transistor performance
    - process
    - power supply voltage
    - temperature



# Fault model focused

- Degradation (Delay fault)
  - NBTI (Negative Bias Temperature Instability)
    - occurs in PMOS Tr. stressed with negative gate voltages at elevated temperatures

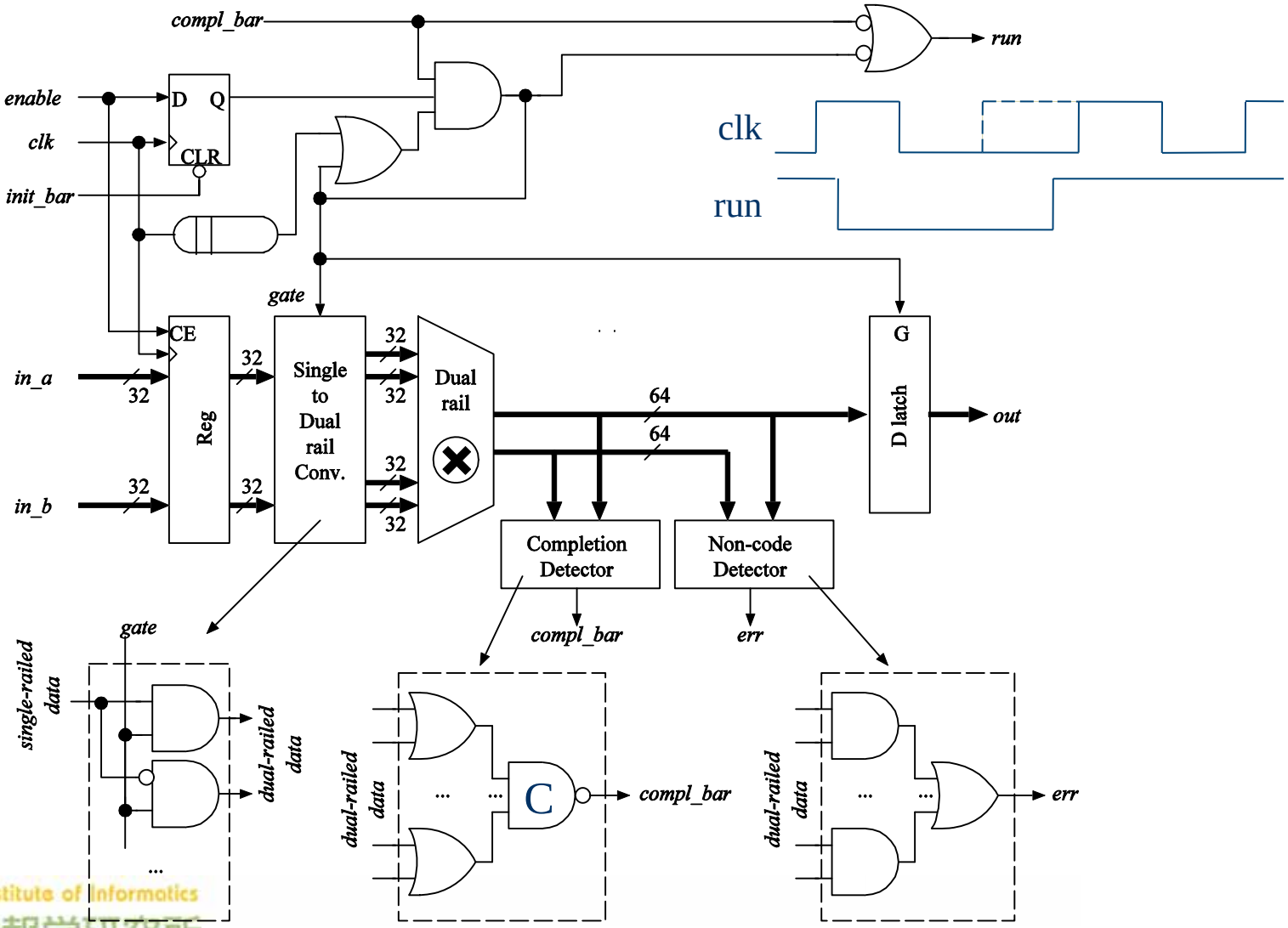



  - HCI (Hot Carrier Injection)
  - Threshold voltage $V_T$ increased, absolute drain current $I_{Dsat}$ decreased ⇒ increased delay

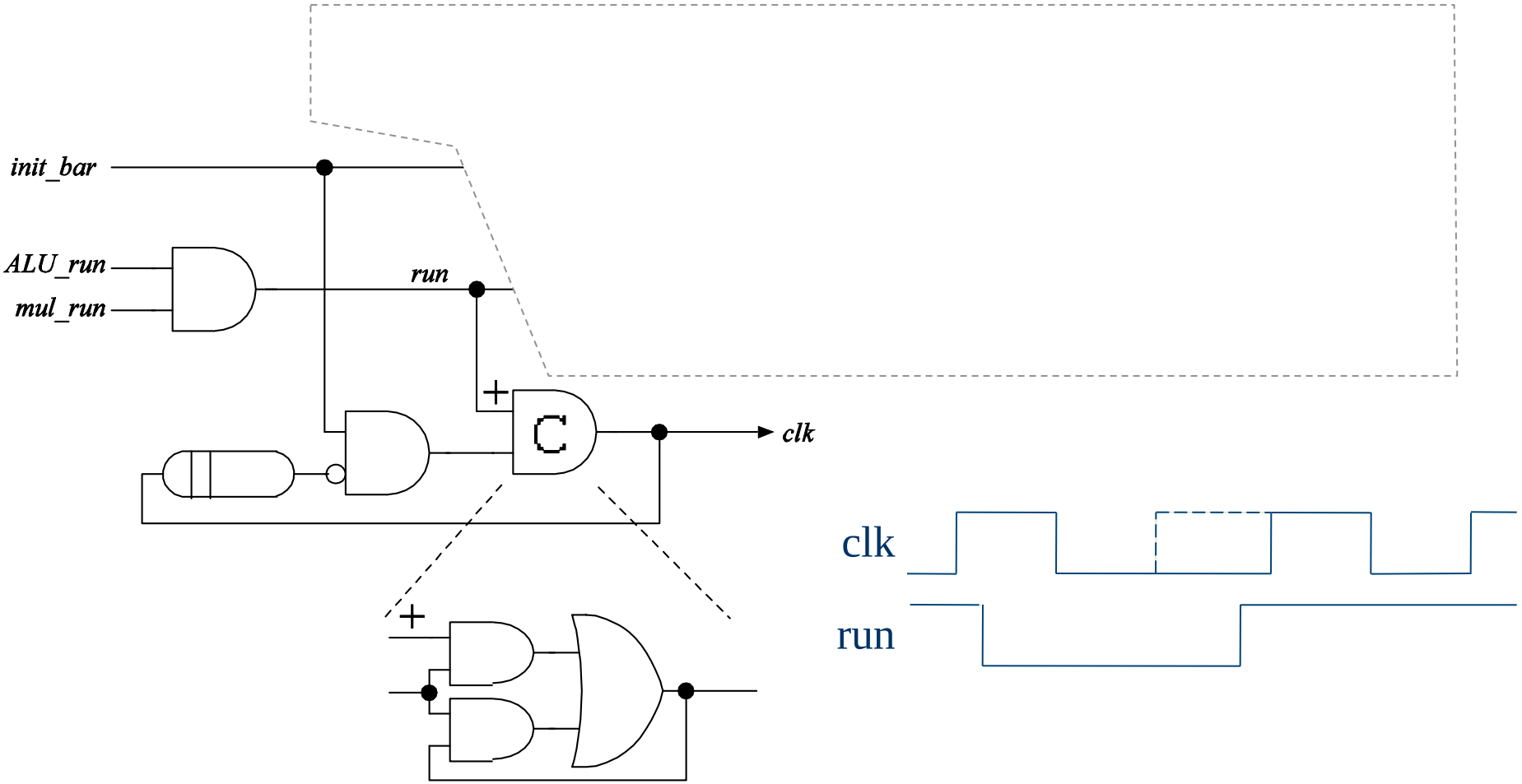
# Trials

- Dual-rail multiplier + Pausable Clock
  - Implemented in V850E core
- Asynchronous network-on-chip
  - Fully asynchronous router
  - 2 phase dual-rail data link

# Dual-rail Multiplier

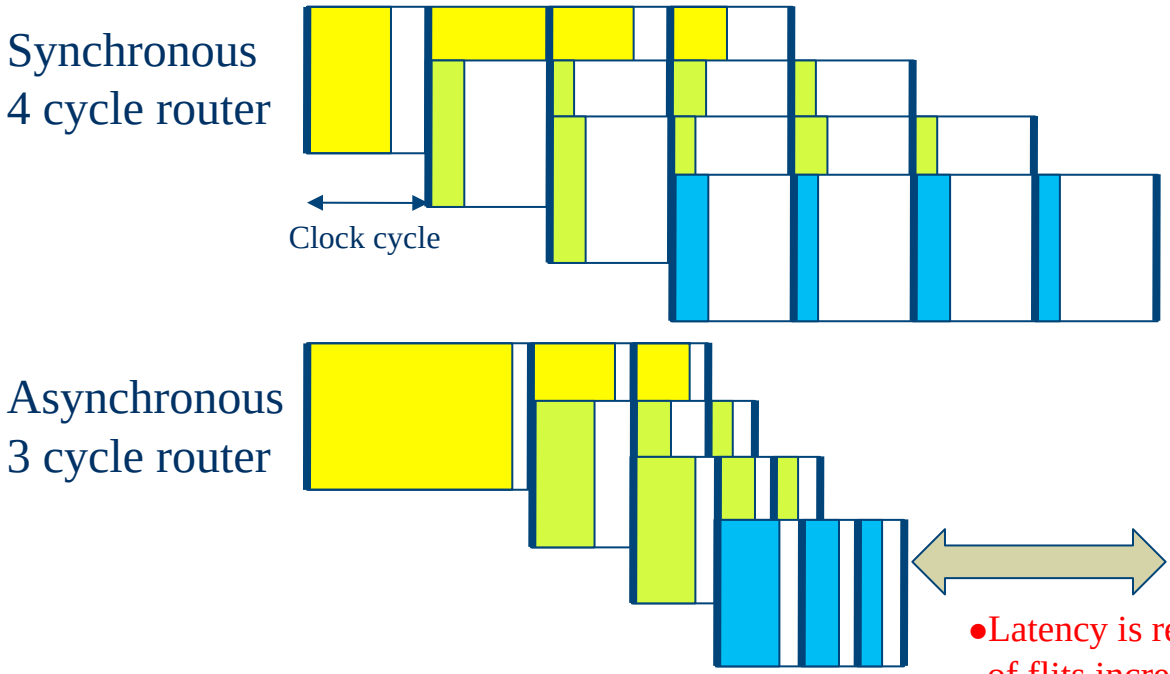


# Pausable Clock System



# Asynchronous Router

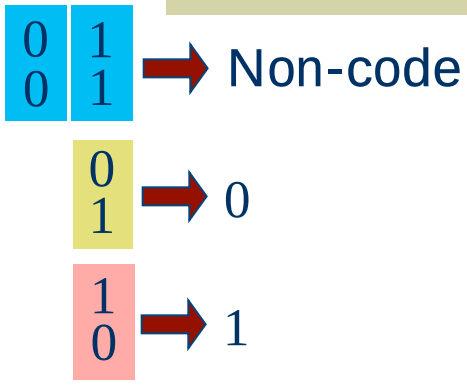
- Handling header flits takes longer time
  - Unnecessary slacks are given for the other flits for synchronous routers
  - Those flits can go quickly for asynchronous routers

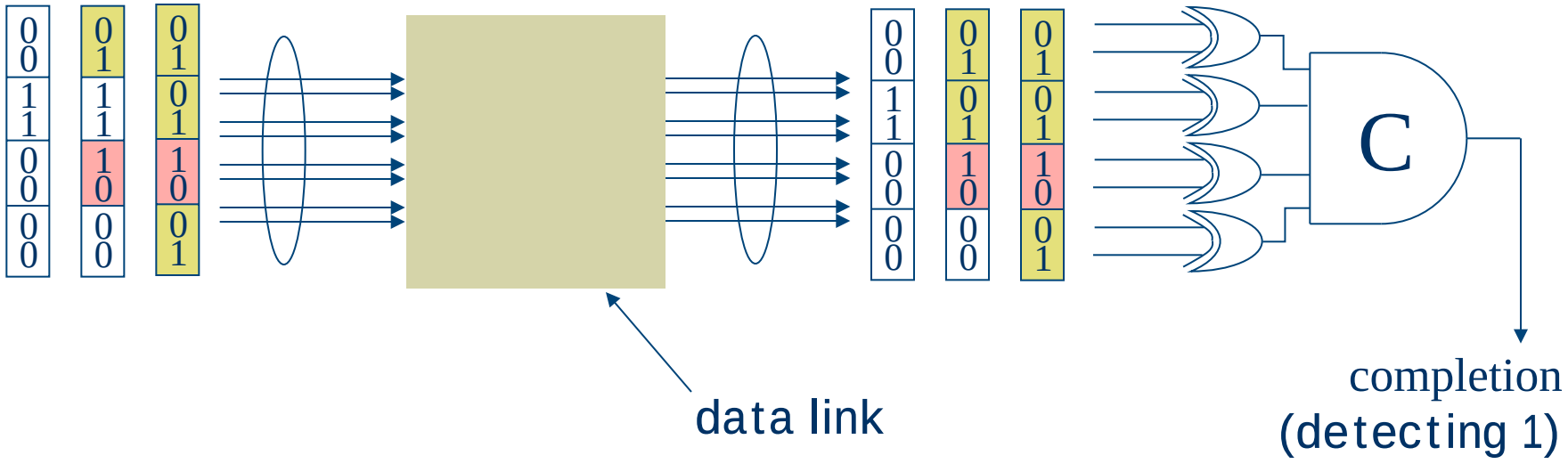



- Latency is reduced as the number of flits increases
- Path can be released earlier

# 2 cycle signaling dual-rail encoding method

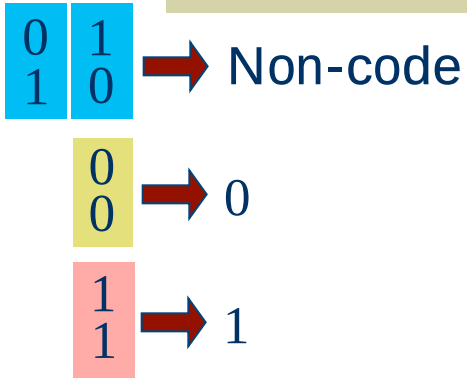
Odd-phase

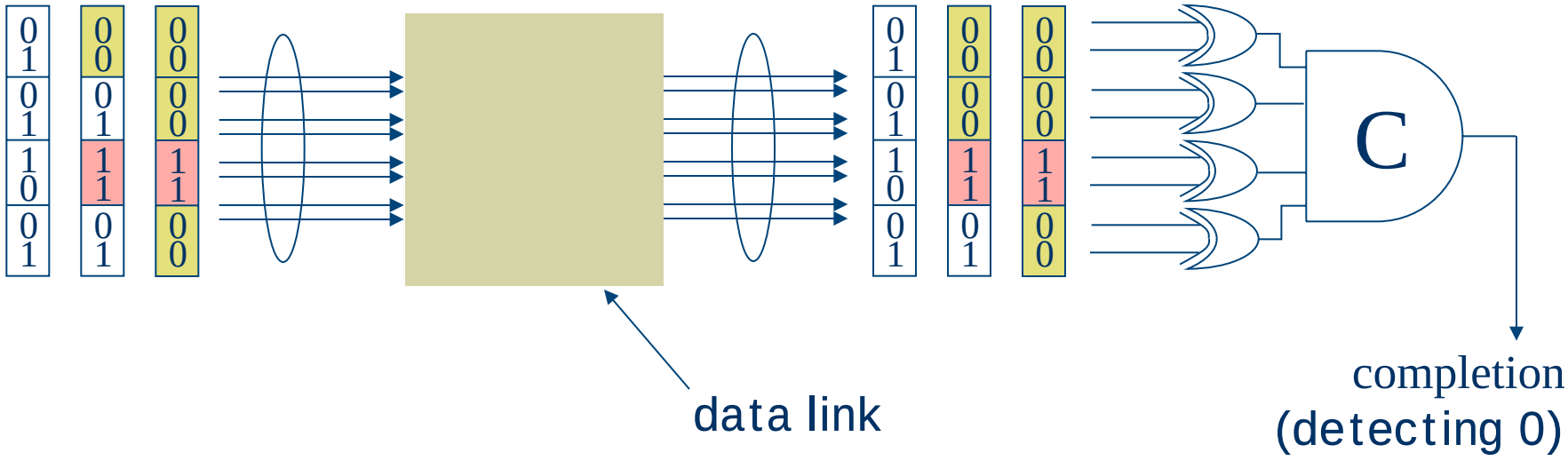


# 2 cycle signaling dual-rail encoding method

Even-phase



# Application

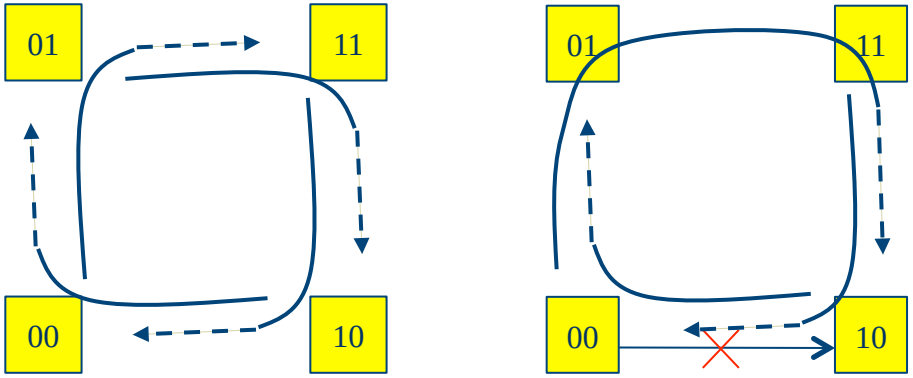
- Power train control for Prius like hybrid engine car
  - Gasoline Engine control
  - Torque computation for Engine, Drive-motor, and Dynamo
  - Brake control
  - Battery control
- Simulink model developed with an ECU company

# Next Stage models

- Implement stuck-fault tolerance
  - Dependable, deadlock-free, and adaptive routing mechanism for routers
  - Detection mechanism for links, routers, and cores
- Task allocation over NoC
  - Redundant task allocation for fault-tolerance
  - Mechanism to guarantee real-time property

# Deadlock

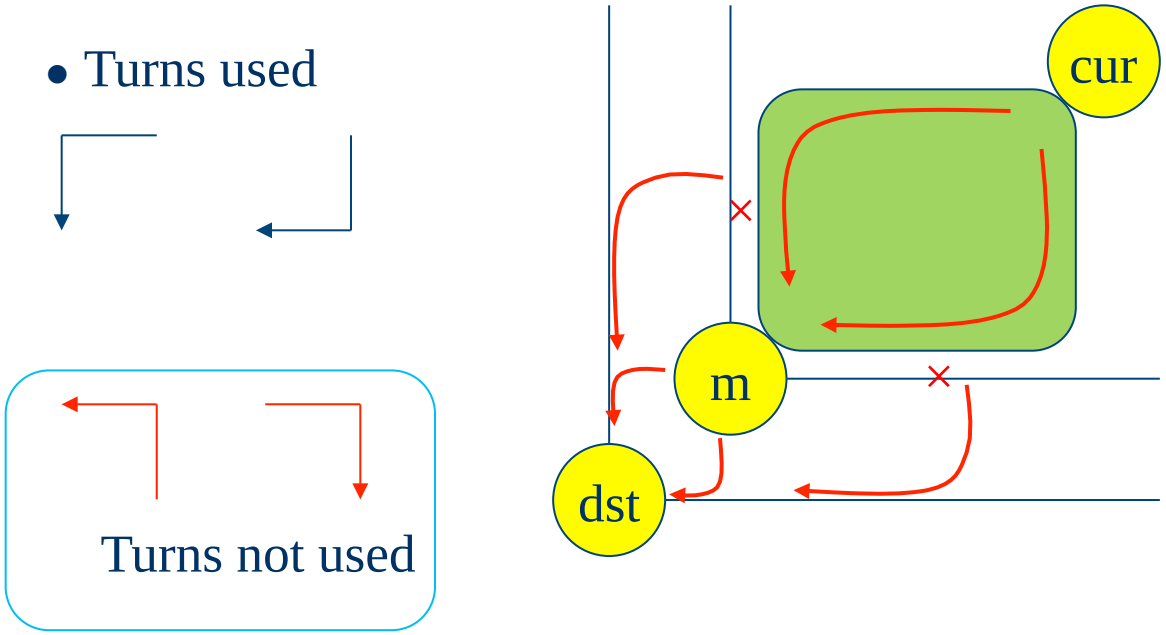
- Links are occupied by different packets in a cyclic manner




- Glass,Ni: Fault-Tolerant Wormhole Routing in Meshes, FTCS-23, pp. 240-249, 1993

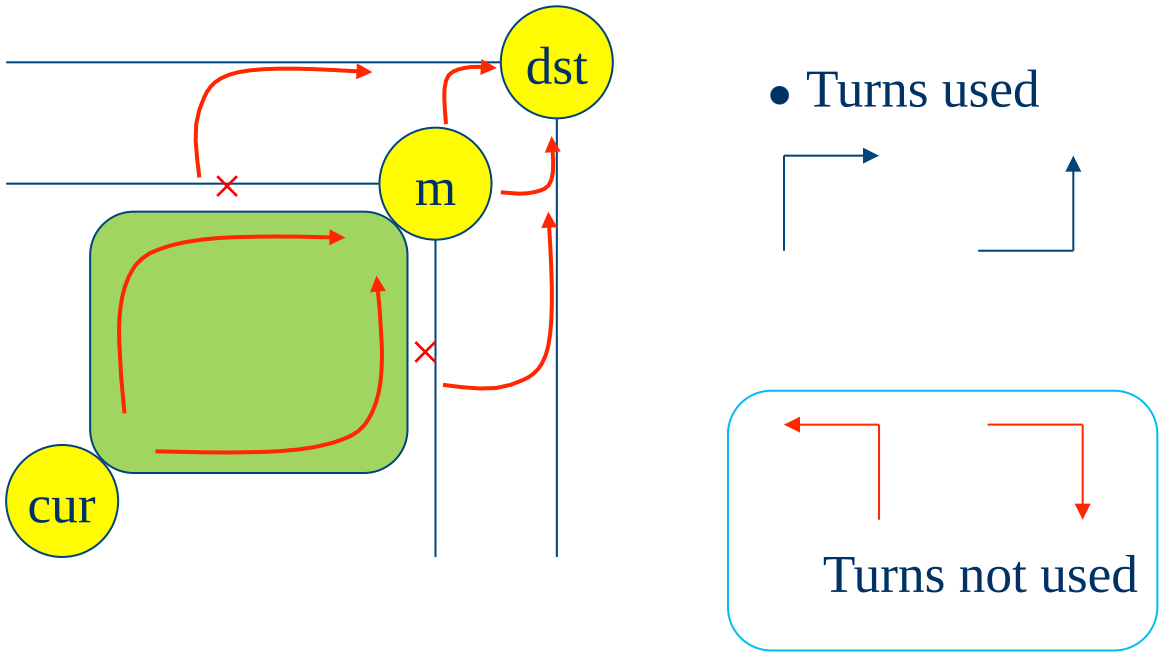
# Deadlock-free dependable routing

- cur_x > dst_x, cur_y > dst_y



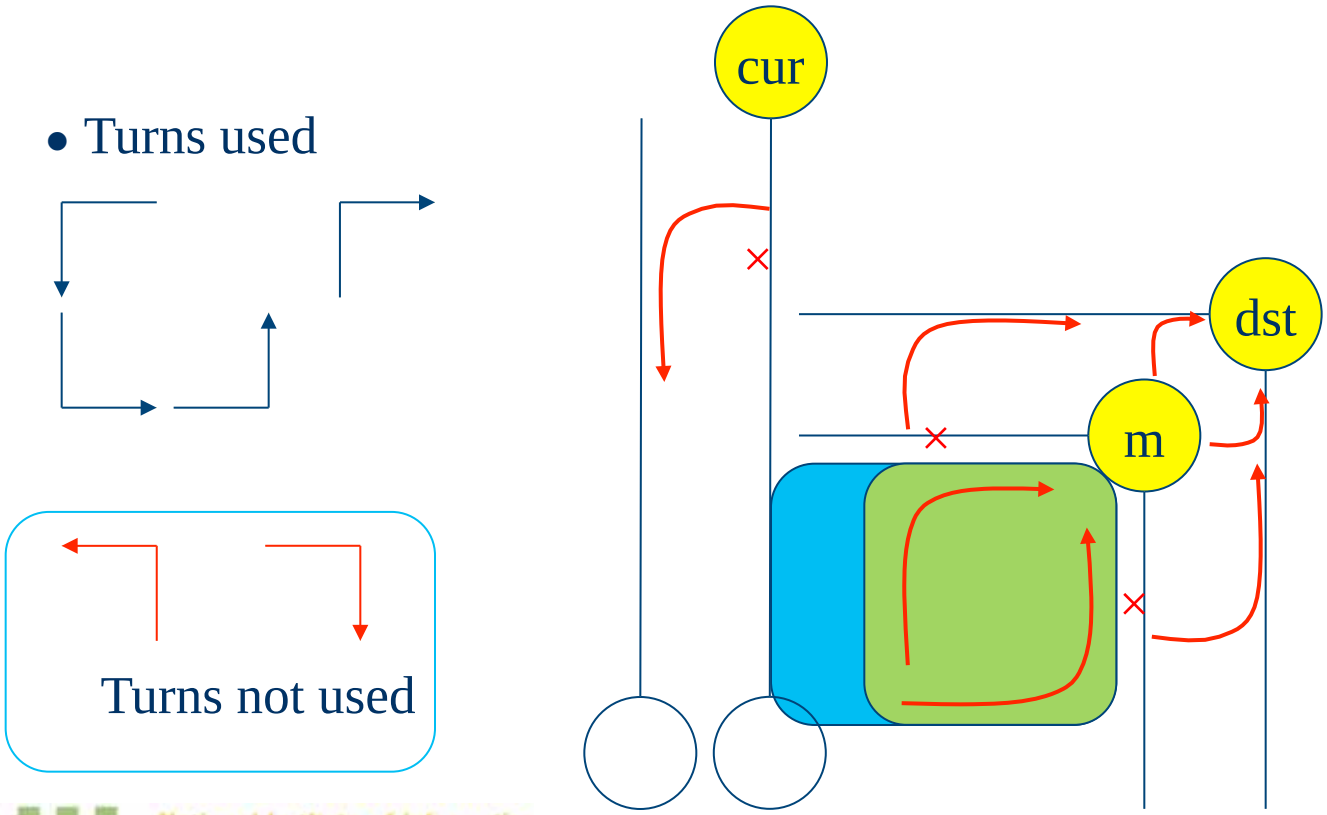
# Deadlock-free dependable routing

- cur_x < dst_x, cur_y < dst_y



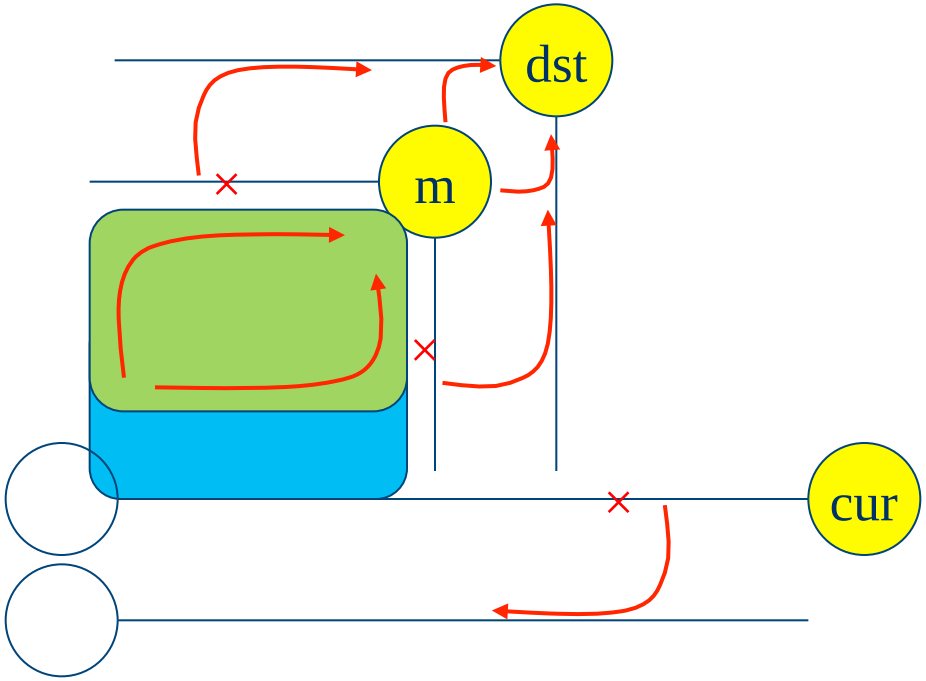
# Deadlock-free dependable routing

- $cur\_x \leq dst\_x, cur\_y \geq dst\_y$



# Deadlock-free dependable routing

- cur_x ≥ dst_x, cur_y ≤ dst_y




- Turns used